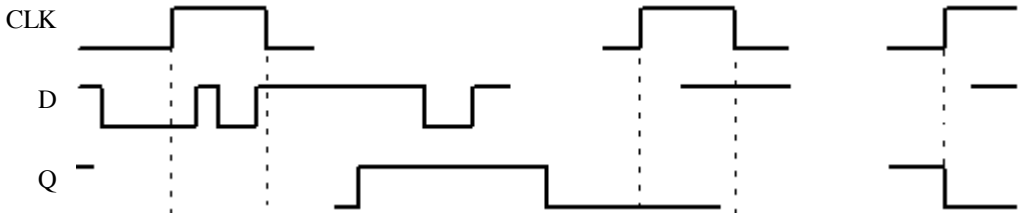
No.: _____(alphabetical number) **ECE 1250 homework # D3** b

Name: _____

1. Fill in the missing parts of the timing diagram below.



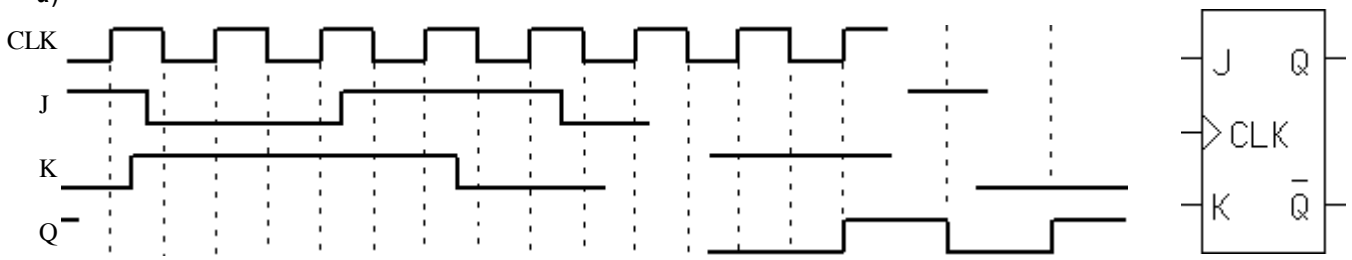
2. Fix the truth tables in Figures 12.85 (p691) and 12.86 in the textbook so that they match Figure 12.87 on the Reset and Set lines.

These two lines:

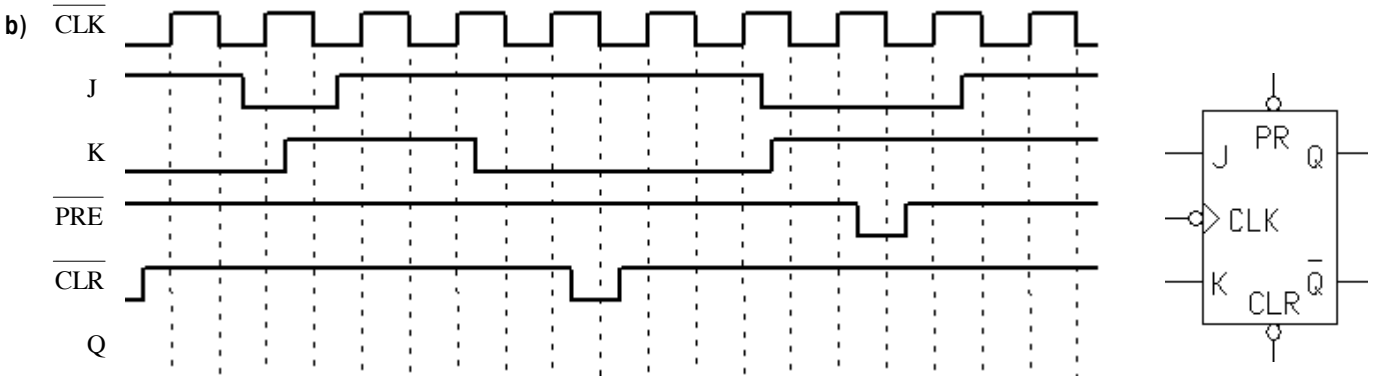
J	K	Q	$\overline{Q}$	Mode
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
0	1	0	1	Reset
1	0	1	0	Set
.	.	.	.	.
.	.	.	.	.

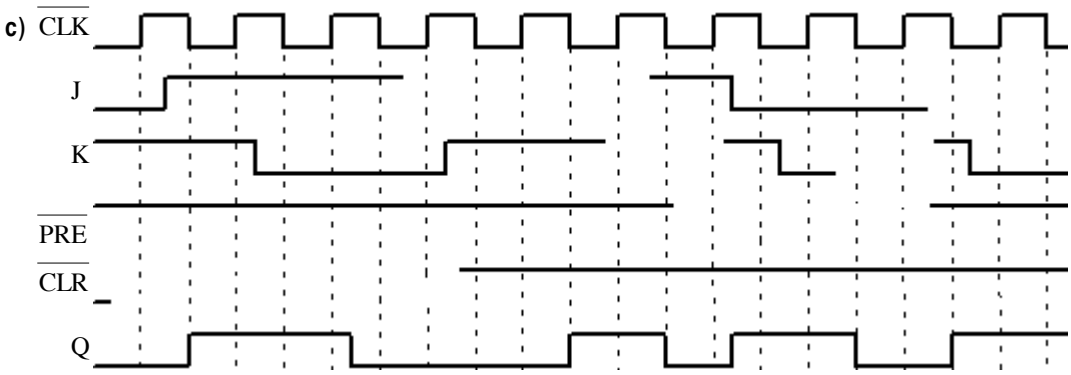
3. Fill in the missing parts of the timing diagrams below.

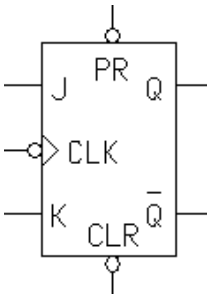
a)



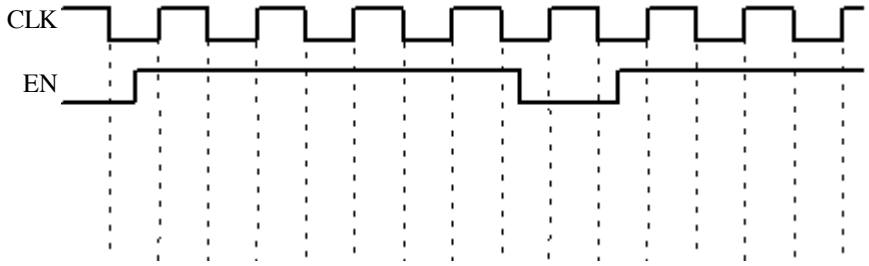
b)

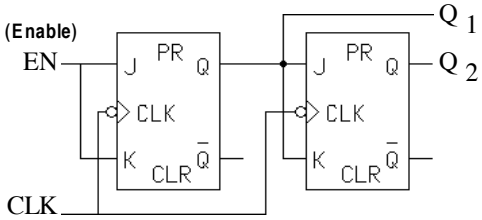


c) 



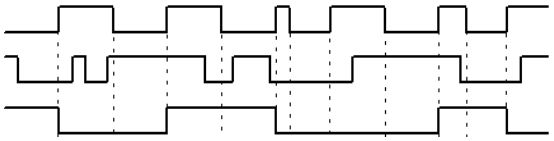
d)

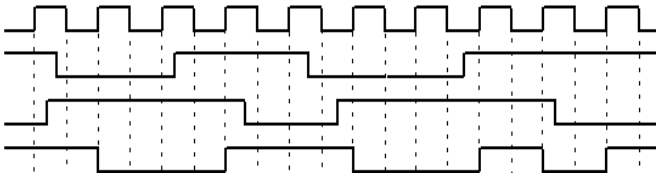


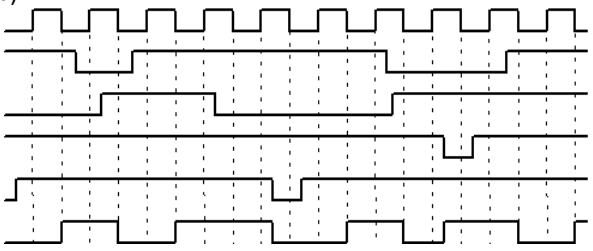


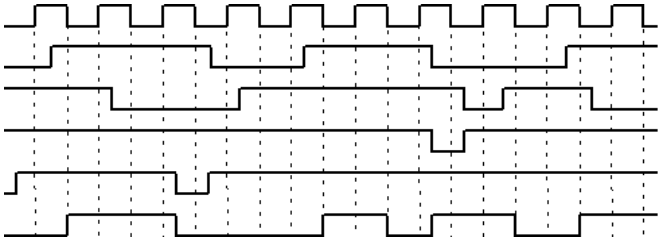
e) What does the circuit of part c) do when it is enabled and there is a clock.

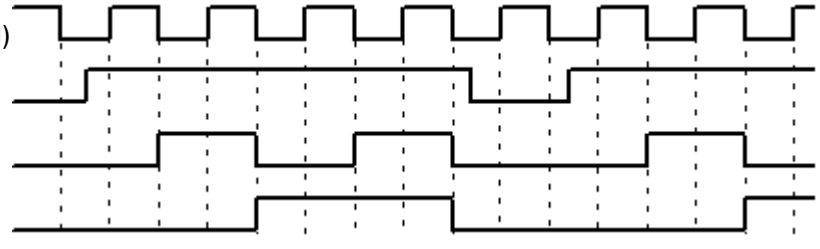
Answers

1. 

3.a) 

b) 

c) 

d) 

e) It's a two bit counter with the clock as the input, Q_1 as the LSB of the output and Q_2 as the MSB.