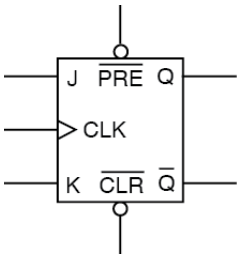
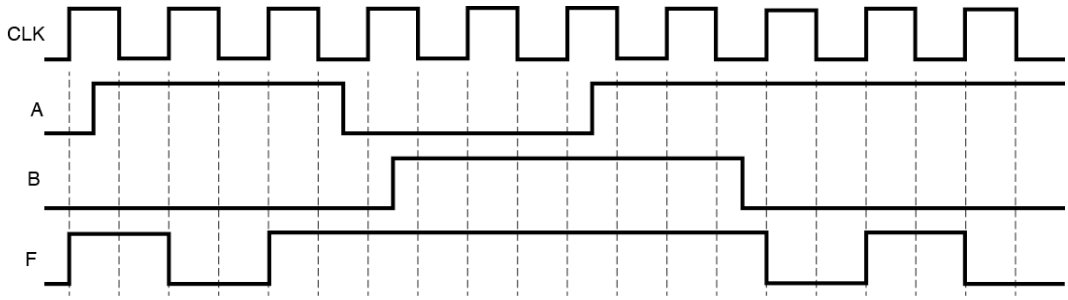
EX: Show the minimum logic circuit (using logic gates and a Flip-Flop) that has the following timing diagram. CLK, A, and B are inputs, and F is the output. You may use AND, OR, EX-OR, and NOT (inverter) gates. The optimal design has the minimum total number of gate inputs.

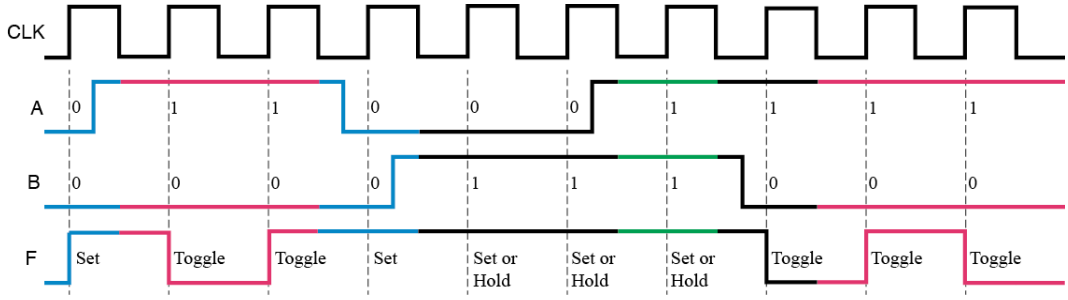


$\overline{PRE}$	$\overline{CLR}$	CLK	J	K	Q	$\overline{Q}$	MODE
0	1	X	X	X	1	0	Preset
1	0	X	X	X	0	1	Clear
0	0	X	X	X	-	-	not used
1	1	↑	0	0	Q	$\overline{Q}$	Hold
1	1	↑	0	1	0	1	Reset
1	1	↑	1	0	1	0	Set
1	1	↑	1	1	$\overline{Q}$	Q	Toggle
1	1	not ↑	X	X	Q	$\overline{Q}$	Hold



SOL'N: First, we observe that the up-going edge of the clock is where changes in the flip-flop output occur that are related to the J and K inputs. Changes in the flip-flop output occurring asynchronously, (i.e., not at the rising edge of the clock), would arise from the preset and clear inputs. There are no such changes, and we may conclude that the preset and clear inputs are irrelevant (i.e., disabled). Thus, they should be tied high.

Second, we observe that if the input signals A and B remain in the same state but the output signal changes state at the up-going edge of the clock signal, then the flip-flop has toggled. That is, J and K were both high. The segments in red in the timing diagram below are where toggling clearly occurs. We see that A=1, B=0 is toggle, for which J=1, K=1.



Other responses of the flip-flop are noted. (We assume that F is the Q output of the flip-flop.) A=0, B=0 produces a set condition of J=1, K=0.

A=0, B=1 produces set, which is J=1, K=0 or hold, which is J=0, K=0. And A=1, B=1 produces set, J=1, K=0, or hold J=0, K=0.

We have the following truth tables for J and K versus A and B:

A	B	J	K
0	0	1	0
0	1	0 or 1	0
1	0	1	1
1	1	0 or 1	0

The simplest solution is to have J=1 all the time, and for K:

$$K = A\overline{B}$$

The design: