NOVEL SINGLE-DEVICE “XOR” AND “AND” GATES FOR HIGH SPEED, VERY LOW POWER LSI MECHANICAL PROCESSORS

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ABSTRACT

We discuss novel functional MEMS/NEMS structures that enable implementation of universal logic gates such as XOR, AND, NAND, NOT, etc. in a single device instead of using 6-14 individual switches used in CMOS. By reducing the number of devices, our approach improves yield, reproducibility and speed and simplifies implementation of circuits such as adders and multiplexers. We show the feasibility of this novel approach through fabrication and testing of XOR, AND and related circuits such as a 2 bit full adder and multiplexer. The XOR gates with \~1.5V turn-on voltage at 50 MHz with \>10^9 cycles of reliable operations are reported. We also discuss the operation of XOR without deterioration at high temperature and in 90 kW ionizing radiation for 120 minutes.

KEYWORDS

MEMS microprocessors, MEMS logic gate, MEMS processors, rad-hard devices.

INTRODUCTION

Simple micro-electro-mechanical on/off switches have been reported during the past few years for applications in processors and to address power management in scaled VLSI, programming interconnect in FPGA’s, biomedical devices where it is desirable to reduce leakage power to prolong implanted battery life, and other applications in harsh environment where CMOS cannot operate due to high temperature or radiation \[1-9\]. Despite their very high off-to-on resistance \((100 \text{ G}\Omega \text{ to } 10 \text{ m}\Omega)\) ratios, and very low off-state leakage \(<10^{-14} \text{ A}\), MEMS switches tend to be slow \(<1 \text{ MHz}\), large \(>40 \mu\text{m}^2\), and unreliable with limited lifetime of \(~10^6\) operation cycles \[1-4\].

MEMS/NEMS switches have many interesting and challenging issues including: a) contact reliability, b) stiction problem related to release during fabrication and micro-welding during hot-contact operation, c) reliability of flexure structures usually used as part of the switch and d) particulate problems that occur during repeated operations that can lead to switch failure. To address some of these issues, our approach during the last two years have shifted from the CMOS paradigm that uses individual p- and n-MOSFET as complementary switches for implementing logic gates to functional structures described here. Here we discuss the fabrication and characterization of these novel single device XOR and AND gates using cross-bridge structures.

FUNCTIONAL STRUCTURE DESIGN

Fig. 1 shows the structure of the XOR gate where metal traces on overlapping bridge structures along with electrostatic actuation are used to realize the logic function. Other gates can be constructed using similar structures but different metallization/contact patterns as shown in Fig. 2 for an “AND” gate.

In Fig. 2 the cross sectional view of the XOR and AND device can be seen. The diagram has the two bridges, Gate 1, Gate 2, Drain and Source labeled.

The novel XOR gate device consists of two nitride bridges with patterned metallization (Figs. 1, 2 and 3).
The two gate regions attract each other only when one of them is high. When both are low or when both are high, there is no electrostatic attraction. When one of the gates is high, the drain and source electrodes contact each other and produce the desired output. This simple structure operates as an XOR gate (truth table is given in Fig. 2b). To prevent the drain-source electrodes from causing the attraction between the two bridges, their overlapping area is 4 times smaller than that of the gate electrodes.

![Figure 3: SEM of the XOR gate.](image)

Fig. 3 shows the SEM image of the XOR. The common implementation of XOR using 8 individual switches is shown in Fig. 4. The factor 8 reduction in device count and associated reduction in number of moving parts and areas lead to 8 times better reliability, at least 4 times faster gate, and proportionately higher yields. Moreover, multi-input (>2) gates can also be designed using the cross-bridge geometry with two or more metal traces for multiple contact electrodes. A 4-input XOR gate will compress the device count by x24.

![Figure 4: XOR implemented using individual switches require 8 devices each 25 μm² while our single XOR device requires only 25 μm² area.](image)

**FABRICATION**

The fabrication process flow for the device is given in Fig. 5. The conducting silicon wafer was insulated with 100 nm stoichiometric silicon nitride, first tungsten layer sputtered uniformly and patterned to form a “stationary” ground electrode. This electrode was used both as a gate in “MOSFET” like operation of the device as well as to use field effect to separate the two bridges if needed. The 100 nm tungsten was then capped with thermal 100 layers (~0.1 nm/layer) of Al₂O₃ deposited using Fiji ALD system and a second layer of LPCVD nitride (100 nm) was deposited and patterned to form the first nitride bridge.

![Figure 5: Fabrication process flow for XOR gate. The same process flow is used for AND gates, but with different Electrode structures.](image)

In step 6, the second layer of tungsten was deposited and patterned to form the electrodes on the first nitride bridge. ALD Al₂O₃ was subsequently used to cap the patterned tungsten, and also serve as the sacrificial gap between bottom and top electrode-bridges. This was followed by the third tungsten metallization and patterning to deposit the electrodes that reside under the second nitride bridge. Then, another patterned nitride layer was used to define the top bridge. After fabricating the whole structure that required 8 masks, the ALD layers were sacrificially etched in BOE etchant to “free” the two bridges from each other and from the substrate.

H₂O₂ at room temperature was used as the wet etchant to pattern tungsten resulting in a clean and uniform etch all over the wafer. Silicon Nitride was patterned using a dry etch recipe of CF₄/O₂ at 200W. This also resulted in a clean etch of the nitride bridges. The ALD Al₂O₃ layers acted as an effective etch stop for this dry etch recipe.

**TESTING**

The micro-fabricated XOR gate was tested for switching and its consistency using an Agilent 4156C
Precision Semiconductor analyzer coupled to a probe station. A switching voltage of approximately 1.5V was observed over repeated cycling (Fig. 6).

The devices were also tested under harsh conditions in an environmentally controlled chamber where temperature was monitored and maintained as required. The I-V characteristics of the switch at 298K and 409K are compared in Fig. 7. It reveals that the switching characteristics are consistent, even at elevated temperatures, albeit shifted by ~0.5V.

RESULTS AND DISCUSSIONS

The setup used to test the device is schematically shown in Fig. 8. As seen from the switching characteristics, the two gate regions attract each other only when one of them is high. No actuation results when either both gates are low or both gates are high. At the ON state (when the bridges contact each other), the drain and source electrodes contact each other and produce the desired output. This simple structure operates as an XOR gate.

The basic design of the device with “D” and “S” electrodes situated on separate bridges lead to very small leakage current that usually increases due to surface leakage currents that are absent in our structures.

Electrodes had dimensions on the order of ~2μm at the points of contact while the leakage current was less than $10^{-14}$A and the leakage power is shown in Fig. 9.

Fig. 10 shows the I-V characteristics of a MOSFET and a XOR gate connected as a switch in 90 kW ionizing radiation environment. The MOSFET became conducting after 120 minutes and the gate could not control the channel current. In the case of XOR switch, the switch characteristics changed but the device continued with clear “on” and “off” states.
As shown in Fig. 10b, in the case of NMOS, the $I_{DS}$ increased by an order of magnitude after 120 minutes at 90 kW and the gate voltage lost its ability in controlling $I_{DS}$. In the case of XOR gate, the 1-Vs are not affected much by the radiation. The TRIGA reactor at UoU was used in these experiments.

Figs. 11a-c shows a 1-bit multiplexer with 4 AND gates, 1-bit adder chip with 3 XOR and 2 AND gates, and a 2-bit full adder circuit utilizing 6 XOR and 4 AND gates that were fabricated and are being tested. 

CONCLUSION

We introduced functional MEMS/NEMS structures to implement logic gates in a single device instead of using individual switches commonly employed in CMOS. Given that 6-14 switches are typically needed in logic gates, the functional structures reduce the device count leading to better reliability, yield, speed and the overall better characteristics (sub-threshold characteristics, smaller turn-on/off voltage variations, etc.). We discussed fabrication and characterization of XOR gate as a specific example of a functional structure and discussed AND gates and circuits such as multiplexers, 1-bit full adder and a 2-bit full adder that employ the XOR and AND gates. We also showed that XOR gate can operate in ionizing radiation for 120 minutes while MOSFET becomes conducting and does not switch anymore.

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REFERENCES


Figure 11: Other circuits fabricated using single device MEMS based XOR and AND gates. a) 2-bit multiplexer, b) 1-bit full adder, and c) 2-bit full adder.