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Abstract—This paper is the second in a series of two papers describing the methodology and algorithms used in the development of MISTIC (Michigan Synthesis Tools for Integrated Circuits). Part I discussed the basic topological algorithms used to produce generic sequences of processing steps required for the fabrication of a given device structure. Part II discusses the expansion of these sequences into complete process flows. This procedure involves the selection of specific recipes from a set of available processing resources and the calculation of recipe parameters. These processing resources are stored in a database central to the MISTIC system framework. Since many process flows are generated for a given device, the paper also discusses the calculation of suitable figures of merit. The capabilities of the MISTIC system are demonstrated with a BiCMOS example. The MISTIC system framework which contains the basic compiler and several supporting modules: a device builder, process viewer, and database editor is also presented.

I. INTRODUCTION

In Part I, we discussed the basic algorithms that produce generic sequences of processing steps required for the fabrication of a given device structure. This paper describes how these sequences are expanded into complete process flows. The expansion begins with the proper selection of specific process recipes. These recipes are selected from a set of recipes specific to a fabrication facility. For example, a polysilicon etch step can be performed using many wet or dry etching recipes, but only a few may be available at the facility. This facility information is contained in the database of the MISTIC framework.

The generation of a process flow requires not only the selection of recipes but also the calculation of recipe parameters. These parameters must be calculated in a self-consistent manner. Some parameters are exclusively dependent on the characteristics of a specific device component, but others depend on the thermal history of subsequent steps. Further, for many recipes the parameters are not unique; hence their calculation is supplemented with auxiliary rules. Since many process flows are generated for a given device, each of these flows must be assigned a figure of merit. The calculation of the figure of merit must reflect yield, cost and include measures of parametric catastrophes. The database associates a unique recipe with a specific material. The recipe contains a set of general instructions for the basic operation, and the output.

II. RECIPE SELECTION AND PARAMETER DETERMINATION

Once an appropriate recipe is selected, its parameters are calculated. Most recipes hold parameters which are simply functions of the step outcome. However, the upper limit is determined by the maximum cost allowed for the step.

For example, a very useful auxiliary condition specifies that the duration of each step must fall within a practical time window

\[ t_{\text{min}} \leq t \leq t_{\text{max}}. \]  

\( (1) \)

The lower limit is determined in practice by equipment constraints such as its temperature ramping and stabilization time, and the upper limit is determined by the maximum cost allowed for the step.

The sections below discuss the selection of an appropriate recipe for specific steps, the recipe parameters, the parameter calculation, and auxiliary conditions.

A. Deposition Steps

Deposition recipes are selected based upon the material grown. The database associates a unique recipe with a specific material. The recipe contains a set of general instructions for the procedure indicating the equipment and its settings, and contains fixed numerical entries for the deposition temperature, temperature limits, and a unique deposition rate. The temperature is used for establishing material compatibility orders, and the rate is used to determine the step run time from the desired layer thickness.
B. Reactive Growth Steps

The calculation of the reactive growth times and temperatures accounts for the fact that MISTIC allows the growth of thick layers to be affected by that of thinner ones. Therefore the algorithm for calculation of the reactive growth time must first solve for the time of the thinnest growth followed by the next thinnest and so on. To perform this calculation, an ordered list containing all the reactive growth steps of the process is first constructed. Each of these growth steps \( g_j \) is assigned a label in the order as they appear in the process. Next a boolean influence matrix \( I \) is constructed. This square matrix has as many rows as reactive growths, and its entries \( i_{i,j} = 1 \) if \( g_j \) is influenced by \( g_i \). Next the gap list is sorted in order of increasing final thickness \( t_i \), and the growth time is calculated from the thinnest layer to the thickest as shown in the algorithm of Fig. 1. For a given growth, this algorithm first calculates forward in time the cumulative effects of earlier thinner growths using \( \text{ForwardCalculateThickness} \) arriving to the initial thickness prior to \( g_i \). It next calculates backward in time the effects of successive thinner grows in \( \text{BackwardCalculateThickness} \) arriving to the final thickness just after \( g_i \) is performed. From these two values, the algorithm next calculates the growth time for \( g_i \). This algorithm solves the thinnest growth first. Since the thinnest growth is not affected by any other growth; the time and temperature for that growth are calculated solely from its final required thickness. This information is used for the calculation of the second thinnest growth and so on until the sorted list is exhausted.

All parameter calculations use the familiar Deal-Grove model of oxide growth shown in Eq. (2). During growth \( g_n \), the oxide thickness change from \( x_i \) to \( x_f \) in an oxidizing environment at temperature \( T_n \) requires a time \( \Delta t_n \) determined from

\[
\Delta t_n = \frac{(x_f^2 - x_i^2)}{B(T_n)} + \frac{(x_f - x_i)}{B/A}(T_n) = \Delta t_n
\]  

(2)

where \( B \) and \( B/A \) are the quadratic and linear rate constants [1]. \( \text{ForwardCalculateThickness} \) solves \( x_f \) from \( x_i \) for all steps prior to \( g_n \), while \( \text{BackCalculateThickness} \) gets \( x_i \) from \( x_f \) for all steps following \( g_n \). The thickness, time, and temperature information for all growths at any given time is stored in the tableau matrix \( R \). For a specific growth step, the step time depends on the growth temperature; therefore the growth conditions are not unique. MISTIC solves this by imposing the time window auxiliary condition of Eq. (1). The function \( \text{CalculateGrothTimeAndTemperature} \) starts with an initial temperature of 1000 °C and finds the cycle time. If it falls within the window it stops otherwise it changes the cycle temperature accordingly in discrete steps until Eq. (1) is satisfied. Finally \( \text{ForwardCalculateThicknessesInAllRegions} \) determines the thicknesses in all unprotected regions of the device.

C. Etch Parameters

The primary function of an etch step is the selective removal of a layer segment of specific material. Ideally, the etch removes this layer without any attack to any other materials that may be exposed. In practice, a specific layer can be removed by many different etchants. Some of these can be highly selective to some materials but interacting with others. Therefore the etch recipe selection depends on the set of exposed materials and the device state at the time of the etch. For etching layer \( l_i \), this set consists of photoresist and the materials present just beneath the gap \( \Gamma_{i-1} \). For a given etchant attacking \( l_i \) the degree of attack on the rest of the exposed layers \( l_j \) is specified by the selectivity quantifier

\[
S(x) = \min_{l_j \in \Gamma_{i-1}} \left( \frac{R(\phi_E, l_j)}{R(\phi_E, l_i)} \right)
\]  

(3)

where \( R(l) \) is the etch rate on layer \( l \) and \( \phi_E \) is the selectivity. This parameter is directly related to device yield as a low
selectivity can compromise the device integrity.

MISTIC selects etch recipes such that layers are attacked at a reasonable rate yet having a negligible attack on other exposed materials. The lower limit on the etch selectivity \( S \geq S_{\text{min}} \) is determined from the maximum damage that other exposed components can withstand. A second consideration in the recipe selection is its etching time. Etchants with etching times within the suitable window of Eq. (1) are accepted to assure a reasonable process time. MISTIC scans the database and selects the etchant with the highest selectivity that meets both requirements. If no such etchant is found the process flow is discarded.

D. Lithography Steps

Lithography recipes consist of a dehydration cycle, resist application, soft bake, exposure and hard bake. The photoresist thickness is determined from the roughness of the surface topography. MISTIC contains several recipes that yield different resist thicknesses. Good resist coverage is accomplished when

\[
t_{\text{resist}} \geq \frac{1}{3} t_{\text{step}} \tag{4}
\]

where \( t_{\text{step}} \) is the maximum step on the surface profile at a particular time. Increasing the resist thickness improves its coverage but degrades the sharpness of the patterns. Therefore the minimum acceptable thickness is used unless the resist is severely attacked by an etchant.

E. Diffusions and Implants

Diffused layers are, in general, formed by an implantation step followed by an intentional drive-in, and other subsequent high temperature steps. Due to the inter-dependency among the diffused layers, diffusion and implantation parameters are solved simultaneously. In the input device file diffused layers are specified in terms of junction depth \( (x_j) \) and peak concentration \( (N_0) \). Implant dose \( Q \), energy \( E_I \), drive-in temperature \( T \), and diffusion time \( t \) are the parameters to be determined.

MISTIC calculates these parameters using two methods. The simplest scheme assumes that all profiles are simple Gaussians, and implants are considered to be shallow. Hence junction depths are computed from intersection between two Gaussians or a Gaussian and a constant background forming the set of simultaneous equations. This approximate method provides very fast solutions hence it is used for estimating parameters for the entire design space. The procedure yields reasonably close approximations to their actual profiles, provided the dopant concentrations are not too high, i.e., the material is essentially intrinsic at the diffusion temperature.

At high dopant concentrations, the diffusion coefficient depends strongly on concentration and local electric field; and the Gaussian profiles are inadequate. MISTIC uses a finite-element diffusion solver for the solution of high concentration, multiple diffusions on different zones of the device, but this method demands very long computation times. Thus, by default the Gaussian method is used for solving all diffusions, and the FEM solver can be invoked for a specific process. A detailed explanation of the numerical solver is beyond the scope of this paper and will be published elsewhere. A Brief description of its operation is given in [2,3].

III. Figures of Merit

The compilation procedure generates many process flows for a given input structure. In order to select the most appropriate process it is necessary to grade them with a suitable figure of merit. The figure of merit must reflect the virtues of the process; hence it must be related to the manufacturing yield. There are many sources of yield loss in a process. In some of them the influence on yield can be readily calculated, but others hold more subtle and qualitative character thus requiring empirical relations. Therefore the figure of merit must reflect yield loss from a diverse set of process characteristics in a unified manner. In the sections below, several quantitative and qualitative merit indicators are constructed and combined as a single figure of merit based on assumptions of independence.

A. Lithographic Defects:

An important source of yield loss originates from the presence of lithographic defects. There are two types of common lithographic defects. Random point defects are associated with dust particles or other point imperfections generated by the lithographic process. If these defects are uniformly generated across the wafer, some of these may land on a critical area of the device hence causing a failure. Systematic defects are associated with registration errors. For each lithography, a fraction of the features can be severely misaligned causing yield loss.

For each lithography, additional defects are generated; and a variable \( Y_i \) is associated with each yield loss mechanism. This yield loss is of course dependent on the size of the features and their spatial distribution on the wafer surface. Because many of these factors are unknown, MISTIC assumes that for each lithographic step, the yield will decrease by a fixed fraction.

MISTIC groups lithographies into critical, over-critical, and non-critical lithographies, each with different \( Y_i \). In critical lithographies, registration errors degrade the device behavior with characteristic yield \( Y_i \). In over-critical lithographies registration errors may cause the process to fail with yield \( Y_o < Y_i \). This occurs, for example, when the component defined by the lithography must be precisely aligned to the edge of an existing diffusion.

The contribution to the yield loss from registration defects is however eliminated if the device components are non-critically aligned. This situation is for example encountered in the fabrication of source and drain diffusions in a CMOS structure as well as during the placement of device implants where some of the patterns on the wafer surface act as masks. In these situations the yield is largest. If defect generation is assumed independent, then in a process with \( N_i \), critical, \( N_o \) over-critical, \( N_n \) non-critical lithographies, the quantity

\[
\mathcal{M}_L = Y_i^{N_i} \cdot Y_o^{N_o} \cdot Y_o^{N_n} \tag{5}
\]

is indicative of the overall yield loss from lithographic steps.

B. Dimensional Control:

The etching steps determine much of the dimensional precision of the device components. Therefore a dimensional figure of merit must reflect the degree of the chemical attack of these components in a quantitative manner. A candidate figure
of merit is hence related to the relative percent of material removed.

For example, in the structure shown in Fig. 2, component $c_i$ must be patterned from a uniform layer $l_i$. Due to variations and spatial non-uniformities in the etch rate, it is customary to over etch $l_i$ for a fraction 10-20% of the nominal etch time. Therefore the components below unmasked areas of $l_i$ are exposed to the etch for some time and are subject to chemical attack. For each of merit is hence related to the relative percent of material removed.

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$$
\Delta_{j,i} = f_{j,i} x_j,
$$

where $f_{j,i}$ is the fractional component damage

$$
f_{j,i} = \frac{c_{i,j} x_i}{x_j S_{i,j}},
$$

$x_i$ and $x_j$ are the corresponding component thicknesses, $S_{i,j}$ is the selectivity of the etch for $c_j$ respect to $c_i$, and $c_{i,j}$ is the etch time ratio for $c_j$ respect to the default etch time. If there are $m$ components exposed to the etchant, the material removed is the vector

$$
\vec{f}_i = [f_{1,i}, f_{2,i}, \ldots, f_{m,i}]^T.
$$

A measure of the overall fractional etch damage for $c_i$ is the normalized vector length

$$
\mathcal{F}_i = \left\{ \begin{array}{ll}
\frac{\|f_i\|}{\sqrt{m}}, & f_{i,j} < 1, \\
1, & f_{i,j} \geq 1,
\end{array} \right.
$$

which indicates how close the damage is to its maximum. A figure of merit for the etch is

$$
\mathcal{M}_i = 1 - \mathcal{F}_i.
$$

The damage caused by multiple etch steps is cumulative; therefore if component $c_j$ is subjected to $N_j$ chemical attacks its total damage is

$$
F_j = \sum_{i=1}^{N_j} f_{j,i},
$$

and for the entire device with $N_c$ components the cumulative fractional damage vector

$$
\vec{F} = [F_1, F_2, \ldots, F_{N_c}]^T.
$$

Following Eq. (9), the overall dimensional figure of merit for the device is

$$
\mathcal{M}_D = 1 - \frac{\|\vec{F}\|}{\sqrt{N_c}} = 1 - \frac{1}{\sqrt{N_c}} \left( \sum_{i=1}^{N_c} F_i^2 \right)^{1/2}.
$$

The main difficulty with Eq. (13) is that it weights damage for all components on an equal basis. This is not a realistic assumption since some components can be more influential than others, and the device may not function if the damage extends beyond a preset component tolerance.

This can be solved using a nonlinear transformation of the fractional damage. MISTIC uses the nonlinear degradation function

$$
D_i = \left( \frac{e^{\alpha_i F_i} - 1}{e^{\alpha_i F_i^*} - 1} \right), \quad 0 \leq F_i \leq F_i^*.
$$

as shown in Fig. 3. Under this transformation $F_i^*$ is an admissibility threshold. Any samples with fractional damage greater than this threshold have zero figure of merit. The parameter $\alpha_i$ can be adjusted to control the shape of the transformation. This is characterized by the half point goodness $\eta_i$

$$
\alpha_i = \frac{2}{F_i^*} \ln\left( \frac{\eta_i}{1 - \eta_i} \right).
$$

The device dimensional figure of merit is then

$$
\mathcal{M}_D = 1 - \frac{\|\vec{D}(\vec{F}, \vec{\eta})\|}{\sqrt{N_c}}.
$$

Table I below shows an example of the dimensional figure of merit for the BiCMOS example discussed in section IV.

C. Reactive Growth:

Reactive growths can be performed using either the etch back or localized oxidation technique. MISTIC prefers localized oxidations over etch back because the dimension of the reactively grown layers are better controlled under this scheme. Therefore a reactive growth figure of merit $\mathcal{M}_R$ is calculated. The merit is decreased for every occurrence of an etch back procedure. An intrinsic penalty of this preference is the fact that the best process may not be the shortest since the etch back method requires less steps due to the lack of the nitride patterning steps.

D. Substrate Planarity:

The topography figure of merit $\mathcal{M}_T$ is used to grade the planarity of the sample. In thin film devices it is desirable to work

\begin{align*}
\text{Fig. 2. Example of chemical attack of device components due to over etching.}
\end{align*}
### Table I
Total over-etch damage to device layers for the BiCMOS design example

<table>
<thead>
<tr>
<th>Layer</th>
<th>Name</th>
<th>Thickness (μm)</th>
<th>Over-Etch (μm)</th>
<th>Over-Etch (%)</th>
<th>η₀</th>
<th>F₁*</th>
<th>D₁</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si</td>
<td>SUBSTRATE</td>
<td>10.300</td>
<td>0.0417</td>
<td>0.40</td>
<td>0.80</td>
<td>0.50</td>
<td>0.0006</td>
</tr>
<tr>
<td>Phosphor</td>
<td>N-WELL</td>
<td>3.0000</td>
<td>0.0417</td>
<td>1.39</td>
<td>0.80</td>
<td>0.50</td>
<td>0.0022</td>
</tr>
<tr>
<td>Boron</td>
<td>P-WELL</td>
<td>3.0000</td>
<td>0.0221</td>
<td>0.74</td>
<td>0.80</td>
<td>0.50</td>
<td>0.0011</td>
</tr>
<tr>
<td>Pad Oxide</td>
<td>PAD OXIDE</td>
<td>0.0500</td>
<td>0.0076</td>
<td>15.30</td>
<td>0.80</td>
<td>0.50</td>
<td>0.0448</td>
</tr>
<tr>
<td>Stoch Nitrid</td>
<td>GROWTH MASK</td>
<td>0.1000</td>
<td>0.0036</td>
<td>3.63</td>
<td>0.80</td>
<td>0.50</td>
<td>0.0063</td>
</tr>
<tr>
<td>Wet Oxide</td>
<td>FIELD OXIDE</td>
<td>0.7000</td>
<td>0.0587</td>
<td>8.39</td>
<td>0.80</td>
<td>0.50</td>
<td>0.0178</td>
</tr>
<tr>
<td>Boron</td>
<td>BASE</td>
<td>1.2000</td>
<td>0.0358</td>
<td>2.98</td>
<td>0.80</td>
<td>0.50</td>
<td>0.0050</td>
</tr>
<tr>
<td>Phosphor</td>
<td>EMITTER</td>
<td>0.9000</td>
<td>0.0138</td>
<td>1.53</td>
<td>0.80</td>
<td>0.50</td>
<td>0.0024</td>
</tr>
<tr>
<td>Phosphor</td>
<td>COLL. CONT.</td>
<td>1.0000</td>
<td>0.0279</td>
<td>2.79</td>
<td>0.80</td>
<td>0.50</td>
<td>0.0047</td>
</tr>
<tr>
<td>Boron</td>
<td>BASE CONT.</td>
<td>0.9000</td>
<td>0.0221</td>
<td>2.45</td>
<td>0.80</td>
<td>0.50</td>
<td>0.0040</td>
</tr>
<tr>
<td>Wet Oxide</td>
<td>BASE OXIDE</td>
<td>0.2000</td>
<td>0.0616</td>
<td>30.79</td>
<td>0.80</td>
<td>0.50</td>
<td>0.2005</td>
</tr>
<tr>
<td>Dry Oxide</td>
<td>GATE OXIDE</td>
<td>0.1000</td>
<td>0.0047</td>
<td>4.72</td>
<td>0.80</td>
<td>0.50</td>
<td>0.0086</td>
</tr>
<tr>
<td>Poly n+</td>
<td>GATE POLY</td>
<td>0.5000</td>
<td>0.0221</td>
<td>4.41</td>
<td>0.80</td>
<td>0.50</td>
<td>0.0079</td>
</tr>
<tr>
<td>Arsenic</td>
<td>NMOS S/D</td>
<td>0.5000</td>
<td>0.0221</td>
<td>4.41</td>
<td>0.80</td>
<td>0.50</td>
<td>0.0079</td>
</tr>
<tr>
<td>Boron</td>
<td>PMOS S/D</td>
<td>0.7000</td>
<td>0.0221</td>
<td>3.15</td>
<td>0.80</td>
<td>0.50</td>
<td>0.0054</td>
</tr>
<tr>
<td>LTO undop</td>
<td>LTO1</td>
<td>0.2000</td>
<td>0.0066</td>
<td>3.30</td>
<td>0.80</td>
<td>0.50</td>
<td>0.0056</td>
</tr>
<tr>
<td>Poly n+</td>
<td>EMITTER POLY</td>
<td>0.7000</td>
<td>0.0221</td>
<td>3.15</td>
<td>0.80</td>
<td>0.50</td>
<td>0.0054</td>
</tr>
<tr>
<td>PSG hidop</td>
<td>LTO2</td>
<td>0.4000</td>
<td>0.0000</td>
<td>0.00</td>
<td>0.80</td>
<td>0.50</td>
<td>0.0000</td>
</tr>
<tr>
<td>Al2PECVD Oxide</td>
<td>METAL1 PASS</td>
<td>1.2000</td>
<td>0.0000</td>
<td>0.00</td>
<td>0.80</td>
<td>0.50</td>
<td>0.0000</td>
</tr>
<tr>
<td>Al2PECVD Oxide</td>
<td>METAL2 PASS</td>
<td>1.3000</td>
<td>0.0000</td>
<td>0.00</td>
<td>0.80</td>
<td>0.50</td>
<td>0.0000</td>
</tr>
</tbody>
</table>

with surface topographies that are as flat as possible. The lithographic pattern transfer quality is optimal when the resist is flat since the pattern sharpness is degraded by the presence of steep steps. The planarity of the sample is also important for the minimization of step coverage problems that occur in metalization processes.

MISTIC keeps track of all step heights on the surface at all times and reports the possible location of stringers. Stringers are leftover sidewall structures that develop during dry etching of a film over a steep step. In general, stringers cause problems because their removal requires a very long overetch (although sometimes stringers are formed deliberately). MISTIC then assigns an empirical merit based on the number of distinct stringers and the maximum profile step height occurring in the process.

### E. Component Proximity:

This merit indicator reflects the need to fabricate components very quickly one after the other. This situation for example is important in the fabrication of MOSFETs where any processing delays present between the gate oxide growth and the gate deposition severely degrade the device performance. The proximity merit \( M_P \) imposes an empirical penalty based upon the “process distance” between any two specified device components. The components are associated during their input in the device builder.

Ultimately, all merit norms must be combined in a single figure of merit. Since these are assumed independent from each other MISTIC computes their product

\[
FOM = M_D \cdot M_L \cdot M_R \cdot M_T \cdot M_P. \tag{17}
\]

This is the global figure of merit used to grade the various processes. Other more sophisticated merit models based on the cumulative yield loss originating from loading effect are discussed in [2] but have not yet been implemented due to the unavailability of experimental data.

### F. Process Costs:

The practical implementation of a device process in a fabrication facility is ultimately determined by its running cost. MISTIC determines the running cost of each process step using the calculated parameters for that step and a set of database cost entries for each step. For example, for a high temperature furnace step the wafers undergo a pre-furnace clean, temperature ramp up, constant temperature processing, temperature ramp down, and other less essential sub-steps. MISTIC uses a fixed cost for each fixed sub-step such as pre-furnace clean and a cost rate per unit time for each sub-step with variable processing time. After all sub-step and step costs are found, the total process cost is calculated. The calculated cost \( C_T \) and the process figure of merit are combined to determine the effective cost \( C_{\text{eff}} \)

\[
C_{\text{eff}} = \frac{C_T}{FOM}. \tag{18}
\]

This effective cost is used to rank the processes generated by the compiler.
IV. A Process Flow Design Example

The performance of the compiler was evaluated with the twin-well BiCMOS test example structure shown in Fig. 4. This structure was used as input to the compiler generating 36 possible process flows. The best process flow was then selected. The best process for the device structure, shown partially in Fig. 5, has 64 steps, 229 sub-steps, 19 lithographic steps, and 4 self-alignments, all using the localized oxidation method. The processing time for the device is 548 hours. In contrast, the second best process has only 56 steps, 211 sub-steps, 18 lithographies, and a total processing time of 534 hours, but the reactive growths were constructed by the etch back method resulting in a slightly lower merit. The synthesized process contains two self-aligned lithographies for the drain and source of the CMOS devices, but it does not show any threshold adjust implants or epitaxial growth steps as these have not yet been implemented in MISTIC.

In this process, the compiler properly selected the CF$_4$:CHF$_3$ He dry-etch recipe for the MOSFET contact holes and the vias for the two level metalization. The aluminum interconnects were etched using the standard wet etch recipe. The best process uses two localized oxidation steps for the growth of gate, intermediate (in the bipolar base), and field oxides. All reactive growth times and temperatures were calculated simultaneously. The etch of the nitride barriers was performed with a SF$_6$: He plasma because of its good selectivity respect to the underlying pad oxide film, and these barriers are stripped using a hot H$_3$PO$_4$ bath. The barrier pad oxide etch and stripping steps were performed using a weak HF solution.

The lithography recipes were fetched from the database based upon the topography present on the sample at the time of the lithography. The same 1.3 $\mu$m-thick resist was selected for all the process lithographies.

The diffusion requirements along with the thermal history of the process were input into the FEM diffusion solver to accurately determine all implant doses and diffusion cycle times. The process was then simulated with SUPREM III using the MISTIC-provided diffusion parameters. Figure 6 shows the comparison between the MISTIC solutions and the simulated values from SUPREM. The junction depths matched its specified target values within 3%. MISTIC also calculates several process statistics. Figures 7, 8, and 9 show the process time, running cost, and figure of merit (FOM) as a function of step number, respectively.

The steep steps in Fig. 7 are caused by the external out-of-fab implantations. The major sources of decline in the device figure of merit, shown in Fig. 9, are lithography steps, non-
localized reactive growth steps and proximity requirements of between layers. The large sudden declines in the figure of merit are caused by a combination of non-localized reactive steps and the proximity requirement between the gate oxide reactive step and the $n^+$ gate polysilicon deposition step. Additional results for NMOS and CMOS devices have been reported in [2].

V. THE SYSTEM FRAMEWORK

The MISTIC system consists of four different modules: the device builder, the compilation module, the process viewer, and the database editor all centered around a common database. These four modules are supervised by a program manager which controls the operation and data flow between the different modules as illustrated in Fig. 10. The compiler module is the system core and contains all the algorithms. The builder is a graphical drawing tool used for the specification of the device, and the viewer displays process statistics, run sheets, and the cross-section of partially built devices at any point in the process. The database contains many recipes for each type of step and physical properties of device materials. This information is used throughout the framework for the calculation of recipe parameters and the determination of logical decisions during the process flow assembly.

A. THE DATABASE ENVIRONMENT

The database is central to the compiler and all parts of the program access it. The database consists of a collection of different records called atoms. These atoms contain information (e.g., rates and times) about individual process recipes for steps such as etching, deposition, diffusion, and lithography. This information can be stored in different formats. The representation of process recipes using elaborate data structures has been studied rather extensively over the past decade [4–6]. These representations can be complex due to the wide variety of recipe types and a potentially large number of recipe parameters. These sophisticated representations are suitable for highly optimized recipes. Much of the information stored inside MISTIC contains recipes which are not thoroughly characterized or understood; therefore, a much simpler representation was adopted. The MISTIC database structure contains two basic types of atoms, process and parametric recipes.
Process atoms are stored as parametric recipes. These recipes contain descriptive information and numerical parameter information. For example, the process atom for an etching step contains a paragraph with instructions for preparing the sample and the specification of equipment settings, and parametric information such as etch rate and selectivity. The descriptive information is directly copied to the process flow run sheet while the parameters are used in calculations. Material atoms contain data on physical properties of specific materials. For example, all dopant information is stored in material atoms. Material atoms associated with deposited materials also contain a process sub-atom with a parametric recipe for its deposition procedure.

The parametric recipes used in MISTIC are rigid with very few variable parameters (usually just one). This is in sharp contrast to other approaches where many recipe parameters can be adjusted according to an expected surface response curve [7]. The rigid parameterization used here is largely justified by the very sensitive behavior of thin film equipment since only finely-tuned recipes give reproducible results. For many MISTIC recipes, the only adjustable variable is the process time, and recipes which work well with many different settings are stored under different names. While somewhat restrictive, the rigid recipe approach is consistent with the way the majority of industrial facilities work today.

Database atoms may be general or lab-specific. General atoms contain information that is always valid such as the chemical composition and rates for wet etch solutions that can be prepared anywhere. Lab-specific atoms contain processes that may be applicable to a particular facility. The database files are hence organized into libraries. In this manner the compiler can generate process flows for different facilities by just uploading a particular lab-specific database file.

When the program manager is invoked, MISTIC uploads the corresponding database files and stores them in the computer memory for access from the other modules. Currently the database contains 50 deposition atoms, 4 different lithography atoms, and about 500 etchant atoms constructed from experimental data collected at the University of Michigan Solid-State Electronics Laboratory and etch data published elsewhere [8, 9].

B. The Device Builder

The device builder is a graphical drawing tool. Devices are schematically drawn on a two-dimensional canvas as a collection of polygons, each corresponding to a single component. In order to draw a component, the type menu is first selected. This menu identifies the type of layer being drawn such as deposition, reactive growth, diffusion, and sacrificial type layers. For each layer type there is a list of possible materials. When a material is selected, the layer menu is displayed prompting for its desired thickness. In addition to graphical editing commands, the device editor has special drawing routines for the calculation of conformal outlines on top of the current device profile and provides customized procedures for drawing reactively-grown layers and diffusions (both self-aligned and non-self-aligned). The device structure is represented as a list of polygons stored in a text file.

C. The Compilation Module

This module contains all the topological algorithms and the recipe parameter calculators. The module assembles process flows supporting self-alignment of diffusions, implantation of dopants through thin layers, localized oxidation and provides simultaneous solutions of multi-zone diffusion to specified target junction depths.

Since many process flows are created for a given device, the compilation module also grades the merit of each process flow subject to several criteria. MISTIC constructs figures of merit from the process robustness, the processing costs, and the dimensional tolerances that can be achieved. One of the most significant modes of failure is caused by overetching of device layers due to the finite etch selectivity. MISTIC rejects flows where the overetch exceeds a specified threshold limit that determines the proper functioning of the device. Processes that pass these tests are assigned a tolerance merit. The actual flow cost is next calculated and a combination of these two quantities is used to provide an overall effective cost. This cost is finally used to rank each flow in order of preference.

MISTIC stores the compilation results in several process files. For each process generated, the files contain both device process and profile information at any given time in the process organized in the following categories:

a) Detailed Run Sheet: The compiler generates a synthesized run sheet file for the device process that contains all the information necessary for the device construction in a particular facility. Each run sheet is a list of numbered process steps, each with detailed recipe directions including processing time, equipment identification, and settings.

b) In-Process Device Cross Sections: The compiler module stores partial device cross sections at all times in the process flow. This information is used to display the sequential construction of the device in the viewer module. Cross section information is also useful to determine how a device looks under a microscope thus establishing a frame of reference for the detection of processing errors.

c) Simulator Interface Files: MISTIC generates input files for other TCAD programs permitting the simulation of the synthesized process with other TCAD tools. Currently MISTIC generates SUPREM III deck files over multiple one-dimensional re-
regions intended for the accurate simulation of the compiled process.

d) Process Statistics: For each process flow generated, a summary is generated. In this file several statistics are recorded including the number of steps, the number of photolithographic masks, the number of self alignments, the total process time, and the processing costs. The summary also contains several empirical figures of merit used for comparison purposes. and keeps track of process flow statistics for the entire design space.

D. The Process Viewer

The process viewer retrieves information from the compilation module output files and displays it in various formats. By default the viewer reads the first flow and generates schematic cross-sections of the device at each different step in the process flow, but has the capability to read all generated process flows. Different flows can be selected from the process selection window that displays various statistics for all the generated device flows. The main viewing area contains a process summary area for each selected process flow listing number of process steps, number of substeps, number of masks, total processing time, total cost and figure of merit. The main viewing window also contains process recipe display window enumerating all processing steps and substeps. This process recipe display can be printed in latex format or ascii text format. The main portion of the viewer includes a device cross-section display window. Each process step can be visually displayed. Device cross-sections and all other outputs, for example, process run sheets and SUPREM deck files, can be saved or printed from this module.

VI. Discussion and Improvements

The compiler developed here provides a fairly detailed version of the device process but not complete. A number of improvements to of the topological and numerical algorithms should be included in future versions.

The determination of threshold-adjust implants is not currently supported. These implants affect the entire process and present additional constraints in the order of steps; therefore they should be included.

An obvious missing step in the example run sheet of Fig. 6 is the placement of alignment keys. Alignment keys are necessary for the alignment of the device components in the substrate and should be constructed in a manner that minimizes the process steps.

The current version of MISTIC does not have a time-etch capability. It is important to have this capability because without it the program cannot deal with substrate etching which is necessary for a large class of MEMS devices. It also does not include any capabilities for anisotropic etching.

In MEMS devices, the automatic placement of sacrificial layers and the generation of its corresponding process steps is very desirable. Sacrificial layers are interesting research subjects. These layers must be deposited and patterned in a very specific manner yielding a sub-step of all possible shapes which may determine the existence of a planar device process. Further, the formation of the sacrificial layer may not be unique.

MISTIC represents device cross-sections as a set of one-dimensional distinct regions on a two-dimensional domain. For most device features this representation is suitable; however for very small devices, the characteristics of the edges becomes dominant. In these cases, this representation breaks down, and a more detailed geometry description is needed. Further, some devices cannot be easily drawn with a single cross section therefore a three-dimensional device builder is also desirable.

Finally, the factors that contribute to the figure of merit in each step and their relative significance should be investigated more comprehensively to determine improved figures of merit. Some of this work is currently being investigated [10, 11].

Despite these pitfalls, the compiler implementation presented in this paper includes the fundamental steps required for the assembly of a process flow; hence it is a valuable tool for the rapid generation of device processes consistent with good design outlines satisfying specific requirements. Further, the system provides a unified framework for the representation of devices, process steps, and flows.

VII. Conclusion

This paper gives a basic overview of the MISTIC automatic process compiler framework. MISTIC takes as input a cross-section of a device structure represented as a collection of distinct one-dimensional regions and generates a set of process flows for the device for a specific fabrication facility. The compiler includes The framework contains the basic compiler and several auxiliary modules, e.g., a device builder, a process viewer, and a database editor forming a self-contained process design environment.

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