Problem 1: (Section 10.1) Consider a logic-circuit family that has a maximum low-frequency voltage gain of 50 V/V. The circuits use a 3.3 V power supply, \( V_{OL} \) and \( V_{OH} \) are the ideal values, and \( V_{th} = 0.4V_{DD} \).

(a) What are the best possible values of \( V_{IL} \) and \( V_{IH} \)? \[ V_{IL} = 1.294 \text{ V}, V_{IH} = 1.360 \text{ V} \]

(b) What are the corresponding noise margins? \[ \text{NM}_H = 1.940 \text{ V}, \text{NM}_L = 1.294 \text{ V} \]

(c) If the actual noise margins were only 7/10 of the values in (b), what would the actual values of \( V_{IL} \) and \( V_{IH} \) be? \[ V_{IL} = 0.906 \text{ V}, V_{IH} = 1.942 \text{ V} \]

Problem 2: (Section 10.1) Consider a logic circuit family with an inverter that has a propagation delay of \( t_P = 1.2 \text{ ns} \), and the delay can be modeled with a fixed current charging or discharging the output capacitance.

(a) If the current for charging the output capacitance is half as large as the current for discharging the output capacitance, what do you expect \( t_{PLH} \) and \( t_{PHL} \) to be? \[ t_{PLH} = 1.6 \text{ ns}, t_{PHL} = 0.8 \text{ ns} \]

(b) When an additional capacitance of 1 pF is added to the output, the propagation delays increase by 70%. What was the original output capacitance? \[ 1.43 \text{ pF} \]

(c) Without the additional capacitance from (b), the load capacitance can be divided into two parts: one part from the next stage being driven by the inverter, and another part from the intrinsic parasitic capacitances of the inverter itself. When the next stage is removed from the inverter output, the propagation delays decrease by 40% (from the original configuration without the additional capacitance from (b)). What are the values of the two parts of the load capacitance? \[ C_{next} = 0.57 \text{ pF}, C_{par} = 0.86 \text{ pF} \]

Problem 3: (Section 10.1) Sedra and Smith: Chapter 10, problem 10.7. \[ (a) f_3 = 0.66, \frac{P_{DP1\lambda}}{P_{DP2\lambda}} = 0.435 \ (b) t_{\lambda} = 0.436, \frac{P_{DP1\lambda}}{P_{DP1\lambda}} = 0.435 \]

Problem 4: (Section 10.1) Sedra and Smith: Chapter 10, problem 10.11. \[ 45 \text{ pJ} \]

Problem 5: (Section 4.10) Sedra and Smith: Chapter 4, problem 4.105. \[ (a) r_{DS,n} = r_{DS,p} = 2.4 \text{ k}\Omega \ (b) I_{sink} = I_{source} = 41.4 \text{ \mu A} \ (c) V_{IL} = V_{IH} = NM_L = NM_H = 1.3 \text{ V} \]
Problem 6: (Section 4.10) Sedra and Smith: Chapter 4, problem 4.113. \( W_n = 3 \mu m, W_p = 6 \mu m \)

Problem 7: (Section 10.2) Sedra and Smith: Chapter 10, problem 10.22. \( P_{static} = 1.63 \ W, C_{gate} = 3.5 \ fF \)

Problem 8: (Section 10.3) Sedra and Smith: Chapter 10, problem 10.25.

Problem 9: (Section 10.3) Sedra and Smith: Chapter 10, problem 10.29.

Problem 10: (Section 10.3) For the gate designed in the previous question, what should the ratio be between the nMOS and pMOS W/L ratios to obtain equal drive strengths in the pull-up and pull-down networks, assuming that \( \mu_n = 2 \mu_p \)?