Assignment #4
Topics: S.S. Analysis, Diff. Pairs with Active Loads, Frequency Effects
Due Date: Sept. 26, 2008

Problem 1: (Section 6.9) Consider the amplifier in Fig. 1. The power supply voltage is \( V_{DD} = 5 \) V and \( V_{BIAS} \) has been chosen to keep \( M_1 \) in saturation; for NMOS devices \( \mu_n C_{ox} = 100 \mu A/V^2 \), for PMOS devices \( \mu_p C_{ox} = 50 \mu A/V^2 \), \( |V_t| = 1 \) V for all devices, and the sizing of the transistors is as follows: \( (W/L)_1 = 8 \mu m/2 \mu m, (W/L)_2 = 4 \mu m/2 \mu m, \) and \( (W/L)_3 = 4 \mu m/2 \mu m \). You may ignore channel length modulation for \( M_1 \) and \( M_3 \), but you must consider it for \( M_2 \) with \( V'_A = 1.5 \) V/\( \mu m \). You may ignore the body effect.

(a) What is the small signal input resistance, \( r_{in} \)? [\( \infty \) \( \Omega \)]
(b) What is the small signal output resistance, \( r_{out} \)? [30 k\( \Omega \)]
(c) What is the small signal voltage gain, \( v_{out}/v_{sig} \)? [-8.03 V/V]

Problem 2: (Section 6.7) Consider the amplifier in Fig. 2. The power supply voltage is \( V_{DD} = 5 \) V and \( V_{BIAS} \) has been chosen to keep \( M_1 \) in saturation; for NMOS devices \( \mu_n C_{ox} = 100 \mu A/V^2 \), for PMOS devices \( \mu_p C_{ox} = 50 \mu A/V^2 \), \( |V_t| = 1 \) V for all devices, and the sizing of the transistors is as follows: \( (W/L)_1 = 8 \mu m/2 \mu m, (W/L)_2 = 4 \mu m/2 \mu m, (W/L)_3 = 4 \mu m/2 \mu m \). You may ignore channel length modulation for \( M_1 \) and \( M_3 \), but you must consider it for \( M_2 \) with \( V'_A = 1.5 \) V/\( \mu m \). You may ignore the body effect.

(a) What is the small signal input resistance, \( r_{in} \)? [3.53 k\( \Omega \)]

Figure 1: Common source amplifier with source degeneration.
(b) What is the small signal output resistance, $r_{\text{out}}$? \[30 \text{ k}\Omega\]

(c) What is the small signal voltage gain, $v_{\text{out}}/v_{\text{sig}}$? \[8.37 \text{ V/V}\]

**Problem 3:** *(Section 6.10)* Consider the amplifier in Fig. 3. The power supply voltage is $V_{DD} = 5 \text{ V}$ and $V_{BIAS}$ has been chosen to keep $M_1$ in saturation; for NMOS devices $\mu_n C_{ox} = 100 \mu\text{A}/\text{V}^2$, for PMOS devices $\mu_p C_{ox} = 50 \mu\text{A}/\text{V}^2$, $|V_t| = 1 \text{ V}$ for all devices, and the sizing of the transistors is as follows: $(W/L)_1 = 8 \mu\text{m}/2\mu\text{m}$, $(W/L)_2 = 4 \mu\text{m}/2\mu\text{m}$, and $(W/L)_3 = 4 \mu\text{m}/2\mu\text{m}$. You may ignore channel length modulation for $M_1$ and $M_3$, but you must consider it for $M_2$ with $V_A' = 1.5 \text{ V/\mu m}$. You may ignore the body effect.

(a) What is the small signal input resistance, $r_{\text{in}}$? \[\infty \Omega\]

(b) What is the small signal output resistance, $r_{\text{out}}$? \[189 \Omega\]

(c) What is the small signal voltage gain, $v_{\text{out}}/v_{\text{sig}}$? \[0.054 \text{ V/V}\]

**Problem 4:** *(Section 7.5)* Sedra and Smith: Chapter 7, problem 7.62. \[I = 0.2 \text{ mA}\]

**Problem 5:** *(Section 7.5)* Consider the MOS differential amplifier shown in Fig. 7.28(a) of the text, where all transistors have $k'W/L = 0.2 \text{ mA/V}^2$ and $|V_A| = 20 \text{ V}$. Assume $V_{DD} = 5 \text{ V}$ and the pair has been biased with $I = 400 \mu\text{A}$, with the current source implemented by a current mirror with transistor parameters as specified above.

(a) What is the differential gain? \[14 \text{ V/V}\]

(b) What is the common mode gain? \[0.071 \text{ V/V}\]

(c) What is the common mode rejection ratio (CMRR) in dB? \[45.9 \text{ dB}\]
Problem 6: (Section 7.7) Consider the circuit in Fig. 7.40 of the text, with device geometries (in $\mu$m) as specified in Table 1. Let $I_{REF} = 225 \mu A, |V_i| = 0.75 V$ for all devices, $k'_n = 180 \mu A/V^2, k'_p = 60 \mu A/V^2, |V_A| = 9 V$ for all devices, and $V_{DD} = V_{SS} = 1.5 V$.

(a) Find the width of $Q_6, W$, that will avoid systematic offset voltage. \[20 \mu m\]

(b) Find the gain of the first stage, $A_1$. \[-36 \text{ V/V}\]

(c) Find the gain of the second stage, $A_2$. \[-36 \text{ V/V}\]

(d) Find the overall gain of the circuit. \[-1296 \text{ V/V}\]

Problem 7: (Appendix E) Consider the circuit shown in Fig. PE.1 of the text (on page E-6).

(a) What is the transfer function $V_o(s)/V_i(s)$?

(b) Assuming $C_1 = C_2 = 0.5 \mu F$ and $R = 100 \text{ k}\Omega$, sketch the bode plots for the magnitude and phase of the transfer functions, labeling the pole and zero frequencies.

Problem 8: (Appendix E) Sedra and Smith: Appendix E, problem E.9.

Problem 9: (Appendix E) Sedra and Smith: Appendix E, problem E.10. [magnitude = 1.0049, phase = -95.1°]