Midterm Exam I

Oct. 8, 8:35-9:25am

Name: ____________________________

(40 points total)

PROBLEM 1: Consider the circuit shown in Fig. 1, where the dotted line encloses the small signal model for an amplifier and we are interested in the voltage gain $v_{out}/v_{sig}$. The component values are as follows: $R_{sig} = 100 \, \Omega$, $C_{in} = 10 \, \text{pF}$, $R_{out} = 100 \, \Omega$, $C_L = 1 \, \text{nF}$, and $A = 1000$. [11 points]

![Amplifier Model Diagram](image)

(a) What is the transfer function $v_{out}(s)/v_{sig}(s)$? [3]
(b) Sketch the magnitude and phase response bode plots for this transfer function on the plots provided in Fig. 2. [6]
(c) We would like to increase the 3-dB frequency, but the amplifier parameters ($C_{in}$ and $R_{out}$) are fixed. If you can adjust either $R_{sig}$ or $C_L$ by a factor of 10 (increase or decrease), which would you choose, and why? [2]

\[
\begin{align*}
V_{in} &= V_{sig} \cdot \frac{1}{sC_{in}} \cdot \frac{sC_{in}}{\frac{1}{sC_{in}} + V_{2_{sig}}} = V_{sig} \cdot \frac{1}{1 + sR_{sig} \cdot C_{in}} \\
V_{out} &= A \cdot V_{in} \cdot \frac{1}{sC_{L}} \cdot \frac{sC_{L}}{\frac{1}{sC_{L}} + \frac{1}{R_{out}}} = A \cdot V_{in} \cdot \frac{1}{1 + sR_{out} \cdot C_{L}}
\end{align*}
\]
PROBLEM 1 (cont'd)

(b) 

\[ |A(s)| \quad \text{(dB)} \]

\[ \angle A(s) \quad \text{(°)} \]

Figure 2: Bode plots for Problem 1.

6) (cont'd) \[ \frac{V_{out}}{V_{sy}} = \frac{A}{(1 + sR_yC_r)(1 + sR_wC_L)} \]

DC gain: \[ A = 100 \Rightarrow 60 \text{ dB} \]

Poles: \[ \omega_p1 = \frac{1}{R_yC_r} = \frac{1}{1E2 \cdot 1E-11} = 1E9 \text{ rad/s} \]
\[ \omega_p2 = \frac{1}{R_wC_L} = \frac{1}{1E2 \cdot 1E-9} = 1E7 \text{ rad/s} \]

(c) Dominant pole is formed by \( R_w \) and \( C_L \), so we should reduce \( C_L \).
PROBLEM 2: Consider the amplifier shown in Fig. 3, where \( \frac{W}{L}_1 = 10 \) and \( \frac{W}{L}_2 = 5 \). Assume that \( I_{BIAS} \) and \( V_{BIAS} \) have been chosen so that all transistors are biased in the saturation region with \( I_D = 25 \) mA. For NMOS devices \( \mu_n C_{ox} = 200 \) \( \mu A/V^2 \), and for PMOS devices \( \mu_p C_{ox} = 100 \) \( \mu A/V^2 \). You may neglect channel length modulation for all devices, and \( R_{sig} = 50 \) \( \Omega \) and \( C_B = \infty \). [12 points]

![Amplifier Diagram](image)

Figure 3: Amplifier for Problem 2.

(a) Calculate the \( g_m \) values for \( M_1 \) and \( M_2 \). [4]

(b) What is the small signal gain of the amplifier, \( v_{out}/v_{sig} \)? [8]

\[ g_{m1} = \sqrt{2\mu_n \cdot C_{ox} \cdot W/L \cdot I_D} = \sqrt{2 \cdot 200 \cdot 10^{-6} \cdot 10 \cdot 25 \cdot 10^{-3}} = 10 \cdot 10^{-3} = 10 \text{ mA/V} \]

\[ g_{m2} = \sqrt{2\mu_p \cdot C_{ox} \cdot W/L \cdot I_D} = \sqrt{2 \cdot 100 \cdot 10^{-6} \cdot 5 \cdot 25 \cdot 10^{-3}} = 5 \cdot 10^{-3} = 5 \text{ mA/V} \]

(b) Draw S-S models:
PROBLEM 2 (cont’d)

KCL @ A: \[
\frac{V_{in} - (-V_{gs1})}{R_{sig}} + g_{m1} V_{gs1} = 0
\]
\[
V_{in} + V_{gs1} + g_{m1} R_{sig} V_{gs1} = 0
\]
\[
V_{in} = -V_{gs1} \left(1 + g_{m1} R_{sig}\right) \quad (1)
\]

KCL @ B: \[
g_{m1} V_{gs1} + g_{m2} V_{out} = 0
\]
\[
V_{out} = -\frac{g_{m1}}{g_{m2}} V_{gs1} \quad (2)
\]

Combine (1) & (2): \[
\frac{V_{out}}{V_{in}} = -\frac{g_{m1}}{g_{m2}} \left(1 + g_{m1} R_{sig}\right)
\]
\[
= \frac{g_{m1}}{g_{m2} \left(1 + g_{m1} R_{sig}\right)}
\]
\[
= \frac{10E-3}{5E-3 \left(1 + 10E-3 \cdot 50\right)}
\]
\[
= \frac{2}{1 \left(1.5\right)}
\]
\[
= 1.33 \quad \text{(Okay)}
\]
Problem 3: Consider the differential pair shown in Fig. 4. The power supply voltage is $V_{DD} = 5$ V, the transistors are sized with $(\frac{W}{L})_{1,3} = 5$ and $(\frac{W}{L})_{3,4} = 10$, and for all transistors $\mu_n C_{ox} = 200 \mu A/V^2$ and $V_t = 1$ V. You may ignore channel length modulation in this problem. [15 points]

![Differential pair](image)

Figure 4: Differential pair for Problem 3.

(a) Assuming all transistors are in saturation, calculate $V_{GS1}$ and $V_{GS3}$. [4]

(b) Assuming that no differential input has been applied ($V_{in+} = V_{in-}$), what is the minimum allowable value of $V_{out+} = V_{out-}$ to keep all transistors in saturation (assume that $V_{in+} = V_{in-}$ can be set to whatever bias voltage is necessary)? [4]

(c) Using your answer from part (b), what is the maximum allowable value for the $R_D$ resistors? [3]

(d) What is the corresponding gain of the differential pair for this configuration? [4]

\[\begin{align*}
\text{(a) for } M_1: \quad I_D &= \frac{M_0 \mu_c (W/L)}{2} (V_{GS1} - V_t)^2 = \sqrt{\frac{2\cdot I_D}{\sqrt{M_0 \mu_c (W/L)}}} + V_t \\
&= \sqrt{\frac{1\cdot 10^{-3}}{2\cdot 10^{-8}}} + 1 \\
&= 1 + 1 = 2 \ V.
\end{align*}\]

\[\begin{align*}
\text{for } M_3: \quad V_{GS3} &= \sqrt{\frac{2\cdot 10^{-3}}{2\cdot 10^{-8}}} + 1 \\
&= 1 + 1 \\
&= 2 \ V.
\end{align*}\]
Problem 3 (cont'd)

(b) Need to keep $M_3 \neq M_1/M_2$ in saturation.

- Need $V_{DS_{min}}$ for $M_1/M_2 = V_{GS_1} - V_t = 2 - 1 = 1V$.
- Need $V_{DS_{min}}$ for $M_3 = V_{GS_3} - V_t = 2 - 1 = 1V$.
- Start at $0V$.

\[ V_{out_{min}} = V_{DS_{min}} + V_{DS_{min}} = 1 + 1 = 2V. \]

(c) \[ \begin{align*}
   &5V \\
   &\downarrow R_p \\
   &\downarrow V_{out} \\
   &\downarrow I
\end{align*} \]

From ohm's law: $V_{out} = V_{DD} - I \cdot R_p$

\[ 2 = 5 - (0.5E-3) \cdot R_p \]

\[ R_p = 6E3 = 6k\Omega \]

(d) From notes, resistively loaded diff pair with diff outputs:

\[ A_D = g_{m1} \cdot R_p \]

\[ g_{m1} = \frac{\sqrt{2} \cdot m \cdot V_t \cdot I_D}{L} \]

\[ = 1E-3 \cdot 6E3 \]

\[ = 6 \]

\[ A_D = 1 \text{ mA/V} \]
PROBLEM 4: Where would you rather be right now? [2 points]

- On a beach in the tropics, sipping a cocktail. *(boring!)*
- On top of Mt. Everest. *(too cold!)*
- In Belgium watching World Cup cyclocross racing. *AWESOME!!!*
- Nowhere, this midterm is the most darn fun I have ever had. *(wishful thinking!)*