Problem 1: A feedback amplifier employing series-series feedback is shown in Fig. 1, where the feedback network is contained within the dotted box. The component values are $R_s = 1$ kΩ, $R_i = 7$ kΩ, $R_o = 3$ kΩ and $R_L = 6$ kΩ, and $G_m = 0.1$ A/V for the transconductance amplifier. [16 points]

(a) Calculate the relevant 2-port network parameters for the feedback network. [7]

(b) Calculate the open-loop gain of the amplifier ($I_{out}/V_s$) with the loading of the feedback network, source, and load included. [4]

(c) Use the results from the previous parts to calculate the closed-loop with feedback, $A_f = I_{out}/V_s$, as denoted in Fig. 1. [3]

(d) If $G_m$ increases by 5%, by approximately how much (as a percentage) does the closed-loop gain ($A_f$) change? [2]

Figure 1: Series-Series feedback amplifier.
Problem 1 (cont’d)
Problem 2: We are interesting in adding a feedback network to an amplifier with an open loop gain that can be expressed as 
\[ A(s) = \frac{10^6(1+s/10^{10})}{(1+s/10^6)(1+s/10^8)(1+s/10^9)}. \] 

[14 points]

(a) Sketch the bode plot for open loop gain \( A(s) \) in the space provided. [6]

(b) Is the system stable for a feedback factor of \( \beta = 10 \)? If so, what is the phase margin? [2]

(c) Suppose we wish to compensate the system (again with a feedback factor of \( \beta = 10 \)) by moving the dominant pole to a lower frequency. What is the new dominant pole frequency required to obtain a phase margin of 45°? [4]

(d) Suppose that a pole is introduced into the feedback network of the compensated system so that \( \beta = \frac{10}{1+s/10^4} \). Is the system still stable, and if so, what is the phase margin? [2]
Problem 2 (cont’d)
Problem 3: We wish to digitize a signal with a full-scale range from $V_A = 0 \text{ V}$ to $V_A = -5 \text{ V}$. We would like the quantization error of the digitized signal to be less than 2.5 mV. [10 points]

(a) How many bits are required for the ADC? [2]

(b) If the ADC is implemented using a dual-slope ADC (as shown in Fig. 2) with $R = 1 \text{ k} \Omega$, $C = 50 \text{ nF}$, and $f_{clk} = 10 \text{ MHz}$, what is the maximum possible value of $V_{\text{PEAK}}$? [4]

(c) Someone lent the ADC to Borat and he left it out in the rain. As a result, the pivot (point $N_1$) of switch $S_1$ became rusty and developed additional resistance that appears between the switch and resistor $R$. Will this affect the accuracy of the ADC, and if so, will it increase or decrease the digital read-out? [2]

(d) Assume the same premise as part (c), except the rust on switch $S_1$ has developed at contact $N_2$ and the additional resistance appears between the switch and $V_{\text{REF}}$. Will this affect the accuracy of the ADC, and if so, will it increase or decrease the digital read-out? [2]

Figure 2: Dual-slope ADC.
Problem 3 (cont’d)
Problem 4: Who was recently elected to serve a second term as Prime Minister of Canada? [2 points]

(a) Jacques-François Poutine.
(b) Sarah Palin.
(c) Stephen Harper.
(d) Who cares, the United States is the capital of the world! U-S-A, U-S-A!!