Practice Midterm II Super Exam

Nov. 14, 8:35-9:25am

Name: Vanilla Ice

(98 points total)

PROBLEM 1: A feedback amplifier employing **series-shunt** feedback is shown in Fig. 1, where the feedback network is contained within the dotted line. The component values are $R_s = 1$ kΩ, $R_{in} = 10$ kΩ and $R_L = 10$ kΩ, and $A = 10{,}000$ V/V for the basic amplifier. [**13 points**] $R_o = 100\,\Omega$

(a) What type of 2-port network parameters should be used to model the feedback network? [1]

(b) Calculate the relevant 2-port network parameters for the feedback network. [4] (V_o/V_s)

(c) Calculate the forward gain of the amplifier with the feedback network loading effects included. [4]

(d) Use the results from the previous parts to calculate the input resistance with feedback, R_{if}, as denoted in Fig. 1. [4]

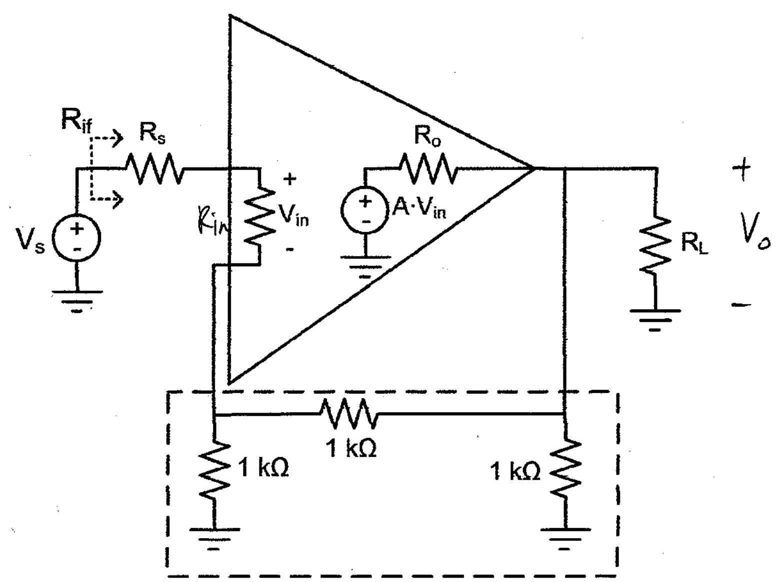
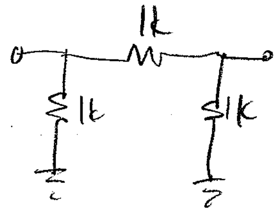


Figure 1: Series-Shunt feedback amplifier.

PROBLEM 1 (cont'd)

(a) h-parameters

(b)



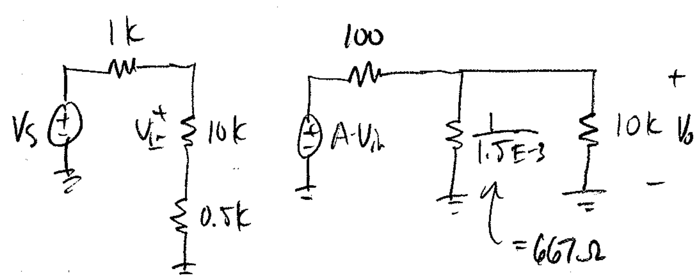
$$h_{11} = \left.\frac{V_1}{I_1}\right|_{V_2=0} = 1k \| 1k = 0.5k$$

$$h_{22} = \left.\frac{I_2}{V_2}\right|_{I_1=0} = \frac{1}{1k} + \frac{1}{2k} = 1.5E\text{-}3 \quad \text{(admittance)}$$

$$h_{12} = \left.\frac{V_1}{V_2}\right|_{I_1=0} = \frac{1k}{1k+1k} = 0.5 = \beta$$

$$h_{22} = \text{neglect}$$

(c)



$$V_o = \frac{(667 \| 1k)}{(667 \| 1k) + 100} \cdot A \cdot V_s \frac{10k}{10k + 1k + 0.5k}$$

$$\therefore \frac{V_o}{V_s} = 6957 = A_L$$

(d) $R_i = 1k + 10k + 0.5k = 11.5k$

$$R_{if} = R_i(1 + A_L \cdot \beta)$$

$$= 11.5k(1 + 6957 \cdot 0.5)$$

$$= 40.01\ M\Omega$$

Problem 2: We are interesting in adding a feedback network to an amplifier with an open loop gain that can be expressed as $A(s) = \frac{10^{12}(1+s/10^9)}{(1+s/10^6)(1+s/10^8)(1+s/10^{11})^2}$. **[16 points]**

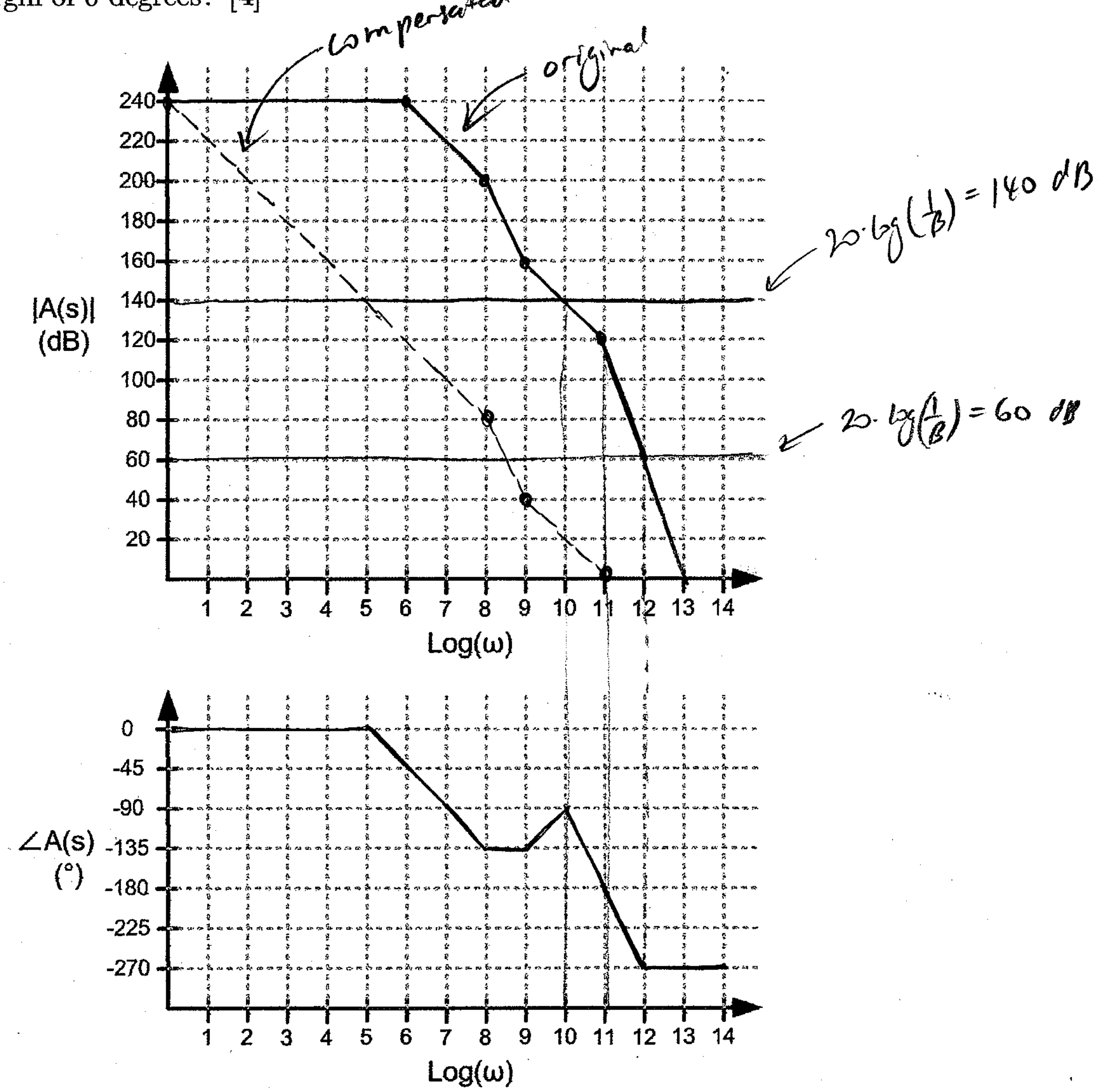
(a) Sketch the open loop bode plot $A(s)$ in the space provided. [**6**]

(b) Using this plot, will the system be stable for a feedback factor of $\beta = 10^{-3}$? If so, what is the phase margin? [**3**]

(c) Repeat part (b) for $\beta = 10^{-7}$ [**3**]

(d) Suppose we wish to compensate the system by moving the dominant pole to a lower frequency. What is the new pole frequency to obtain a phase margin of 0 degrees? [**4**]

(a)



PROBLEM 2 (cont'd)

(b) Plot $20 \log\left(\frac{1}{\beta}\right) = 60\,dB$ on bode plot.

- unstable, phase is at $-270°$ at crossing.

(c) Plot $20 \cdot \log\left(\frac{1}{\beta}\right) = 140\,dB$ on bode plot.

- stable, phase margin is $90°$ at crossing.

(d) From plot, we need the zero crossing to occur at $\omega = 10^{11}$ rad/s.

- need to shift plot down by $20 \cdot \log|A(\omega = 10^{11})| = 120\,dB$.
- first pole must occur $\frac{120\,dB}{20\,dB/dec.} = 6$ decades earlier.
- draw in dotted line for new gain curve after comp.

$\rightarrow$ Dominent pole now occurs at $\omega = 10^0 = 1$ rad/s.

Problem 3: A feedback amplifier employing **series-series** feedback is shown in Fig. 2, where the feedback network is contained within the dotted line. The component values are $R_s = 1$ kΩ, $R_{in} = 10$ kΩ and $R_L = 5$ kΩ, and $A = 100$ A/V for the basic **transconductance amplifier.** **[13 points]** $R_o = 10k$

(a) What type of 2-port network parameters should be used to model the feedback network? [1]

(b) Calculate the relevant 2-port network parameters for the feedback network. [4]

(c) Calculate the forward gain (I_o/V_s) of the amplifier with the feedback network loading effects included. [4]

(d) Use the results from the previous parts to calculate the gain with feedback, $A_f = I_o/V_s$, as denoted in Fig. ~~1~~ 2 [4] fix this

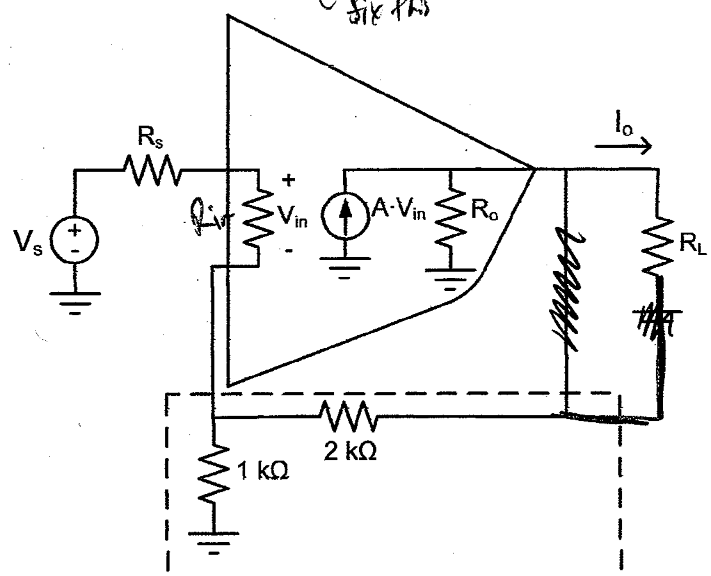
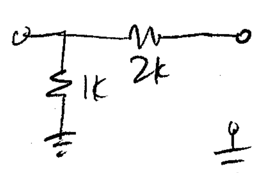


Figure 2: Series-Series feedback amplifier.

(a) z-parameters

(b)



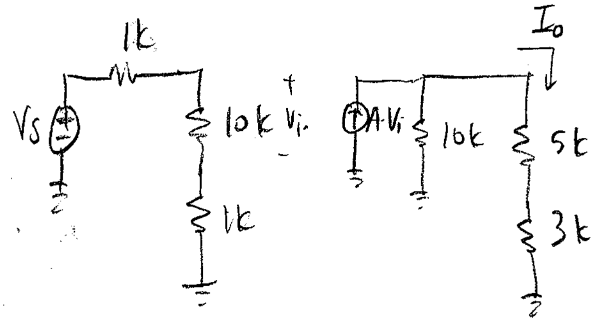
$$z_{11} = \left.\frac{V_1}{I_1}\right|_{I_2=0} = 1k$$

$$z_{22} = \left.\frac{V_2}{I_2}\right|_{I_1=0} = 3k$$

$$z_{12} = \left.\frac{V_1}{I_2}\right|_{I_1=0} = 1k = \beta$$

PROBLEM 3 (cont'd)

(c)



$$I_o = \frac{10k}{10k+8k} \cdot A \cdot V_s \cdot \frac{10k}{10k+1k+1k}$$

$$\frac{I_o}{V_s} = 46.3 = A_L$$

(d) $A_f = \frac{A_L}{1+A_L\beta} = \frac{46.3}{1+1000 \cdot 46.3} = 1.0 \times 10^{-3}$

PROBLEM 4: We wish to digitize a signal with a full-scale range from 0-5 V. We would like the quantization error of the digitized signal to be less than 0.05 V. **[10 points]**

(a) How many bits are required for the ADC? [**2**]

(b) What is the size of one LSB for the resulting ADC? [**1**]

(c) If the ADC is implemented using a dual-slope ADC (as shown in Fig. 3) with $R = 1\ \text{k}\Omega$, $C = 3.95\ \cancel{\text{p}}\,\text{nF}$, and $f_{clk} = 10$ MHz, what is the maximum possible value of V_{PEAK}? [**4**]

(d) What is the maximum sample rate for this ADC? [**3**]

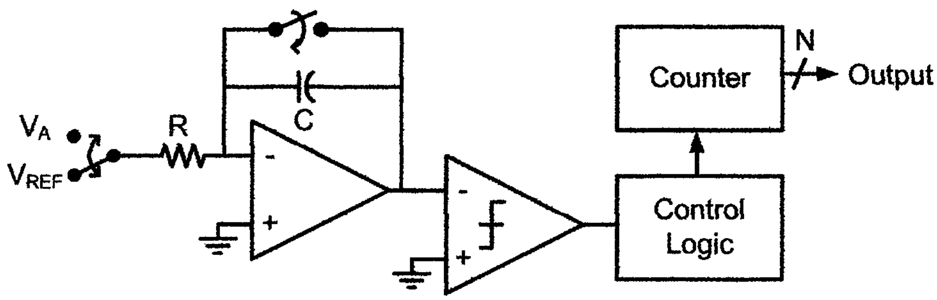


Figure 3: Dual-slope ADC.

(a) $\left(\frac{5}{2^N-1}\right)\cdot\frac{1}{2} \leq 0.05$

$2^N - 1 \geq 50$ ∴ Choose $N = 6$ bits

(b) $1\ \text{LSB} = \frac{5}{2^N-1} = 79\ \text{mV}$

(c) During charging, $I = \frac{V}{R}$ ∴ $I_{max} = \frac{V_{max}}{R} = \frac{5}{1000}$.

- cap. charges for $2^N - 1 = 63$ clock cycles, $T_1 = 63 \cdot \frac{1}{f_{CLK}} = 6.3E-6$

- for cap., $V = \frac{Q}{C} = \frac{I \cdot T_1}{C} = \frac{5}{1000} \cdot \frac{6.3E-6}{3.95E-9} = 7.97\ V. = V_{max}.$

(d) Each charge and discharge period takes $2^N = 64$ clock cycles

$f_S = \frac{f_{CLK}}{2 \cdot 64} = 78.1\ \text{kS/s}.$

PROBLEM 4 (cont'd)

Problem 5: The designer of the 3-bit binary-weighted DAC in Fig. 4 mistakenly sized resistor R_{b1} as 3 kΩ instead of the correct value of 4 kΩ. **[10 points]**

(a) What is the maximum output voltage (V_{OUT}) possible with this design? [2]

(b) Which of the 8 output levels will be in error? Specify the output levels as $S_{b3}S_{b2}S_{b1}$ where a 1 for a given switch specifies that it is in the right position. [4]

(c) What is the maximum error in the output voltage as compared to a 3-bit DAC with the correct resistor value for R_{b1}? [4]

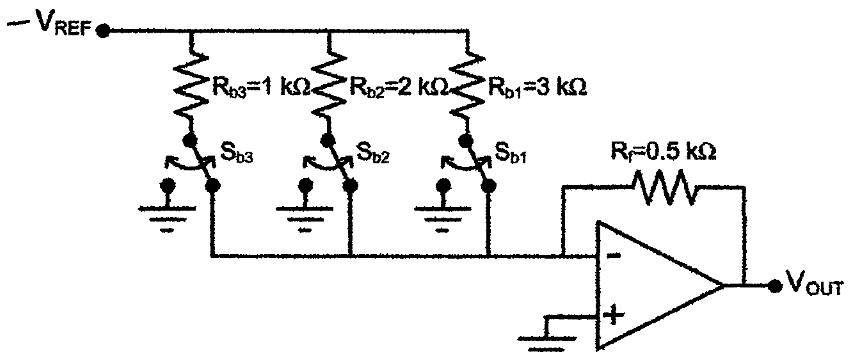


Figure 4: Binary-weighted DAC.

(a) $I_{max} = \frac{V_{REF}}{1k} + \frac{V_{REF}}{2k} + \frac{V_{REF}}{3k}$

Max. $V_{out} = V_{REF}\left(\frac{1}{1k} + \frac{1}{2k} + \frac{1}{3k}\right) \cdot 0.5k = 0.92 \cdot V_{REF}$

(b) Any output level where S_{b1} is on will be in error: 001, 011, 101, 111

(c) Error results only from LSB: ideal $= \frac{V_{REF}}{4k} \cdot 0.5k = 0.125\, V_{REF}$

actual $= \frac{V_{REF}}{3k} \cdot 0.5k = 0.167\, V_{REF}$

$\therefore$ Error $= 0.042\, V_{REF}$

PROBLEM 6: We wish to design a CMOS logic gate to implement the function $\overline{Y} = (A+B)\cdot C$. **[12 points]**

(a) Draw the logic gate. [4]

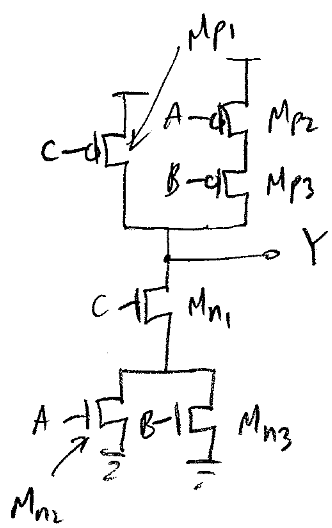
(b) With the assumption that $\mu_n = 6\times10^{-2}$ m^2/Vs and $\mu_p = 2\times10^{-2}$ m^2/Vs, size the transistors to provide equal worst-case drive strengths for the pull-up network and pull-down network. [4]

(c) With $C_{ox} = 2\times10^{-3}$ F/m^2, what would the dynamic power consumption be of the circuit driving the A input at 10 MHz? [4]

Assume $L = 1\ \mu m$ for all devices.

Assume $V_{DD} = 5V$.

(a)



(b) $M_{n_1} = 2$, $M_{n_2} = 2$, $M_{n_3} = 2$ (worst case drive = 1)

$M_{p_1} = 3$, $M_{p_2} = 6$, $M_{p_3} = 6$ (worst case drive = 1)

(c) Loading from gates of A: $C_{in} = (W_{p_2}\cdot L_{p_2})\cdot C_{ox} + (W_{n_2}\cdot L_{n_2})C_{ox}$

$= 2E\text{-}3\,(6E\text{-}12 + 2E\text{-}12)$

$= 16E\text{-}15 = 16$ fF

$\therefore P_D = C V_{DD}^2 \cdot f_{clk} = 16E\text{-}15\,(25)\cdot 10E6 = 4E\text{-}6 = 4\ \mu W.$

Problem 7: The same designer who provided us with the ill-fated modified CMOS inverter that we analyzed in class has come up with another inverter architecture, shown in Fig. 5. Despite our skepticism, we have decided to review his latest chef-d'oeuvre. Assume that $V_{DD} = 5$ V for this process, and the device threshold voltages are $V_{tn} = V_{tp} = 1$ V. [**12 points**]

(a) Draw the voltage transfer characteristics (VTC) for this gate in the space provided, and indicate which operating region each transistor will be in at different segments of the curve (hint: there should be 5 distinct segments). [8]

(b) Find the threshold voltage for the gate, under the assumption that both devices are in saturation at this point. [4]

devices are sized for equal drive.

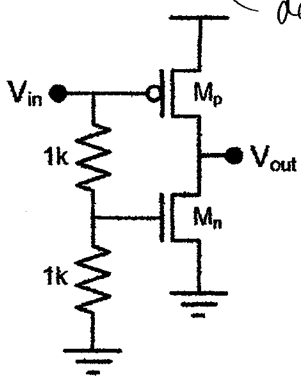
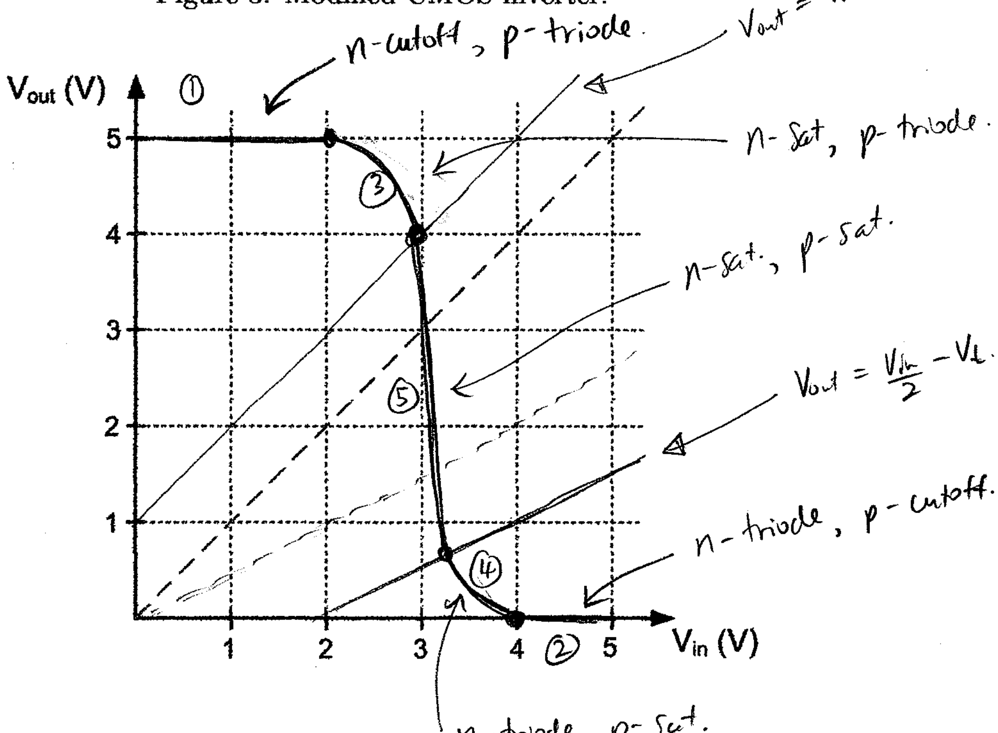


Figure 5: Modified CMOS inverter.



Problem 7 (cont'd)

(a) First draw in regions ①, ② where one device is in cutoff.

- Find where p enters sat.: $V_{DS_p} \geq (V_{GS_p} - V_t)$

$$\cancel{V_{DD}} - V_{out} = \cancel{V_{DD}} - V_{in} - V_t.$$

$$V_{out} = V_{in} + V_t.$$

(plot this line on curve and note ③)

- Find where n enters sat.: $V_{DS_n} \geq (V_{GS_n} - V_t)$

$$V_{out} = \frac{V_{in}}{2} - V_t.$$

(plot this line and note ④)

- Final segment is where both devices are in sat. (⑤)

(b) Express equality between drain currents:

$$(V_{GS_n} - V_t)^2 = (V_{GS_p} - V_t)^2$$

$$\frac{V_{in}}{2} - V_t = V_{DD} - V_{in} - V_t.$$

$$1.5 \cdot V_{in} = 5$$

$$\therefore V_{in} = \frac{5}{1.5} = 3.3\text{ V}$$

- this makes sense based on our sketch.

PROBLEM 8: Consider a standard CMOS inverter with power supply $V_{DD} = 5$ V, implemented in a process with $V_{tp} = V_{tn} = 1$ V, $\mu_n = 5 \times 10^{-2}$ m²/Vs, $\mu_p = 2.5 \times 10^{-2}$ m²/Vs, and $C_{ox} = 2 \times 10^{-3}$ F/m². The devices are sized with $\left(\frac{W}{L}\right)_n = 1$ and $\left(\frac{W}{L}\right)_n = 2$. **[12 points]**

(a) What is the low noise margin (NM_L) for this inverter? **[1]**

(b) What is the propagation delay for the inverter, assuming it drives a load of $C = 10$ fF? **[2]**

(c) What is the maximum clock speed for a logic chain consisting of ~~a~~ ten inverters in this technology? **[2]** Max. capacity at ~~700 MHz~~

(d) What is the total power consumption of a chip with 100,000 gates, each with a probability of switching of 0.25 on any given clock cycle (assume the inverter being discussed is representative of all of the gates)? **[2]** all see 10 fF load.

(e) We now wish to scale back the power supply voltage to reduce the power consumption, how much can we reduce V_{DD} and still maintain a clock speed greater than ~~400 MHz~~ 1.8 GHz? **[3]**

(f) How much will this extend the battery life? **[2]**

(a) $NM_L = \frac{1}{8}(3 \cdot V_{DD} + 2 \cdot V_t) = \frac{1}{8}(15 + 2) = 2.125\ V$

(b) $t_p = \dfrac{1.6 \cdot 10E{-}15}{5E{-}2 \cdot 2E{-}3 \cdot 1 \cdot 5} = 3.2E{-}11 = 32\ ps.$

(c) $f_{clk_{max}} = \dfrac{1}{t_p \cdot 10} = 3.125\ GHz.$

(d) $P = 3.125E9 \cdot (5V)^2 \cdot 10E{-}15 \cdot 0.25 \cdot 100{,}000$
$= 19.5\ W.$

(e) $f_{clk} = 1.8\ GHz = \dfrac{1}{10 \cdot t_p} = \dfrac{1}{10 \cdot 1.6 \cdot 10E{-}15} \cdot 5E{-}2 \cdot 2E{-}3 \cdot V_{DD}.$

$\therefore V_{DD} = 2.88\ V$

(f) Power is reduced to $\left(\frac{2.88}{5}\right)^2 = 0.33$ of what it was

$\therefore$ Battery Life $= \dfrac{\text{Energy}}{\text{Power}} = \dfrac{1}{0.33} = 3.03$

$\therefore$ Life is extended to 3 x what it was.