Midterm Exam II

Nov. 14, 8:35-9:25am

Name: Mili Vanilli

(40 points total)

PROBLEM 1: A feedback amplifier employing series-shunt feedback is shown in Fig. 1, where the feedback network is contained within the dotted line. The component values are $R_s = 1 \, \text{k}\Omega$, $R_m = 10 \, \text{k}\Omega$, $R_o = 100 \, \Omega$ and $R_f = 1 \, \text{k}\Omega$, and $A = 1,000 \, \text{V/V}$ for the basic amplifier. [14 points]

(a) What type of 2-port network parameters should be used to model the feedback network? [1]

(b) Calculate the relevant 2-port network parameters for the feedback network. [6]

(c) Calculate the forward gain of the amplifier with the feedback network loading effects included. [4]

(d) Use the results from the previous parts to calculate the gain with feedback, $A_f = V_{out}/V_s$, as denoted in Fig. 1. [3]

Figure 1: Series-Shunt feedback amplifier.
PROBLEM 1 (cont’d)

(a) h-parameters

(b) \( h_{11} = \left. V_i \right|_{I_2=0} = 1k + 1k || 1k = 1.5k \)

\( h_{22} = \left. V_2 \right|_{I_1=0} = 2k \)

\( h_{21} = \text{neglect} \)

\( h_{12} = \left. \frac{V_1}{V_2} \right|_{I_1=0} = \frac{1k}{1k+1k} = 0.5 = \beta \)

(c) \( A_L = \frac{V_{out}}{V_i} = \frac{2k || 1k}{10k+10k+1.5k} = 698.7 \)

(d) \( A_f = \frac{A_L}{1 + A_L \beta} = \frac{696}{1 + 696 \cdot 0.5} = 1.994 \)
Problem 2: We are interesting in adding a feedback network to an amplifier with an open loop gain that can be expressed as $A(s) = \frac{10^6}{(1+s/10^5)(1+s/10^8)(1+s/10^{10})^2}$.

12 points]

(a) Sketch the bode plot for open loop gain $A(s)$ in the space provided. [6]

(b) What is the phase margin for a feedback factor of $\beta = 1$? Is the system stable in this configuration? [2]

(c) Suppose we wish to compensate the system (again with a feedback factor of $\beta = 1$) by moving the dominant pole to a lower frequency. What is the new dominant pole frequency to obtain a phase margin of 45 degrees? [4]
PROBLEM 2 (cont’d)

(a) done.
(b) Phase Margin = -90°, unstable
(c) From plot, \( \omega_p = 10^2 \text{ rad/s} \).
Problem 3: Consider a standard CMOS inverter with power supply $V_{DD} = 5$ V, implemented in a process with $V_{tp} = V_{tn} = 1$ V, $\mu_n = 5 \times 10^{-2}$ m$^2$/Vs, $\mu_p = 2.5 \times 10^{-2}$ m$^2$/Vs, and $C_{ox} = 2 \times 10^{-3}$ F/m$^2$. [12 points]

(a) If the NMOS device is sized with $W/L = 2$, how should the PMOS device be sized to equalize the inverter's pull-up and pull-down drive strengths? [2]

(b) If one inverter has a propagation delay of 32 ps, what is the maximum clock speed for a logic chain consisting of twenty inverters in this technology? [2]

(c) What is the dynamic power consumption of one inverter driving a 10 fF load at 500 MHz? [3]

(d) Suppose that a glitch in the system causes the input to the inverter to be fixed at $V_{in} = 2.5$ V. What will the static power consumption of the inverter be under these conditions? [5]

(a) For pmos, $\frac{W}{L} = 4$ to compensate for $\mu_p$.  

(b) $f_{ck} = \frac{1}{2 \cdot 32 \cdot 10^{-12}} = 1.56$ GHz

(c) $P_d = C \cdot V_{DD}^2 \cdot f_{ck} = 10E-15 \cdot (5)^2 \cdot 500E6 = 1.25E-4 = 125 \mu W$

(d) Find what: $i_n = i_p = \frac{\mu_n \cdot C_{ox} \cdot (V / L)_n \cdot (V_{in} - V_t)^2}{2} = \frac{5E-2 \cdot 2E-3 \cdot 2 \cdot (2.5 - 1)^2}{2} = 225 \mu A$

$$P_d = I \cdot V_{DD} = 225 \mu A \cdot 5V = 1.125 \text{ mW}$$
PROBLEM 3 (cont’d)
PROBLEM 4: Napolean is having some problems with his time machine (see Fig. 2), and he thinks it is because his A/D converter isn't fast enough. What A/D converter architecture would you recommend for him? [2 points]

Figure 2: Napolean and his sweet time machine.

Napolean should use a flash A/D. They are way fast and totally sweet.