Laboratory 2: Differential Pairs

To be performed during Week 4 (Sept. 15-19)
Due Week 5 (Sept. 22-26)

1 Pre-Lab

This Pre-Lab should be completed before attending your regular lab section. The Lab TA will need to see your completed Pre-Lab and check it off at the start of the lab session before you can begin taking your measurements.

Read Sections 7.1, 7.2, and 7.4.1 in the text, which cover the design and analysis of MOSFET differential pairs. For this lab, we will build and take measurements on the differential pair shown in Fig. 1. In the following calculations we will determine how we expect the differential pair to operate, based on the theory covered in the lectures and the text. For all calculations, use the MOSFET parameters given in Table 1 which are representative values for the 2N7000 transistors we will be using in this lab. You may ignore channel length modulation ($V_{A}$) for all of the calculations except where noted.

1. For the differential pair shown in Fig. 1, assume that $V_{in+} = V_{in-} = 0$ V and calculate $V_{GS1} = V_{GS2}$ for $I_{bias} = 80$ mA (remember that $I_{bias}$ will split equally between $M_1$ and $M_2$).

2. Using the value of $V_{GS}$ calculated above, find the value of $R_{SS}$ required to obtain $I_{bias} = 80$ mA.

3. Calculate the value of $V_{DS}$ for $M_1$ and $M_2$. Are the two devices in saturation?

4. Assuming a single-ended output (as shown in Fig. 1), calculate the common mode gain ($A_{cm}$) for the differential pair.

5. Again assuming a single-ended output, calculate the differential mode gain for the differential pair.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_t$</td>
<td>2.1 V</td>
</tr>
<tr>
<td>$\mu_n C_{ox} (W/L)$</td>
<td>180 mA/V²</td>
</tr>
<tr>
<td>$V_A$</td>
<td>50 V</td>
</tr>
</tbody>
</table>

Table 1: Approximate NMOS transistor parameters for hand calculations.
6. Now assume that $R_{SS}$ has been replaced by a current mirror biased with 80 mA, calculate the new values of $A_{cm}$ and $A_d$. You will need to take into account the finite output impedance of the current mirror using the early voltage.

7. By what factor is the common mode rejection ratio (CMRR) improved by using a current mirror instead of a resistor for biasing?

2 Measurements

The parts that will be used to build the current mirror circuit are listed in Table 2, and can be obtained from the EE stores (along with bread boards and wiring equipment). We will use 2N7000 N-Channel field effect transistors during this lab (see data sheet at http://www.ece.utah.edu/~ccharles/ece3110/Labs/2N7000.pdf). The pinout diagrams of the TO-92 package that we will be using are shown in Fig. 2. MOSFETs must be handled with care to avoid damaging them; try to avoid touching the gate terminal (middle pin) as the static charge on your fingers can be enough to blow the gate capacitor. **When you place the MOSFETs in your bread board, take care to get the drain and source oriented properly as these discrete MOSFETs do not have interchangeable sources and drains.** If your differential pair is not working correctly, double check that you have the correct orientations.

Build the circuit shown in Fig. 3. The 200 $\Omega$ resistor is a potentiometer and the voltage source on the output is a variable DC source. Pay close attention to the proper orientation of the terminals for each transistor.
Figure 2: (a) TO-92 package pin-out, (b) N-Channel MOSFET.

<table>
<thead>
<tr>
<th>Component</th>
<th>Value/Part Number</th>
<th>Quantity</th>
</tr>
</thead>
<tbody>
<tr>
<td>MOSFET</td>
<td>2N7000</td>
<td>4</td>
</tr>
<tr>
<td>Opamp</td>
<td>741 Ω</td>
<td>1</td>
</tr>
<tr>
<td>Potentiometer</td>
<td>200 Ω</td>
<td>2</td>
</tr>
<tr>
<td>Resistor</td>
<td>100 Ω</td>
<td>3</td>
</tr>
<tr>
<td>Resistor</td>
<td>50 Ω</td>
<td>1</td>
</tr>
<tr>
<td>Resistor</td>
<td>20 Ω</td>
<td>1</td>
</tr>
</tbody>
</table>

Table 2: Parts list.
2.1 DC Bias Measurements

1. Connect both $V_{in^+}$ and $V_{in^-}$ to ground (0 V), and adjust the potentiometer until $I_{bias} = 80 \text{ mA}$. Measure and record $V_{S1} = V_{S2}$, $V_{D1}$, and $V_{D2}$.

2. Power off the circuit, remove the potentiometer and measure the resistance using the multimeter. Record the total resistance (the measured potentiometer resistance plus the fixed 20 Ω resistor).

3. Remove each of the 100 Ω resistors and measure and record their resistances using the multimeter, keeping track of which value corresponds to which branch of the differential pair ($M_1$ or $M_2$).

4. Replace the potentiometer, power the circuit back on, and confirm that $I_{bias}$ is still set at 80 mA.

2.2 Common Mode Gain Measurements

1. Connect a 1-kHz sinusoidal signal of 500 mV peak-to-peak to both inputs, as shown in Fig. 4. Note that the differential amplifier from Fig. 3 has been represented as a block. **Remember to set the HP 33120A to high-impedance (“HI-Z”) load mode for the following experiments, or your signal amplitudes will be off by a factor of two.**
2. Check both $V_{cm}$ and $V_{out}$ with your oscilloscope to insure that there is no distortion. If you observe distortion, reduce $V_{cm}$ until the distortion disappears. If you cannot lower the amplitude enough to get rid of the distortion completely, build a resistive voltage divider using the 500 Ω resistor and 500 Ω potentiometer to attenuate the input signal further.

3. Measure and record $V_{cm}$ and $V_{out}$. Compute and record the common mode gain, $A_{cm} = V_{out}/V_{cm}$.

### 2.3 Differential Mode Gain Measurements

To measure the differential mode gain, you will need two equal amplitude signals which are opposite in sign. The circuit shown in Fig. 5 will supply the needed signals (use a 741 or similar op amp, see data sheet at [http://www.ece.utah.edu/~ccharles/ece3110/Labs/NJM741.pdf](http://www.ece.utah.edu/~ccharles/ece3110/Labs/NJM741.pdf) for pin-out).

1. Adjust the 200 Ω potentiometer until $V_{in+}$ and $V_{in-}$ are exactly equal in magnitude. To do this, connect a 1 kHz, 500 mVpp sinusoidal signal to $V_{in}$ and one input of your oscilloscope and the 741 output into the other. Set the scope to sum the two channels (or subtract with one channel inverted; we want to observe the amplitude difference...
between the two opposite-signed signals). Adjust the range of the scope to insure that the difference signal is as close to zero as possible.

2. Now, with the two signals driving your differential amplifier, reduce $V_{in}$ until $V_{out}$ is sinusoidal (for no distortion you may need to build a resistive voltage divider to attenuate the input signal).

3. Measure and record $V_{in}$ and $V_{out}$, and compute the differential mode gain ($A_d = V_{out}/V_{in}$).

2.4 Current Mirror Bias Measurements

We will now try to improve the performance of the differential amplifier by substituting a current mirror for the resistive bias used in Fig. 3.

1. Build the circuit shown in Fig. 6, and adjust the 200 $\Omega$ potentiometer until $I_{bias} = 80$ mA.

2. Measure and record the common mode and differential mode voltage gains using the techniques described previously.

3 Analysis

Answer the following questions in the analysis section of your lab report:

1. How well do your calculated values of $R_{SS}$ and $V_{GS}$ agree with your measured values?
2. In class we discussed the upper and lower limits on the input common mode range of a differential pair, assuming biasing with a current source. For the resistively biased differential pair in Fig. 1, how would you expect the upper limit on the input common mode range to compare with a differential pair biased with a current mirror for the same $I_{bias}$ at $V_{cm} = 0$ V?

3. Based on your measurements of the drain voltages (with $V_{in+} = V_{in-} = 0$ V) and the calculated differential mode gain for the resistively biased differential pair, what is the input offset voltage for the differential pair?

4. Based on your measurements of the exact values of the 100 Ω drain resistors, how much of that input offset voltage is due to resistor mismatch and how much is due to transistor mismatch?

5. Compare the theoretical (from your pre lab calculations) and measured common mode rejection ratios (CMRR) for each of the differential pairs. Was the expected improvement seen by switching to current mirror biasing?

6. Would you expect the CMRR for the current mirror-biased differential pair to improve or deteriorate if $I_{bias}$ was reduced, and why?