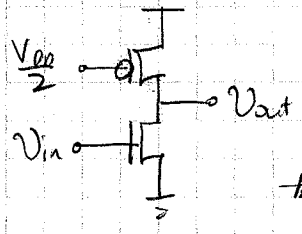


Correction: $V_{IL} = \frac{1}{8}(5V_{DD} + 2V_t)$

Nov. 5

Example: A CMOS process has $C_{ox} = 2E-3 \text{ F/m}^2$, $\mu_n = 5E-2 \text{ m}^2/\text{V}\cdot\text{s}$, $\mu_p = 2.5E-2 \text{ m}^2/\text{V}\cdot\text{s}$, and $L_{min} = 1 \mu\text{m}$ and $W_{min} = 2 \mu\text{m}$, $V_t = 1 \text{ V}$, $V_{DD} = 5 \text{ V}$.
 → design a standard CMOS inverter, and compare it's performance with that of this architecture:

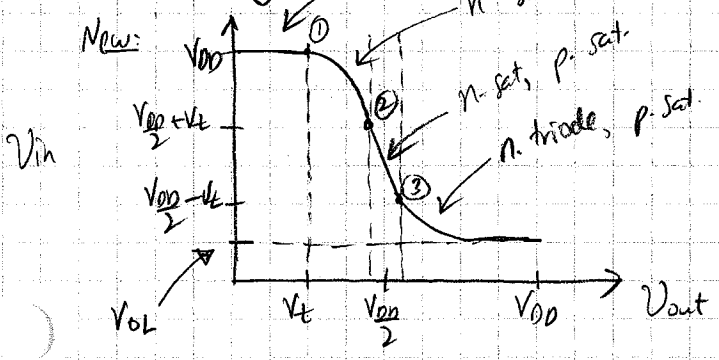


- Possible advantages?
 - easier signal routing
 - less gate capacitance to drive.

→ size CMOS with $(w/L)_n = 2 \mu\text{m}/1 \mu\text{m}$ and $(w/L)_p = 4 \mu\text{m}/1 \mu\text{m}$ to equalize drive strengths. (Same for new gate).

→ Compare behaviour:

① Noise Margin



- When $V_{in} = 0$, nmos is off, pmos pulls V_{out} up to V_{DD} .
 → $V_{OH} = V_{DD}$
- At ①, nmos turns on in saturation
- At ②, pmos enters saturation
- At ③ nmos enters triode.

→ note that $V_{OL} \neq 0$, since pmos never shuts off (stays in saturation)

→ Find V_{OL} : equate nmos, pmos currents:

$$\frac{1}{2} \left(\frac{V_{DD} - V_t}{2} \right)^2 = (V_{DD} - V_t) V_{OL} - \frac{V_{OL}^2}{2}$$

$$V_{OL}^2 - 8 \cdot V_{OL} + 2.25 = 0$$

Solve quadratic equation: $V_{OL} \approx 0.3 \text{ V}$ (other answer is above $V_{DD} = 5 \text{ V}$)

→ Since $V_{OL} < V_t$, this confirms $V_{OH} = V_{DD}$, since nmos will be fully shutoff when driven with a low logic level by the previous stage.

→ Find V_{IL} to find noise margin.

Equate currents: nmos in sat, pmos in triode.

$$\frac{1}{2} (V_i - V_t)^2 = \left(\frac{V_{DD} - V_t}{2} \right) \cdot (V_{DD} - V_o) - \frac{1}{2} (V_{DD} - V_o)^2$$

← mistake.

take deriv. w.r.t. V_i : $V_i - V_t = -\frac{dV_o}{dV_i} \left(\frac{V_{DD} - V_t}{2} \right) + \frac{1}{2} \cdot \frac{dV_o}{dV_i}$

Sub in $\frac{dV_o}{dV_i} = -1$, $V_i = V_{IH}$: $V_{IL} - 1 = 1.5 - 0.5$

$$\Rightarrow V_{IL} = 2 \text{ V}$$

$$\therefore NM_L = V_{IL} - V_{OL} = 2V - 0.3V = 1.7V$$

$$\begin{aligned} \rightarrow \text{Compare to CMOS: } NM_L &= \frac{1}{8}(3 \cdot V_{DD} + 2 \cdot V_t) \\ &= \frac{1}{8}(15 + 2) = 2.125V \end{aligned}$$

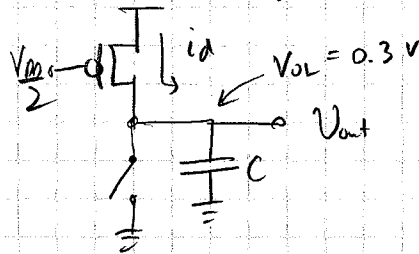
\therefore The new architecture is less robust than CMOS (lower noise margin).

② Propagation Delay

\rightarrow Let's examine a low-to-high transition.

- instantaneous input switching (high-to-low), nmos turns off immediately.

Equivalent circuit:



- t_{PLH} is time for output voltage to change by $\frac{1}{2}$ of final value.

- voltage on C needs to increase by $\frac{4.7}{2} = 2.35V$ to $V_{out} = 2.65V$.

- pmos enters triode region at $V_{out} = \frac{V_{DD}}{2} + V_t = 3.5V$, so pmos will be in saturation during this entire time \rightarrow constant current. (very nice!)

$$\begin{aligned} \rightarrow \text{Find charging current: } i_d &= \mu_p \cdot C_{ox} \left(\frac{W}{L}\right)_p \left(\frac{V_{DD}}{2} - V_t\right)^2 \\ &= \frac{2E-3 \cdot 2.5E-2 \cdot 2.4(2.5-1)^2}{2} \\ &= 225 \mu A \end{aligned}$$

Now, assume loading by next gate, find C: $C = (W \cdot L)_n \cdot C_{ox}$

$$\begin{aligned} &= 2E-6 \cdot 1E-6 \cdot 2E-3 \\ &= 4E-15 = 4 \text{ fF (small!)} \end{aligned}$$

$$\rightarrow \text{Now, } Q = CV \Rightarrow \Delta V = \frac{1}{C} \Delta Q = \frac{1}{C} \int i_d dt$$

$$\therefore 2.35V = \frac{1}{4E-15} \cdot 225E-6 \cdot t_{PLH}$$

$$t_{PLH} = 4.18E-11 \text{ s} = 41.8 \text{ ps}$$

$$\begin{aligned} \rightarrow \text{Compare to CMOS: } t_{PLH} &= \frac{1.6 \cdot C}{\mu_p \cdot C_{ox} \left(\frac{W}{L}\right)_p \cdot V_{DD}} \quad \text{where } C = [(W \cdot L)_n + (W \cdot L)_p] \cdot C_{ox} \\ &= \frac{1.6 \cdot 12E-15}{2.5E-2 \cdot 2E-3 \cdot 4.5} \\ &= 1.92E-11 = 19.2 \text{ ps} \end{aligned}$$

\therefore pmos is faster, despite added capacitance.

\rightarrow Max. clock speed for new architecture (assume fan-out of 4, 10 gate delays).

$$f_{max} = \frac{1}{t_{PLH} \cdot 40} \cong 600 \text{ MHz.}$$

③ Power Consumption (assume 100,000 gates, fanout of 4, $P(\text{switch}) = 0.3$)

→ Dynamic Power: - same as CMOS, but only cycling capacitor between $V_{OL} = 0.3 \text{ V}$ and $V_{DD} = 5 \text{ V}$.

- assume max. clock speed of 600 MHz.

$$\therefore P_D = f \cdot C \cdot (V_{OH} - V_{OL})^2 \\ = 600 \text{ E}6 \cdot 4 \cdot 4 \text{ E} - 15 \cdot (4.7)^2 \cdot 1 \text{ E} 5 \cdot 0.3 = 6.36 \text{ W}$$

→ Compare to CMOS: $P_D = 600 \text{ E}6 \cdot 4 \cdot 12 \text{ E} - 15 \cdot (5)^2 \cdot 1 \text{ E} 5 \cdot 0.3 = 21.6 \text{ W}$

∴ CMOS has higher dynamic power consumption (increased swing & loading) (Nov. 7)

→ BUT, new architecture will also have static power consumption during the low output level.

- Assume high & low occur with equal probability.

$$\therefore P_S = \frac{1}{2} \cdot I_{DL} \cdot V_{DD} \cdot \# \text{ of gates}$$

→ Midterm!
- pick a day for review?

$$\rightarrow \text{from before: } I_{DL} = I_{DIP} = \frac{M_p \cdot C_{ox} \cdot (W/L)_P}{2} \cdot (V_{DD} - V_t)^2 \\ = \frac{2.5 \text{ E} - 2 \cdot 2 \text{ E} - 3 \cdot 4}{2} \cdot (2.5 - 1)^2 \\ = 22.5 \text{ E} - 5 = 225 \mu\text{A}$$

$$\therefore P_S = \frac{1}{2} \cdot 225 \text{ E} - 6 \cdot 5 \cdot 1 \text{ E} 5 = 56.25 \text{ W (large!)}$$

→ So, total power for new architecture is $P_T = P_S + P_D = 62.6 \text{ W}$, almost three times that of CMOS ($P_T = 21.6 \text{ W}$ since there is no static power).

→ As a final comparison point, let's compare power delay products:

$$\text{New: } PDP = 5.78 \text{ E} - 4 \cdot 41.8 \text{ E} - 12 = 2.42 \text{ E} - 14 \text{ J}$$

↑
power scaled down to 1 gate.

$$\text{CMOS: } PDP = 5.4 \text{ E} - 5 \cdot 19.2 \text{ E} - 12 = 1.04 \text{ E} - 15 \text{ J}$$

∴ CMOS is way better, there is no reason to use this new process.

General CMOS Logic Gates

→ Let's look at CMOS gates for general logic functions