Q. Perform standard circuit analysis techniques (KCL or KVL) to determine the gain, etc. (e.g., input impedance, output impedance)

- By inspection,
  \[ V_{p} = V_{i} \left( \frac{R_{o}}{R_{o} + R} \right) \approx V_{i} \text{ if } R_{o} \gg R. \]

  \[ V_{o} = -g_{m} V_{i} \left( \frac{R_{o}}{R_{o} + R} \right) \]

  \[ \text{Voltage gain: } A_{V} = -g_{m} \left( \frac{R_{o}}{R_{o} + R} \right) \]

  \[ A_{V} \approx -g_{m} R_{o} \text{ if } R_{o} \gg R \text{ (often the case), } A_{V} \approx -g_{m} R_{o} \]

- This straightforward set of steps can be applied to any of the amplifier configurations to confirm their properties that were mentioned (or to any other transistor-based circuit). With experience, you will know what to neglect and be able to analyze without drawing out the S.S. model each time.

BJT Review

- BJT is similar to MOSFET in that it is used as a voltage controlled current source.
- Do a brief review although we will focus on MOSFET circuits.

Structure: NPN:

- Several modes of operation, depending on whether each p-n junction is forward or reverse biased.
- Most important is "Active" region, where BE is forward biased, BC is reverse biased.

  - Current flows in forward-biased BE junction.
  - Mostly electrons due to doping levels
  - Base is thin, so electrons reach BC junction and are swept across by E-field of reverse-biased junction.
  - Results in a small base current leading to a large collector current.
Large Signal Equation:

\[ i_C = I_S e^\frac{V_{BE}}{V_T} \]

- \( V_T \): thermal voltage, not threshold voltage
- \( I_S \): source current (related to doping, device geometry)
- \( I_B \): fixed, constant
- \( I_E = I_C + I_B \)

Plot \( I_C \) vs. \( V_{CE} \) and \( V_{BE} \):
- Finite slope leads to finite \( V_T \) resistance, \( V_T \) to include this effect:
  \[ i_C = I_S e^\frac{V_{BE}}{V_T} \left( 1 + \frac{V_{BE}}{V_A} \right) \]

Exponential characteristic:

- \( p-n \) junction becomes reverse biased
- \( p-n \) junction becomes forward biased

- Like MOSFET, we can find parameters for small signal model by taking derivatives of the above curves:
  \[ g_m = \frac{\partial I_C}{\partial V_{BE}} = \frac{I_C}{V_T} \] (linearly prop. to \( I_C \), better than MOSFET)
  \[ r_0 = \left[ \frac{\partial I_C}{\partial I_C} \right]^{-1} = \frac{V_A}{I_C} \] (early voltage)

- Unlike MOSFET, we need an additional parameter to account for the finite input resistance looking into the base:
  \[ R_{in} = \frac{V_T}{I_B} \] (\( = \frac{\partial I_B}{\partial V_{BE}} \))

Small signal model:

\[ V_T \]

\[ R_0 \]

\[ V_{BE} \]

Circuit analysis proceeds in the same manner as for MOSFETs:
- Use bias conditions to determine SS parameters
- Sub in SS model and use KCL/KVL to find gain, etc.
MOSFET vs BJT (Comparison)

- MOSFET & BJTs are very similar devices, can sometimes be used interchangeably.
- Biggest Differences:
  - MOSFETS have zero input current (through gate), BJTs have some small but definite base current.
  - BJTs have an exponential relationship of Ic vs Vce, MOSFETS have a square law relationship of Ic vs. Vgs (ideally), leading to higher gain for BJTs (better).

- MOSFETS are far more widely used in IC design for several reasons (despite superior transconductance of BJTs):
  1. Zero input current leads to no static power dissipation for digital circuits, allowing large chips with millions of transistors.
  2. Easy to make complementary devices of comparable quality (Nmos/Pmos).
  3. Structure allows smaller devices and higher levels of integration.

- Most large ICs designed today are complex "Systems-on-Chip" containing both analog & digital circuits, analog circuits use MOSFETS since it is so much better for the digital circuits.

- Some processes are "BiCMOS", offering both BJTs and MOSFETS, great for analog design.

Modern CMOS processes:

- Described by "feature size", which is the smallest possible feature that can be created (L (feature)) corresponds to the smallest possible length of a MOSFET.

- Current companies are rolling out 45 nm processes for production.
- Move to a smaller feature size every 1.5-2 years, double # of transistors on chip (Moore's law).
- Next: 32 nm, 22 nm
- Power supply voltages are now very low (1V)

We will focus on MOSFETS on BJTs, so let's get started!

MOSFET Current Mirrors

- In our discussion of amplifier stages we used a current source for biasing, in an IC:

  \[ I_{DD} \]

  \[ R \]

  \[ I_{I} \]

  \[ V_{DD} \]

  \[ I_{D1} \]

  \[ M1 \]

  \[ V_{S} \]

  \[ M2 \]

- Consider transistors one at a time

- \[ M1: \] gate connected to drain ("diode connected")

  \[ V_{DS} = V_{GS}, \quad I_{D} > (V_{DS} - V_{T}), \quad \text{always in saturation} \]

  \[ I_{D1} = \frac{M}{2} \left( \frac{V_{S} - V_{T}}{I} \right) \]

(1) \[ I_{D1} = \frac{M}{2} \left( \frac{V_{S} - V_{T}}{I} \right) \]
**Equation 2** \( I_{D2} = \frac{V_{DS}}{R} \)

- Combine (1) and (2) to find \( V_{DS} \) and \( I_{D2} \).

- Now, \( V_{DS} \) for \( M2 \) = \( V_{DS} \) for \( M1 \), so as long as \( M2 \) has a \( V_{DS} \) high enough to keep it in saturation,

\[
I_{D2} = \frac{M \cdot I_{D1} \cdot (L/L') \cdot (V_{DS} - V_t)^2}{2}
\]

- So, neglecting the finite output impedance (due to channel length modulation in \( M2 \)), \( I_{D2} = I_{D1} \) with a scaling factor of \( (L/L')^2 \).

- This is very useful for replicating a \( I_{D1} \) current at different points in a circuit.

- Can plot output current vs. output voltage: (just \( I_{D2} - V_{DS} \) relationship of \( M2 \)).

- Finite slope due to finite output impedance (= \( V_o \) of \( M2 \)).

- This also assumes we need to "sink" a current of \( I_{SFP} \), if we need to "source" that same current we can use PMOS devices:

- Same circuit can be used with BSFJs, although \( I_{SFP} - I_o \) relationships are not as simple due to finite base current.

- Big reason to use differential amplifier is reduced sensitivity to noise & interference.

- Diff. amps are well-suited for integrated circuits due to good matching between devices.