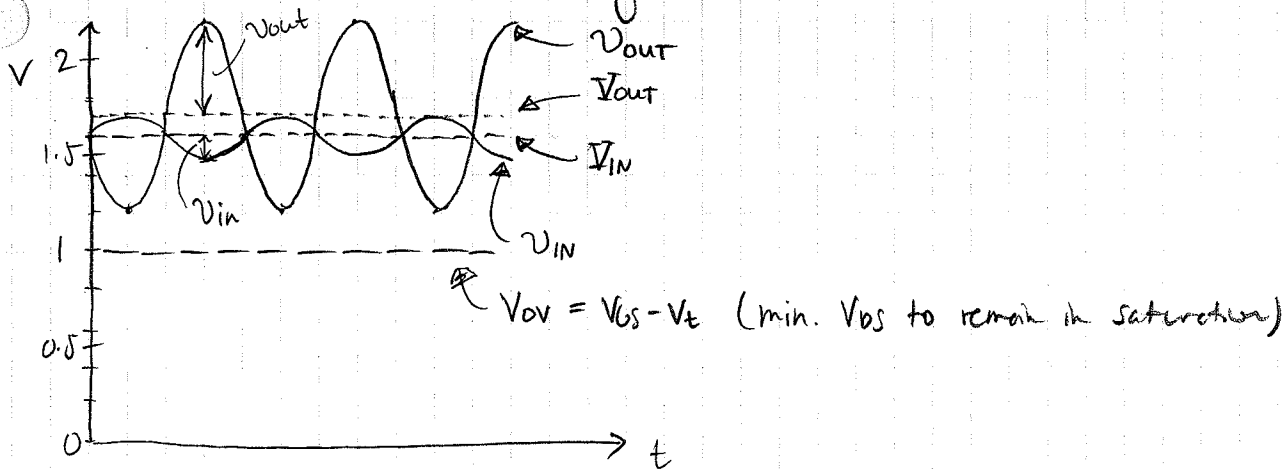


→ What do the signals actually look like?

- if we hooked up a DC coupled scope to the inputs and outputs, we would see the following:



→ as a check, device remains in saturation for this signal amplitude
 - if it entered triode region we would see significant distortion in the output wave.

→ This is the general procedure to use for any circuit that you analyze

- ① Establish bias conditions (ignoring signal component)
- ② Calculate small signal parameters using bias conditions
- ③ Use small signal model to calculate signal component (ignoring bias voltages & currents)
- ④ Check that assumptions used for small signal model hold true across signal range

→ It is very important to understand these concepts.

- If you learn anything at all from this course, this should be it.

Lecture # 13

Sept 10

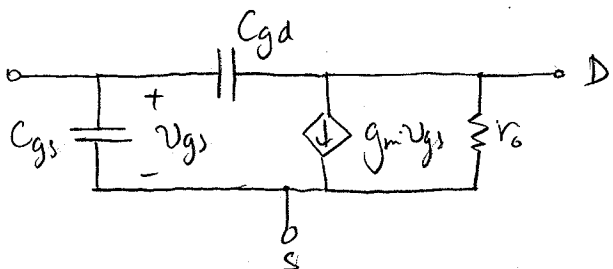
Next: Active Loads with differential pair

→ But first: review frequency behavior of amplifier, relevant to the rest lab.

→ so far we have not included capacitances in our s.s. model
 - these become important at higher frequencies

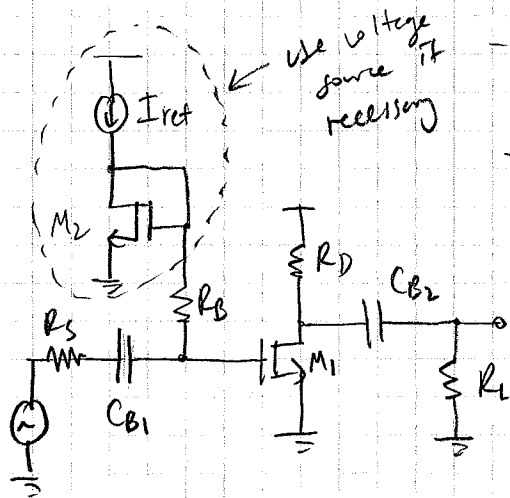
→ More complete s.s. model:

- can include other capacitances as well, but these are the dominant ones.



- these capacitances will cause the gain of MOSFET amplifiers to fall off at higher frequencies.

→ Let's reconsider the CS amplifier we talked about earlier:

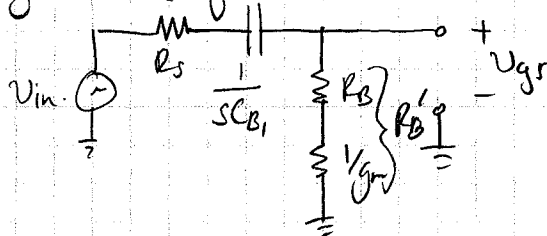


- M_2 acts as a current mirror, setting current in M_1 (may need to check matching in lab)
- R_B is blocking resistor, allowing dc bias voltage to pass but blocking signal.
- C_{B1}, C_{B2} are blocking caps, blocking dc but passing signals

→ Until now we have assumed $C_{B1,2}$ are large enough to be shorts at freq. of interest, and internal MOSFET caps. are small enough to be considered open circuits.

Low Freq: - at low frequencies, C_{B1}, C_{B2} will have large impedance, blocking signal { reducing gain: (neglect internal MOSFET capacitances)

Consider input to FET:



- so,
$$V_{gs} = V_{in} \cdot \frac{R_B'}{R_B' + R_s + 1/sC_{B1}} \quad (\text{voltage divider})$$

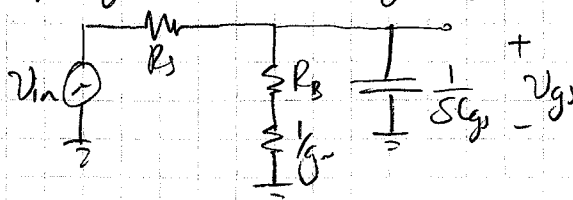
→ at higher frequencies, $\frac{1}{j\omega C_{B1}} \rightarrow 0$, $V_{gs} = V_{in} \cdot \frac{R_B'}{R_B' + R_s} \approx V_{in}$

- as $\omega \downarrow$, $\frac{1}{j\omega C_{B1}} \uparrow$, $V_{gs} \downarrow$.

- less of the input signal appears across the gate of the FET, gain falls off.

High Freq: - at high frequencies, neglect C_{B1}, C_{B2} , but must now consider internal capacitances, which will cause the gain to fall off.

- for simplicity, consider only C_{gs} ; and input to FET:



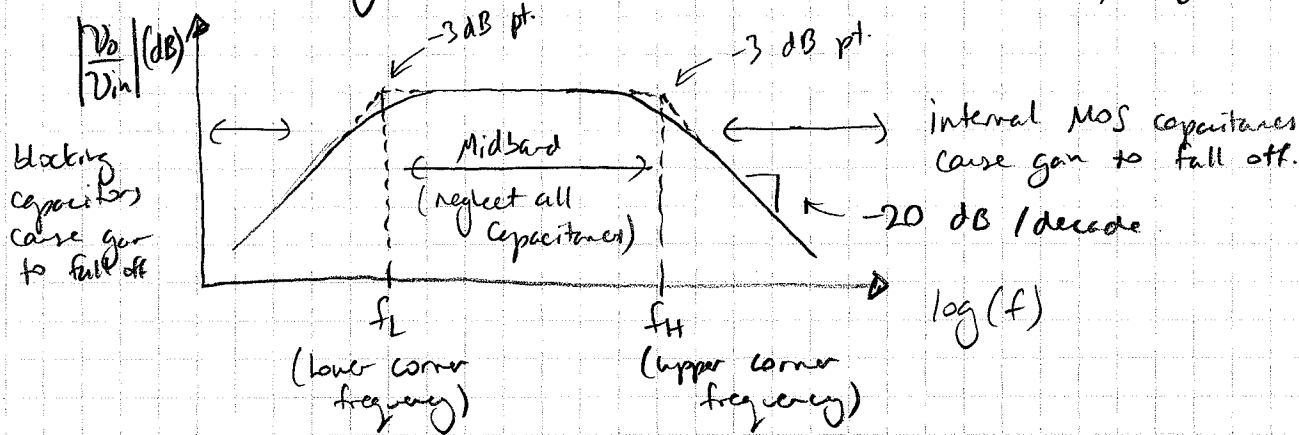
- so,
$$V_{gs} = V_{in} \cdot \frac{(R_B' \parallel 1/sC_{gs})}{R_s + (R_B' \parallel 1/sC_{gs})}$$

→ at low frequencies, $\frac{1}{sC_{gs}} \gg R_B'$, $V_{gs} = V_{in} \cdot \frac{R_B'}{R_s + R_B} \approx V_{in}$

→ as $\omega \uparrow$, $\frac{1}{sC_{gs}} \downarrow$, $(R_B' \parallel \frac{1}{sC_{gs}}) \downarrow$ (C_{gs} shorts out R_B'), $V_{gs} \downarrow$

- again, less signal appears across gate, gain drops

→ Draw a magnitude Bode plot of the gain with frequency:



→ obviously we want our signals of interest to fall in the midband.

→ What are f_H, f_L ?

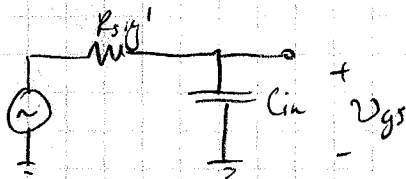
- see section 4.9 in the text for a full derivation,

$$\omega_H = \frac{1}{C_{in} R'_{sig}}, \text{ where } R'_{sig} = R_{sig} \parallel R_B' \quad \leftarrow R_B \text{ in the book, different topology}$$

$$C_{in} = C_{gs} + C_{gd}(1 + g_m R_L')$$

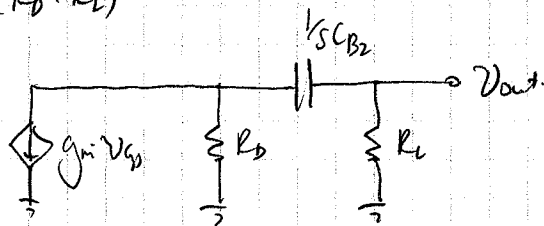
↑ Miller Effect.

→ dominant pole is that of equivalent input RC circuit:



$$\omega_L = \frac{1}{C_{B2}(R_D + R_L)}$$

→ dominant pole is at output.



- neglect r_o

- not as obvious, but pole forms at $\omega = \frac{1}{C_{B2}(R_D + R_L)}$
(do the math)

- book lists dominant pole as being due to C_s , we don't have that in our architecture.

→ there will be many other non-dominant poles:
- we care most about the dominant poles.

