

Final Design Project

- **Project Proposal due Friday, April 11 by 6:00 pm**
- **Final project report due Friday, May 2 by 6:00 pm.**

In this project, you will design, lay out, and simulate an analog integrated circuit. You are free to select the system you wish to create, but it must have a significant analog component (i.e., not all digital), and it must be significantly more complex than an op-amp or a comparator. You will likely need to read ahead in the textbook or consult other books or journal articles to come up with a suitable project.

You may work individually, or in a team of two people. Larger teams are not allowed. Each team need only turn in one project proposal and final report.

Possible projects include, but are not limited to:

- A digital-to-analog converter (Chapters 11, 12) or analog-to-digital converter (Chapters 11, 13) with sample-and-hold input (Chapter 8).
- A switched-capacitor filter (Chapters 9, 10).
- A continuous-time filter (Chapter 15).
- A bandgap voltage reference (Chapter 8).

Some projects could involve a fair amount of digital design (e.g., the state machine controlling a successive-approximation ADC). It is recommended that you have taken ECE/CS 6710 to tackle such a design, as the T.A. in this class cannot spend much time helping you with digital synthesis tools.

Optional Chip Fabrication: If you wish, you may have your circuit fabricated over the summer in AMI's 0.5 μm CMOS process. If you have your chip fabricated, you may take a one-credit "Analog IC Testing" class (ECE 6722) in the fall semester. You will receive credit for testing your chip and writing a report on the test results. You must be enrolled for the following fall semester if you wish to have your chip fabricated this summer. Having your chip fabricated will not affect your grade in this class, but it will require more work on your part: you will have to connect "pads" in your layout that will surround the perimeter of the chip and connect your circuitry to the IC ceramic package via bondwires. This topic will be discussed in class in greater detail. **If you wish to have your design fabricated, it must fit within an area of 900 μm \times 900 μm . It can use up to 40 pins, including power and ground.** Final chips GDS file, complete with pads for fabrication, must be submitted no later than noon on Monday, May 14.

Project Proposal

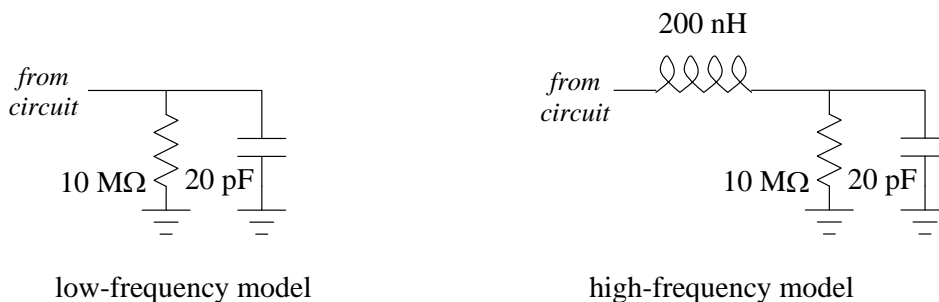
In one week, you must submit a one-page project proposal containing the following information:

- Name(s) and e-mail address(es) of team member(s). (This *must* be typed, not handwritten!)
- Description of proposed project. What are you going to design, and what are your performance specifications, in terms of power, speed, accuracy, etc.? It's okay if these specs change as your design progresses, but it is important to put down rough target specs now. Reference any relevant book chapters or journal articles. If your project involves subcircuits such as op-amps or comparators, discuss the performance requirements for these units.
- Do you wish to have your chip fabricated over the summer?

A Note on Simulation

In your simulations (*not* your layout), you are *required* to include an “off-chip load” of 20 pF in parallel with 10 M Ω to any output signals. This load is roughly equivalent to the parasitic impedances of the ceramic package (1-5 pF), breadboard (2-6 pF), and a 10 \times oscilloscope probe (8-15 pF in parallel with 10 M Ω). If you intend your circuit to operate at frequencies higher than 10 MHz, you should also include the typical series inductance of a 10 \times oscilloscope probe: about 200 nH. (The bond wires and ceramic package also contribute about 10 nH, but this can be neglected due to the dominance of the probe inductance.)

Off-Chip Load Models



Final Project Report

Your final report must contain the following:

1. A cover page with your name(s), e-mail address(es), and project title.
2. Readable schematics. Neatly draw schematics of your project. You may wish to include several pages. For example, if your system uses op-amps, draw one schematic of the overall system with the standard triangular op-amp symbol, then draw the internal schematic of the op-amp on a separate page. Uses as many

- pages as you need to make the schematics readable. Start with the “big picture” and then move on to the details. Label each transistor with a different number (e.g., “Q1”, “Q2”, etc.) so that you may reference specific transistors in your report and write the width and length of the device (in microns) beside each transistor in the format (“W/L”). For example, if you make a transistor with $W = 15 \mu\text{m}$ and $L = 0.6 \mu\text{m}$, you might write beside it, “Q8 15/0.6”.
3. Layout. A full-page printout of your layout, zoomed in so that your circuit fills the entire screen. Label the x and y dimensions of your circuit, in microns. Also label relevant input and output signals and/or draw boxes around subsections of your circuit and label them. For example, you might draw a box around an op-amp inside your circuit and label it as “op-amp 1”.

The rest of the report must be typed (not hand-written) using a word processor. Cadence plots should be inserted into the document as figures, *not* attached as separate sheets.

4. Project description. Describe what you have designed. List the performance specifications (e.g., power, speed, etc.) of your circuit. Explain what circuit-design strategies you used to build this circuit. If you used significant subcircuits such as op-amps or comparators, discuss their design.
5. Simulated circuit performance. Go through all the required performance metrics listed above and discuss your results for each simulation. In other words, prove (with simulation results) that you met your performance specs. Include the requested plots as figures within this text. Remember, do *not* include Cadence plots as separate sheets; insert the graphics directly into your word-processed document!
6. Testing strategies. (You must include this section even if you are not having your chip fabricated.) How would you test this chip if it were fabricated? Discuss the general types of equipment you would need (e.g., function generators, oscilloscopes, etc.), and describe how you would connect your chip to measure data that would verify its simulated performance.
7. Limitations, trade-offs, and future improvements. What limitations of the technology stopped you from making your circuit perform even better? Discuss any trade-offs you observed while optimizing your circuit. In what way could you improve this circuit in the future if you had more time?

Grading will be based both on the quality of your report and the quality of your design. ECE 5720 and 6720 will be graded separately.