Switched-Capacitor Circuits [Ch. 10]

The basic premise of switched-capacitor circuits is that continuous time resistors can be replaced by clocked capacitors.

\[ \Phi_1, \Phi_2 \]

\[ V_1, V_2 \]

\[ C_1 \]

- Here \( \Phi_1 \) and \( \Phi_2 \) are complementary non-overlapping clocks.

- Recall that \( Q = C \cdot V \) for a capacitor.

\[ \text{Operation:} \]

1. \( \Phi_1 \) high, \( \Phi_2 \) low: \( C_1 \) charges to \( V_1 \)

2. \( \Phi_1 \) low, \( \Phi_2 \) high: \( C_1 \) charges to \( V_2 \).

- During \( T \), the total charge transferred is

\[ \Delta Q = C_1 \cdot V_1 - C_1 \cdot V_2 \]

\[ = C_1 (V_1 - V_2) \]

- Eq. If \( V_1 = 1 \text{V}, V_2 = 0 \text{V} \), then during \( \Phi_1 \) all of this charge is dumped into \( V_2 \), for

\[ \Delta Q = C_1 (1 - 0) = 1 \cdot C_1 \]

- So, the average current flow will be

\[ I = \frac{Q}{t} = \frac{C_1 (V_1 - V_2)}{T} \]

- Now, for a resistor we have

\[ \Delta V = I \cdot R \implies V_1 - V_2 = I \cdot R \]

- For this capacitor circuit, we have

\[ I = C_1 (V_1 - V_2) \]

\[ \implies V_1 - V_2 = \frac{I}{C_1} \]

- So the capacitor circuit can be seen to be equivalent to a resistor of value

\[ R_{eq} = \frac{1}{C_1} = \frac{1}{f \cdot C_1} \]

- One way to design S.C. circuits is by taking cont. time RC circuits and replacing the resistors with the above circuit.

- Let's try this for a simple active circuit: an integrator.
Continuous-time RC Opamp Integrator

\[ \text{Current of } I_m = \frac{\text{Vin}}{R} \text{ flows in resistor due to virtual ground.} \]

\[ \text{Flow into capacitor: } \text{Vout} = \frac{Q}{C_2} \]

\[ Q = \int_{t_0}^{t} I_m dt \]

\[ \text{Vout} = -\frac{1}{C_2} \int_{t_0}^{t} \text{Vin} dt \]

\[ \text{So, this is an inverting integrator:} \]

\[ \text{for constant } \text{Vin} = 1V: \]

\[ \text{Vout} = -\frac{1}{RC_2} \]

Now let's replace the resistor with a switched-capacitor:

Assume Vout has an initial value of 0V.

\[ \text{Operate: } 0 \text{ } \Phi_1 \text{ } \text{high, } \Phi_2 \text{ low: } \text{Vin} \]

\[ \text{Vout} = 0V \]

\[ C_1 \text{ charges up to } \text{Vin} \text{ and stores a charge of } Q_{in} = C_1 \cdot \text{Vin} \]

\[ \text{Operate: } \Phi_1 \text{ low, } \Phi_2 \text{ high: } \text{Qin} \]

\[ \text{Vout = Vin} \]

Charge on C1 must flow somewhere since -ve opamp input is pegged to virtual ground.
→ Flow onto $C_2$, causing a voltage change of $\Delta V_{in} = -\frac{Q_{in}}{C_2} = -\frac{C_1}{C_2} \cdot V_{in}$

- The change in voltage is added to whatever voltage was already present on capacitor (0 V in this example).

Now, $V_{out} = V_{in}$ due to virtual ground.

→ So, next time $Q_1$ goes high, $V_{out} = 0 V - \frac{C_1}{C_2} \cdot V_{in}$

→ Since this is discrete-time operation, this can be expressed as:

$$V_{out}(n) = V_{out}(n-1) - \frac{C_1}{C_2} \cdot V_{in}(n-1)$$

→ Clearly this is performing an integration, plot output to compare to continuous time circuit:

[Diagram showing voltage changes over time]

→ Again let $V_{in} = 1 V$

$$\text{Slope} = \frac{\text{rise}}{\text{run}} = -\frac{C_1}{C_2} \cdot \frac{1}{T} = -\frac{C_1}{C_2} \cdot \frac{1}{T}$$

→ Compare to cont.time:

- RC: slope = $-\frac{1}{RC}$
- S-C: slope = $-\frac{C_1}{C_2} \cdot \frac{1}{T}$

→ Notice that in the RC version, the slope depends on absolute values of $R \approx C$, not very well controlled for 20% tolerances.

→ In the S-C version, the slope depends on ratio of $C_1$ to $C_2$ (well-controlled) and $T$ (well-controlled if coming from a crystal oscillator).

- So with S-C circuit we can build filters where we have much better control over pole and zero locations.

→ Since S-C circuit is equivalent to RC circuit at low frequencies, at high frequencies (approaching half the sampling frequency), more accurate analysis is provided by discrete time Z-transform analysis.
Take Z-transform of \( V\text{out} (n) = V\text{out} (n-1) - \frac{C_1}{C_2} \cdot V\text{in} (n-1) \)

\[ V\text{out} (z) = z^{-1} \cdot V\text{out} (z) - \frac{C_1}{C_2} \cdot z^{-1} \cdot V\text{in} (z) \]

\[ \Rightarrow H(z) = \frac{V\text{out} (z)}{V\text{in} (z)} = -\left( \frac{C_1}{C_2} \right) \cdot \frac{z^{-1}}{1 - z^{-1}} = -\left( \frac{C_1}{C_2} \right) \left( \frac{1}{z-1} \right) \]

Peronitics

We have mentioned previously that poly-poly capacitors have a significant peronitic capacitance to ground.

- Worse for bottom plate, but exists for top plate also.
- When using these capacitors in our circuits, we should pay attention to their orientation and place the bottom plate on the less sensitive node.

Let's look at the impact of peronitics on the S-C integrator:

Consider effect of each cap:
- \( C_{p_1} \): adds to \( C_1 \)
- \( C_{p_2} \): no effect (both ends grounded)
- \( C_{p_3} \): no effect (one end grounded, one end virtual ground)
- \( C_{p_4} \): increases output load, but no effect on accuracy

So the result is that the transfer function becomes:

\[ H(z) = -\left( \frac{C_1 + C_{p_4}}{C_2} \right) \cdot \frac{1}{z-1} \]

This is undesirable as \( C_{p} \) is not well controlled and leads to reduced accuracy in designing S-C circuits.

The book describes several variations on this topology that are not impacted by this peronitic capacitor.

Let's use an example to illustrate S-C filter design.
Example: We have a signal that is band-limited to 10 kHz. Design a 1st order low-pass S-C filter to filter out content above 8 kHz. (design)

1. Choose a sampling frequency: need \( f_s/2 \geq 10 \text{ kHz} \Rightarrow f_s \geq 20 \text{ kHz} 
   - Choose \( f_s = 40 \text{ kHz} \) to be safe.

2. Determine the pole location:
   - This can be done directly in the discrete time domain, but another option is to map to the continuous time domain, choose the pole, then map back to the \( Z \)-domain.

   \[
   \frac{\pi}{2} \Rightarrow \pi \\
   \frac{f_s}{2} \Rightarrow 2\pi
   \]

   \[
   -0.3249 \downarrow \rightarrow 0.3249
   \]

   \[
   Z = \frac{1 + s}{1 - s} \quad \text{Bilinear Transform}
   \]

   \[
   \Rightarrow Z = \frac{1 - 0.3249}{1 + 0.3249} = 0.5095
   \]

3. Choose the filter topology: Let's start with a continuous time architecture and convert it to a digital version.

   \[
   V_{out} = -\frac{Z_2}{Z_1} = -\frac{R_2}{1 + SR_3C} \quad \frac{1}{R_1} = -\frac{R_2}{1 + SR_3C} 
   \]

   \[\Rightarrow \text{dc gain } -\frac{R_2}{R_1}, \text{ pole at } w = -\frac{1}{R_2C} \]
Operation: 
\[ \Phi_1 \text{ high: } Qc_1 = C_1 \cdot V_{in}(n-1) \]
\[ Qc_2 = C_2 \cdot V_{out}(n-1) \]

\[ \Phi_2 \text{ high: } V_{out}(n) = V_{out}(n-1) - \frac{Qc_1}{C_3} - \frac{Qc_2}{C_3} \]
\[ V_{in}(n) = V_{in}(n-1) - \frac{C_1 \cdot V_{in}(n-1)}{C_3} - \frac{C_2 \cdot V_{out}(n-1)}{C_3} \]

Take \( Z \)-transform:
\[ V_{out}(z) = z^{-1} \cdot V_{out}(z) - z^{-1} \cdot \frac{C_1 \cdot V_{in}(z)}{C_3} - z^{-1} \cdot \frac{C_2 \cdot V_{out}(z)}{C_3} \]

Transfer function:
\[ \frac{V_{out}(z)}{V_{in}(z)} = H(z) = \frac{-C_1/C_3}{z - \frac{C_2}{C_3}} \]

The book presents a signal-flow analysis that allows one to go more directly from the filled schematic to the \( Z \)-domain transfer function.

\( \Phi \) & \( \Phi_2 \):
- dc gain: set \( z = 1 \) \( (e^{j0}) \):
\[ H(1) = \frac{-C_1/C_3}{1 - \frac{C_2}{C_3}} = -\frac{C_1}{C_2} \]
- pole freq: \( z = \frac{C_3 - C_2}{C_3} \)

\( \Phi \) & \( \Phi_2 \):
- pole: \( 0.5095 = \frac{C_3 - C_2}{C_3} \Rightarrow C_3 = \frac{C_2}{0.4905} \)

- Choose \( C_2 = 5 \text{ pF} \) \( \Rightarrow \) \( C_1 = 10 \text{ pF} \), \( C_3 = 10.19 \text{ pF} \)

- Many, many other \( S-C \) circuits; see text for details.