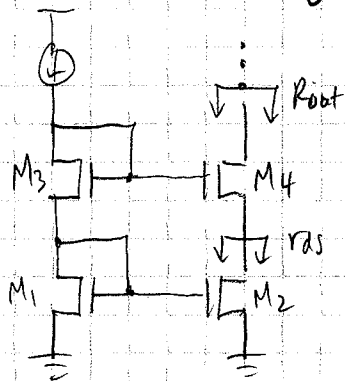


Cascode Current Mirror

- The input impedance of the source degenerated current mirror increases for larger R_s .
- we want a very large effective R_s , but without the large size and large voltage drop.

→ How about using a transistor?



→ M_1 & M_2 form a normal current mirror, so resistance looking into M_2 is r_{ds2}

→ M_4 is a source degenerated current mirror with M_2 acting as R_s , so we can calculate R_{in} as:

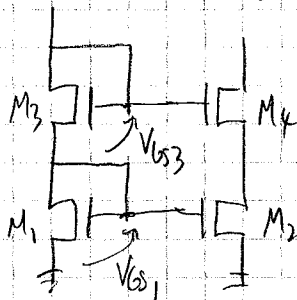
$$R_{out} \approx r_{ds4} (1 + g_m r_{ds2})$$

- as we saw in the example, r_{ds2} is on the order of $k\Omega$, so this leads to a substantial increase in output impedance.

* → How about the minimum voltage at the output to keep all transistors in saturation?

- For channel at drain of M_4 to be pinched off, drain must be no more than one V_T below the gate.

→ Find V_{G4} :



$$- V_{G4} = V_{GS1} + V_{GS3}$$

$$\therefore V_{out, \min} = V_{GS1} + V_{GS3} - V_T$$

$$= 2V_{GS1} - V_T$$

(if $M_1 = M_3$)

→ This arrangement of transistors (stacked) is called a "cascode".

Example: Let's redo the last example for the cascode current mirror

(a) R_{out} ? $R_{out} \approx r_{ds4} (1 + g_m r_{ds2}) = 2.91k (1 + 2.1E-3 \cdot 2.91k)$
 $= 20.7k$

(b) % error? $\Delta I_D = \frac{\Delta V_D}{R_{out}} = \frac{2}{20.7k} = 0.097 \text{ mA} \Rightarrow \frac{0.097}{2.75} \times 100\% = 3.5\%$

(c) $V_{out, \min}$? $V_{out, \min} = 2V_{GS1} - V_T = 2(3.62) - 1 = 6.24 \text{ V}$

→ Let's recap with a comparison of the three current mirrors from these examples:

(trade-offs)

	Basic	Source Deg. ($R_s = 400 \Omega$)	Cascade
R_{out}	2.75 k	5.35 k	20.7 k
% error	25%	13%	3.5%
$V_{out, min}$	2.62 V	3.72 V	6.24 V
Size	Smallest	largest	small

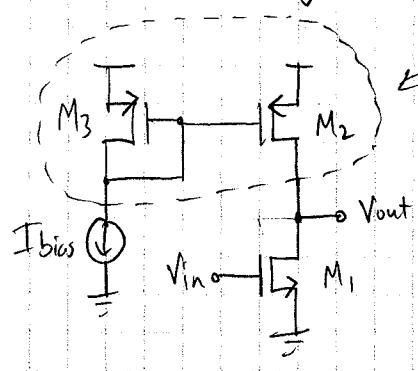
→ The text also covers another high impedance current mirror called the Wilson Current Mirror.

- this is like the cascade but with only half the output impedance, so we won't bother covering it here.

→ Now that we have beaten the current mirror to death, let's take a look at single stage transistor amplifiers

Common-Source Amplifier [32] Reading: Sections 3.2, 3.7, 3.11 (part on common source)

- Useful when you need high gain, high input impedance



← current mirror. (active load)

→ Both M_1 & M_2 are biased in the saturation region.

Large Signal Analysis

- Current mirror formed by M_2 & M_3 is referred to as an "active load"
- better than a resistive load for several reasons:
 - transistors are much smaller than resistors
 - presents a large load impedance when biased in saturation region, without excessive voltage drop
 - also biases M_1 with desired current (I_{bias}), with better control than a resistor.

→ As long as M_1 & M_2 are in saturation and the dc level of V_{in} is appropriate, the bias current in M_1 & M_2 will be I_{bias} .

Small Signal Analysis

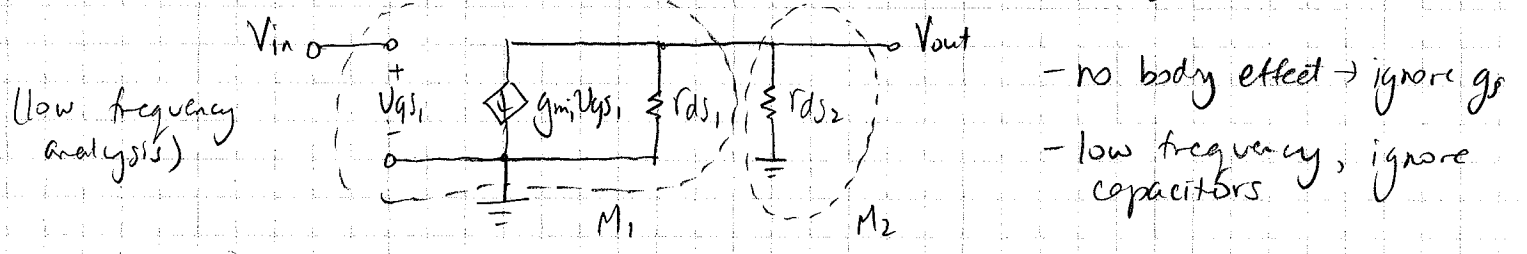
- Recall two rules of small signal analysis:
 - 1) independent voltage sources (dc, large signal) are shorted in the small signal analysis (grounded)

2) Independent current sources (dc, large signal) are open-circuited in the small signal analysis.

→ So, the analysis of the pmos current mirror formed by M_2 & M_3 is the same as the nmos case we have already considered.

- looking into the drain of M_2 we see just a resistance of r_{ds2} (to ground)

→ We can use this to simplify the small signal analysis:



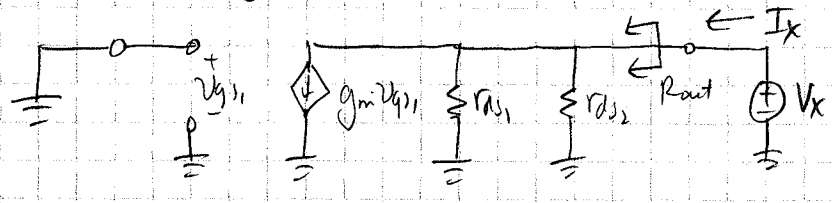
- no body effect → ignore g_s
 - low frequency, ignore capacitors

→ Find gain: $V_{gs1} = V_{in}$, $V_{out} = -g_{m1} V_{gs1} (r_{ds1} || r_{ds2})$

$V_{out} = -V_{in} \cdot g_{m1} (r_{ds1} || r_{ds2})$

Voltage gain: $A_v = \frac{V_{out}}{V_{in}} = -g_{m1} (r_{ds1} || r_{ds2})$

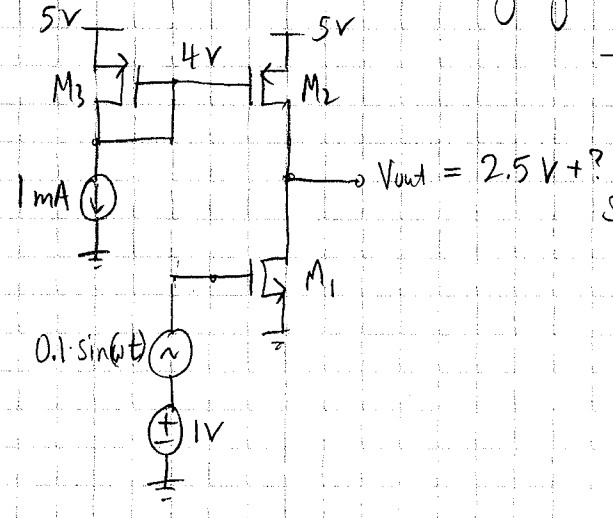
→ Output impedance: - ground input, put test source at output.



→ $V_{gs1} = 0 \Rightarrow g_m$ has no effect

$\therefore R_{out} = \frac{V_x}{I_x} = r_{ds1} || r_{ds2}$

Qualitative look at what is going on



- small signal analysis we just covered is a simplification w/o the large signal equations that govern the behavior.

Steady state: - all transistors are biased with 1 mA
 - $V_{gs1} = |V_{gs2}|$, V_{out} is between the power rails

→ Now suppose we increase V_{in} slightly (through sinusoidal source)

- for M_1 : $I_{D1} = \frac{\mu_n C_{ox} (W/L)}{2} (V_{DS1} - V_T)^2 (1 + \lambda V_{DS1})$

→ so, by increasing V_{DS1} , we are increasing I_{D1} from it's nominal value of 1 mA

- I_{D1} must be equal to I_{D2} , so if I_{D1} increases then I_{D2} must also.

→ but, $|V_{DS2}|$ has not changed, so how can it's current increase?

$$I_{D2} = \frac{\mu_n C_{ox} (W/L)}{2} (V_{DS2} - V_T)^2 (1 + \lambda V_{DS2})$$

↑ this must increase

- so, V_{DS2} increases so that $I_{D1} = I_{D2}$, corresponding to a drop in V_{out} .

→ This explains the negative gain, an increase in V_{in} leads to a drop in V_{out} .

- when V_{in} drops, opposite occurs: V_{DS1} drops, I_{D1} drops, I_{D2} drops, $|V_{DS2}|$ drops, V_{out} rises.

→ Solving these equations to find amount of increase in $|V_{DS2}|$ for an increase in V_{DS1} is difficult

- this is why we use the linearized small signal parameters: g_m & r_{ds}

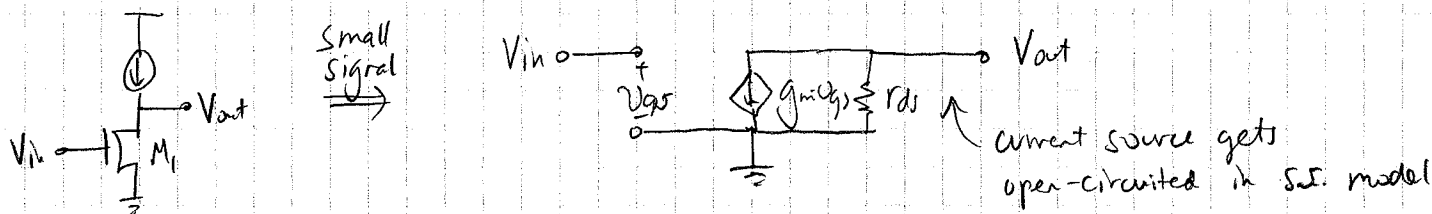
5720/6720: Lecture #8

Jan. 31

Common-Source Amplifier with Cascode [3.7]

→ What if we want more gain out of this stage?

- if we replaced the active load with an ideal current source, model would be:



gain: $A_v = -g_m r_{ds}$, (about double what it was before).

→ Now, gain is limited by the finite output impedance of M_1 (r_{ds})

- for further increases, we to increase the impedance seen looking into the drain of M_1 .

→ As with the current mirror, we can again use a cascode (stacked transistors) to achieve this.