

UNIVERSITY OF UTAH

ELECTRICAL AND COMPUTER ENGINEERING DEPARTMENT

ECE/CS 5720/6720

Analog Integrated Circuit Design

Midterm

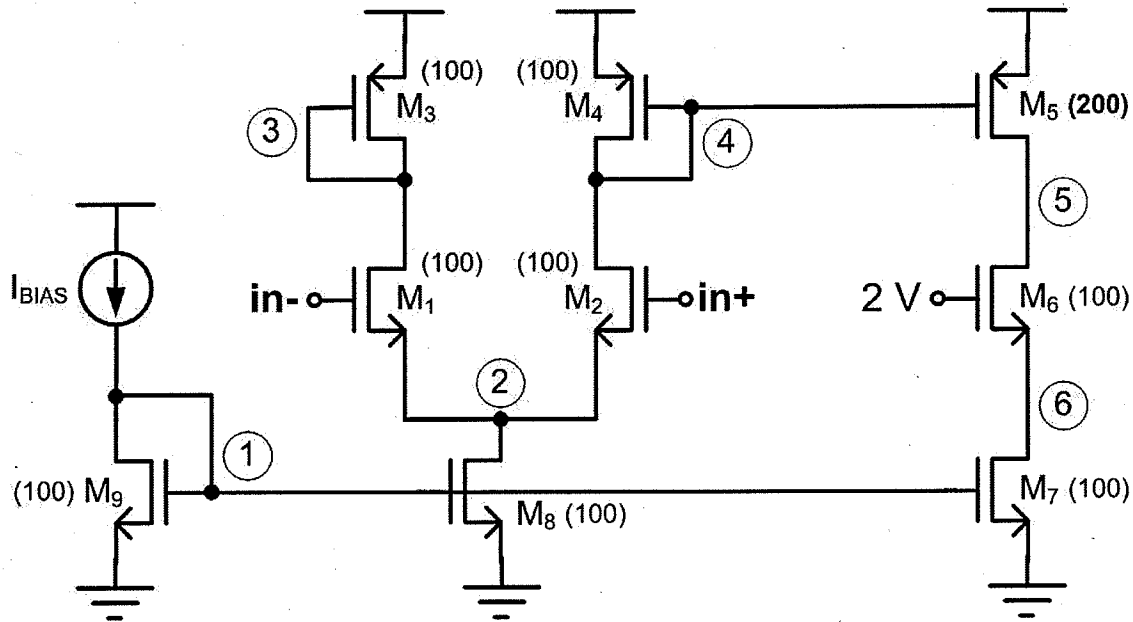
March 6, 2008

NAME: McLovin ECE/CS 5720 ECE/CS 6720
circle one

(Please print)

- Do not open the exam until instructed.
- Draw a circle or box around your final answers.
- All answers should include units (e.g., V, mA, k Ω) where appropriate. **For frequencies, use Hz (or kHz, or MHz), *not* radians/second.**
- If you want partial credit on incorrect answers, *show your work on the pages you turn in!* If you choose to turn in any sheets of scratch paper, *write your name on those sheets!*
- Don't spend all of your time on one difficult problem. Don't be afraid to skip ahead if you get stuck. You don't have to work the problems in order.
- The use of any wireless communication devices is prohibited during the exam.

1. (20 points total) Consider the op-amp shown below. You may assume that all the transistors are operating in saturation mode. Device W/L ratios are given in brackets beside each device, and node numbers are circled. V_{DD} is 5 V, and $in- = in+ = 2.5$ V.



$$V_{in} = -V_{tp} = 0.7 \text{ V}$$

$$\mu_p C_{ox} = 40 \mu\text{A}/\text{V}^2$$

$$I_{BIAS} = 100 \mu\text{A}$$

$$\mu_n C_{ox} = 80 \mu\text{A}/\text{V}^2$$

(a) (12 points) Using large signal analysis, solve for the dc voltages at the following nodes, **ignoring body effect and channel length modulation**:

$$V_1 = \underline{0.858 \text{ V}} \quad V_1 = V_{bs9}; \quad V_{gs9} = V_{tn} + V_{eff9}; \quad V_{eff9} = \sqrt{\frac{I_D \cdot 2}{\mu_n \cdot C_{ox} \cdot W/L}} = \sqrt{\frac{100e-6 \cdot 2}{80e-6 \cdot 100}} = 0.158$$

$$V_2 = \underline{1.688 \text{ V}} \quad V_2 = in+ - V_{bs2}; \quad V_{gs2} = V_{tn} + V_{eff2}; \quad V_{eff2} = \sqrt{\frac{50e-6 \cdot 2}{80e-6 \cdot 100}} = 0.112$$

$$V_4 = \underline{4.142 \text{ V}} \quad V_4 = V_{DD} - |V_{bs4}|; \quad |V_{gs4}| = |V_{tp}| + V_{eff4}; \quad V_{eff4} = \sqrt{\frac{50e-6 \cdot 2}{40e-6 \cdot 100}} = 0.158$$

$$V_6 = \underline{1.142 \text{ V}} \quad V_6 = 2 - V_{bs6}; \quad V_{gs6} = V_{tn} + V_{eff6}; \quad V_{eff6} = \sqrt{\frac{100e-6 \cdot 2}{80e-6 \cdot 100}} = 0.158$$

(b) (2 points) What is the minimum allowable common-mode input voltage to keep all of the transistors in saturation?

$$\begin{aligned} V_{CM, \min} &= V_{GS, 11} + V_{eff, 8} & V_{eff, 1} &= 0.112 \\ &= 0.7 + 0.112 + 0.158 & V_{eff, 3} &= V_{eff, 4} = 0.158 \end{aligned} \quad \left. \vphantom{\begin{aligned} V_{CM, \min} &= V_{GS, 11} + V_{eff, 8} \\ &= 0.7 + 0.112 + 0.158 \\ &= 0.970 \text{ V} \end{aligned}} \right\} \text{from previous part}$$

(c) (1 point) Which node should be taken as the output of the op-amp?

⑤

(d) (2 points) Between which two nodes should the compensation capacitor be connected, if the Miller effect is to be exploited?

④ & ⑤

(e) (3 points) Provide an approximate expression for the low frequency differential gain of this op-amp, assuming the output node is as specified in part (c). Your answer should be in terms of the g_m and r_{ds} of the various devices (e.g., g_{m1} , r_{ds1}).

$$\begin{aligned} A_u &= \frac{g_{m2}}{2} \cdot 2 \cdot (r_{ds5} \parallel r_{ds6} \cdot g_{m6} \cdot r_{ds7}) \\ &= g_{m2} \cdot (r_{ds5} \parallel g_{m6} \cdot r_{ds6} \cdot r_{ds7}) \end{aligned}$$

2. (2 points) In order to avoid latch-up, when doing layout we should (circle most appropriate answer):

- (a) avoid placing transistors too close to one another.
- (b) include plenty of substrate contacts.
- (c) avoid creating parasitic bipolar junction transistors.
- (d) place isolation trenches around all n-wells.

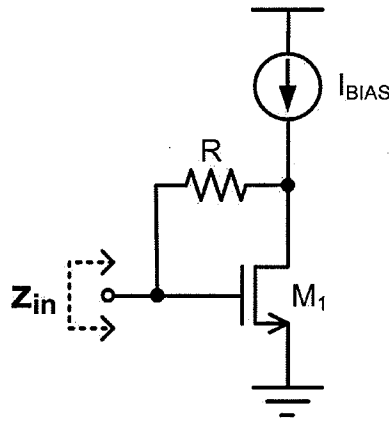
3. (2 points) An output buffer should be included in an op-amp design when the op-amp will be (circle most appropriate answer):

- (a) driving on-chip, capacitive loads.
- (b) used in a feedback configuration.
- (c) driving low-impedance loads.
- (d) used in a low-power design.

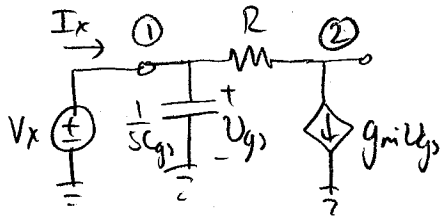
4. (2 points) Fingered transistor layouts are useful for (circle the most appropriate answer):

- (a) reducing source/drain to bulk capacitance.
- (b) reducing channel resistance.
- (c) minimizing body effect.
- (d) all of the above.

5. (10 points total) Consider the circuit shown below. Assume that M_1 is operating in the saturation region, and that **the current source has infinite output impedance**.



(a) (8 points) Find the small signal input impedance z_{in} , as shown above. For M_1 , you may assume that $r_{ds} = \text{infinite}$, and **neglect all parasitic capacitances except C_{gs}** . Leave your answer in terms of component values and small signal parameters



$$\text{KCL @ ①: } I_x = V_x \cdot sC_{gs} + \frac{V_x - V_2}{R}$$

$$R I_x = V_x \cdot sRC_{gs} + V_x - V_2 \quad \square$$

$$\text{KCL @ ②: } \frac{V_2 - V_x}{R} + g_m U_x = 0$$

$$V_2 - V_x + g_m V_x \cdot R = 0$$

$$V_2 = V_x (1 - g_m \cdot R) \quad (*)$$

$$\text{Sub } (*) \text{ into } \square: R \cdot I_x = V_x (1 + s \cdot R \cdot C_{gs} - 1 + g_m \cdot R)$$

$$\Rightarrow Z_{in} = \frac{V_x}{I_x} = \frac{R}{sRC_{gs} + g_m \cdot R} = \boxed{\frac{1}{g_m \left(1 + s \frac{C_{gs}}{g_m}\right)}} = Z_{in}$$

(b) (2 points) From your answer to part (a), over what bandwidth will this circuit have a constant input impedance? Your answer should again be in terms of component values and small signal parameters.

Z_{in} will be constant at $Z_{in} = \frac{1}{g_m}$ up until pole at

$$\omega_p = \frac{g_m}{C_{gs}}$$

6. (2 points) The Miller effect is useful for compensation because it (circle most appropriate answer):

- (a) allows us to use a smaller physical capacitor to achieve compensation.
- (b) moves the poles closer together.
- (c) moves the zero from the RHP into the LHP.
- (d) increases the phase margin.

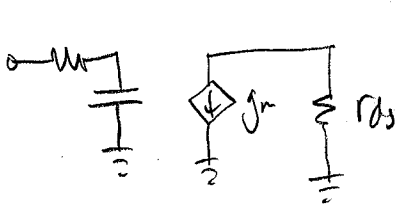
7. (2 points) Systematic offset voltage can be avoided in op-amp design by (circle most appropriate answer):

- (a) using a PMOS differential pair input stage.
- (b) always using the op-amp in a negative feedback configuration.
- (c) including a source-follower output stage.
- (d) sizing the transistors in a given branch to have equal bias currents.

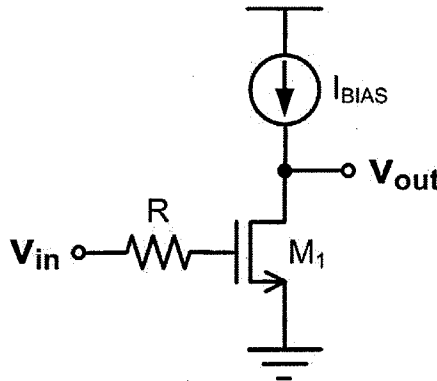
8. (2 points) Slewing behavior in an op-amp is undesirable because it (circle most appropriate answer):

- (a) reduces the phase margin of the op-amp.
- (b) increases the power consumption of the op-amp.
- (c) leads to distortion in the output signal.
- (d) all of the above.

9. (12 points total) Consider the circuit shown below. Assume that M_1 is operating in the saturation region, and that **the current source has infinite output impedance**. Also, for M_1 , $r_{ds} = 8000 \cdot L/I_D$ and you may **neglect all small signal capacitances except C_{gs}** . For each question below, circle the appropriate term and enter your numerical answer.



$$A_v = \frac{-g_m r_{ds}}{(1 + sR(C_{gs}))}$$



$$g_m = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D}$$

$$r_{ds} = \frac{8000 L}{I_D}$$

$$C_{gs} = W \cdot L \cdot \frac{C_{ox}}{t_{ox}}$$

(a) (3 points) If I_{BIAS} is doubled, the low frequency gain will increase / decrease by a factor of $\sqrt{2}$.

$$A_v \propto \frac{\sqrt{I_D}}{I_D} = \frac{1}{\sqrt{I_D}}$$

(b) (3 points) If t_{ox} for M_1 is reduced by one half, the 3-dB frequency will increase / decrease by a factor of 2.

$$\omega_{3dB} = \frac{1}{R \cdot C_{gs}} \propto t_{ox}$$

(c) (3 points) If the width of M_1 is doubled, the 3-dB frequency will increase / decrease by a factor of 2.

$$\omega_{3dB} \propto \frac{1}{W}$$

(d) (3 points) If the length of M_1 is reduced by one half, the low frequency gain will increase / decrease by a factor of $\sqrt{2}$.

$$A_v \propto \frac{L}{\sqrt{L}} = \sqrt{L}$$

10. (Bonus – 2 points total) An electrical engineering professor spends 90% of his time being afraid.

(a) (1 point) For how many minutes of the day is he afraid?

$$0.9 \cdot 24 \cdot 60 = 1296 \text{ minutes}$$

(b) (1 point) What is he so afraid of? (circle the most appropriate answer)

- i. bats.
- ii. maniacs.
- iii. not getting tenure.
- iv. snakes.