

UNIVERSITY OF UTAH

ELECTRICAL AND COMPUTER ENGINEERING DEPARTMENT

ECE/CS 5720/6720

## Analog Integrated Circuit Design

Midterm

March 6, 2008

NAME: \_\_\_\_\_ ECE/CS 5720 ECE/CS 6720  
circle one

(Please print)

- Do not open the exam until instructed.
- Draw a circle or box around your final answers.
- All answers should include units (e.g., V, mA, k $\Omega$ ) where appropriate. **For frequencies, use Hz (or kHz, or MHz), *not* radians/second.**
- If you want partial credit on incorrect answers, *show your work on the pages you turn in!* If you choose to turn in any sheets of scratch paper, *write your name on those sheets!*
- Don't spend all of your time on one difficult problem. Don't be afraid to skip ahead if you get stuck. You don't have to work the problems in order.
- The use of any wireless communication devices is prohibited during the exam.



(b) (2 points) What is the minimum allowable common-mode input voltage to keep all of the transistors in saturation?

(c) (1 point) Which node should be taken as the output of the op-amp?

(d) (2 points) Between which two nodes should the compensation capacitor be connected, if the Miller effect is to be exploited?

(e) (3 points) Provide an approximate expression for the low frequency differential gain of this op-amp, assuming the output node is as specified in part (c). Your answer should be in terms of the  $g_m$  and  $r_{ds}$  of the various devices (e.g.,  $g_{m1}$ ,  $r_{ds1}$ ).

2. (2 points) In order to avoid latch-up, when doing layout we should (circle most appropriate answer):

- (a) avoid placing transistors too close to one another.
- (b) include plenty of substrate contacts.
- (c) avoid creating parasitic bipolar junction transistors.
- (d) place isolation trenches around all n-wells.

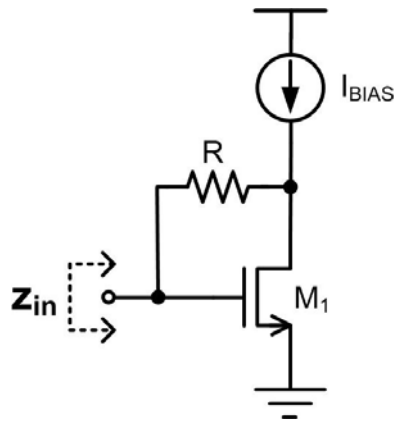
3. (2 points) An output buffer should be included in an op-amp design when the op-amp will be (circle most appropriate answer):

- (a) driving on-chip, capacitive loads.
- (b) used in a feedback configuration.
- (c) driving low-impedance loads.
- (d) used in a low-power design.

4. (2 points) Fingered transistor layouts are useful for (circle the most appropriate answer):

- (a) reducing source/drain to bulk capacitance.
- (b) reducing channel resistance.
- (c) minimizing body effect.
- (d) all of the above.

5. (10 points total) Consider the circuit shown below. Assume that  $M_1$  is operating in the saturation region, and that **the current source has infinite output impedance**.



(a) (8 points) Find the small signal input impedance  $z_{in}$ , as shown above. For  $M_1$ , you may assume that  $r_{ds} = \text{infinite}$ , and **neglect all parasitic capacitances except  $C_{gs}$** . Leave your answer in terms of component values and small signal parameters

(b) (2 points) From your answer to part (a), over what bandwidth will this circuit have a constant input impedance? Your answer should again be in terms of component values and small signal parameters.

6. (2 points) The Miller effect is useful for compensation because it (circle most appropriate answer):

- (a) allows us to use a smaller physical capacitor to achieve compensation.
- (b) moves the poles closer together.
- (c) moves the zero from the RHP into the LHP.
- (d) increases the phase margin.

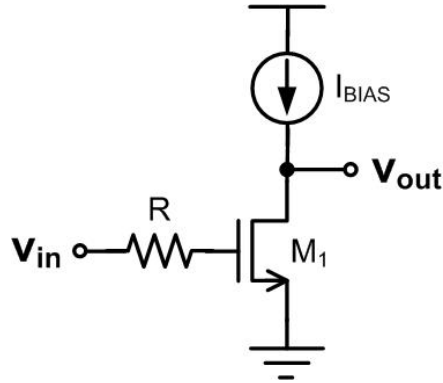
7. (2 points) Systematic offset voltage can be avoided in op-amp design by (circle most appropriate answer):

- (a) using a PMOS differential pair input stage.
- (b) always using the op-amp in a negative feedback configuration.
- (c) including a source-follower output stage.
- (d) sizing the transistors in a given branch to have equal bias currents.

8. (2 points) Slewing behavior in an op-amp is undesirable because it (circle most appropriate answer):

- (a) reduces the phase margin of the op-amp.
- (b) increases the power consumption of the op-amp.
- (c) leads to distortion in the output signal.
- (d) all of the above.

9. (12 points total) Consider the circuit shown below. Assume that  $M_1$  is operating in the saturation region, and that **the current source has infinite output impedance**. Also, for  $M_1$ ,  $r_{ds} = 8000 \cdot L/I_D$  and you may **neglect all small signal capacitances except  $C_{gs}$** . For each question below, circle the appropriate term and enter your numerical answer.



(a) (3 points) If  $I_{BIAS}$  is doubled, the low frequency gain will increase / decrease by a factor of \_\_\_\_\_.

(b) (3 points) If  $t_{ox}$  for  $M_1$  is reduced by one half, the 3-dB frequency will increase / decrease by a factor of \_\_\_\_\_.

(c) (3 points) If the width of  $M_1$  is doubled, the 3-dB frequency will increase / decrease by a factor of \_\_\_\_\_.

(d) (3 points) If the length of  $M_1$  is reduced by one half, the low frequency gain will increase / decrease by a factor of \_\_\_\_\_.

10. (Bonus – 2 points total) An electrical engineering professor spends 90% of his time being afraid.

(a) (1 point) For how many minutes of the day is he afraid?

(b) (1 point) What is he so afraid of? (circle the most appropriate answer)

- i. bats.
- ii. maniacs.
- iii. not getting tenure.
- iv. snakes.