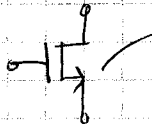


→ 4 main sections to be covered on the midterm.

① Devices

→ PN junctions: - junction capacitance (reduced with reverse bias)
- dependence on doping concentration

→ MOSFETs:  arrow indicates source terminal, direction indicates n-type material (also direction of current flow).

- Large signal behavior in 3 operating regions (I_D):

- 1) cutoff ($V_{GS} < V_T$)
- 2) triode ($V_{GS} > V_T$, $V_{DS} \leq V_{eff}$)
- 3) saturation ($V_{GS} > V_T$, $V_{DS} \geq V_{eff}$)

Also: - channel length modulation (in sat.)
- body effect

- Small signal models for 3 operating regions:

- 1) cutoff (trivial)
- 2) triode (like a resistor)
- 3) Saturation (Hybrid- π model)
 - include s.s. capacitances and body effect transconductance if needed

② Processing & Layout

→ general layout rules & techniques

- fingers
- getting circuits from a layout & vice versa

→ Latch-up

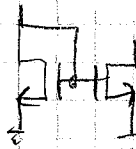
③ Basic Current Mirrors & Amplifiers (Building Blocks)

→ Determine operating region, sub in s.s. model and solve for s.s. gain, input/output impedance

→ Knowing what terms can be neglected

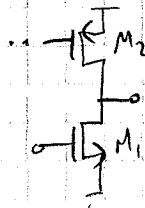
→ Doing quick s.s. approximations without subbing in the model.

- basic current mirror:



- $r_{out} = r_{ds}$

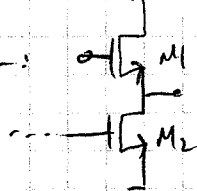
- common source amp:

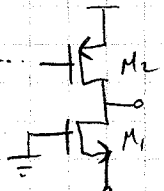


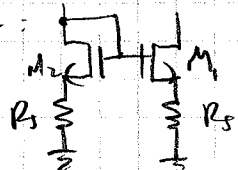
- $A_v = -g_m (r_{ds1} \parallel r_{ds2})$

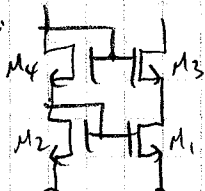
- $r_{out} = r_{ds1} \parallel r_{ds2}$

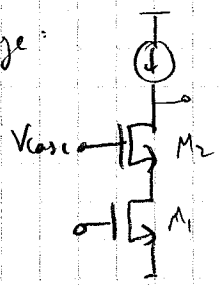
2

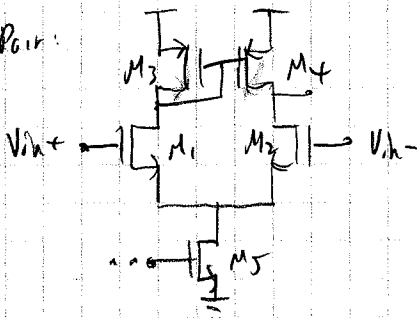
- Source Follower:  - $A_v \approx \frac{g_{m1}}{g_{m1} + g_{s1}}$ - $r_{out} \approx \frac{1}{g_{m1} + g_{s1}}$

- Common gate:  - $A_v \approx g_{m1} (r_{ds1} \parallel r_{ds2})$ - $r_{out} = r_{ds1} \parallel r_{ds2}$
- $r_{in} = \frac{2}{g_{m1}}$

- Source deg. current mirror:  - $r_{out} = r_{ds2} (1 + R_s (g_{m2} + g_{s2}))$

- Cascode current mirror:  - $r_{out} \approx r_{ds3} (r_{ds1} g_m)$

- Cascode gain stage:  - $A_v = g_{m1} [(r_{ds2} g_{m2} r_{ds1}) \parallel R_{cs}]$

- Diff. Pair:  $A_{diff} = g_{m1} (r_{ds2} \parallel r_{ds4})$
 $A_{cm} \approx \frac{-1}{2 g_{m3} r_{ds5}}$

④ Opamp Design & Compensation

→ DC gain, freq. response, slew rate, offset voltage.

→ Compensation: - theory behind this (phase margin)
- poles & zeros, RHP vs LHP
- C_c (Miller effect) & R_c (lead compensation)

→ Biasing (not bandgap voltage reference)