

Instances for NMOS & PMOS transistors

For NMOS transistors, select **NCSU_Analog_Parts** library and choose **N_Transistors** in the menu below. This will lead to a sub-menu where you would choose **nmos4**. This is a 4-terminal nmos transistor, the four terminals being Gate, Source, Drain and Body (or Substrate). For the process we are using, the body of a NMOS transistor will always be connected to Vss (our most negative supply voltage). On selecting **nmos4**, an **Add Instance** window will pop up.

The screenshot shows the 'Add Instance' dialog box with the following fields and values:

Field	Value
Library	NCSU_Analog_Parts
Cell	nmos4
View	symbol
Names	
Array Rows	1
Array Columns	1
Model name	ami06N
Model Type	system (selected), user
Multiplier	1
Fingers	1
Width (grid units)	10
Width	1.5u M
Width (minimum)	1.5u M
Length (grid units)	4
Length	600n M
Length (minimum)	600n M
Drain diffusion area	2.25e-12
Source diffusion area	2.25e-12
Drain diffusion perimeter	6u M
Source diffusion perimeter	6u M

Generally, we would enter the W/L values in the **Width** and **Length** fields.

The simulator will calculate the values in the other fields like Width/Length Grid Units, Source/Drain Diffusion area/perimeter.

The multiplier 'M' gives us the option of adding 'M' transistors of size W/L in parallel.

Selecting a PMOS transistor is similar, but in the library **NCSU_Analog_Parts**, choose **P_Transistors** in the menu below. This will lead to a sub-menu where you choose **pmos4**.

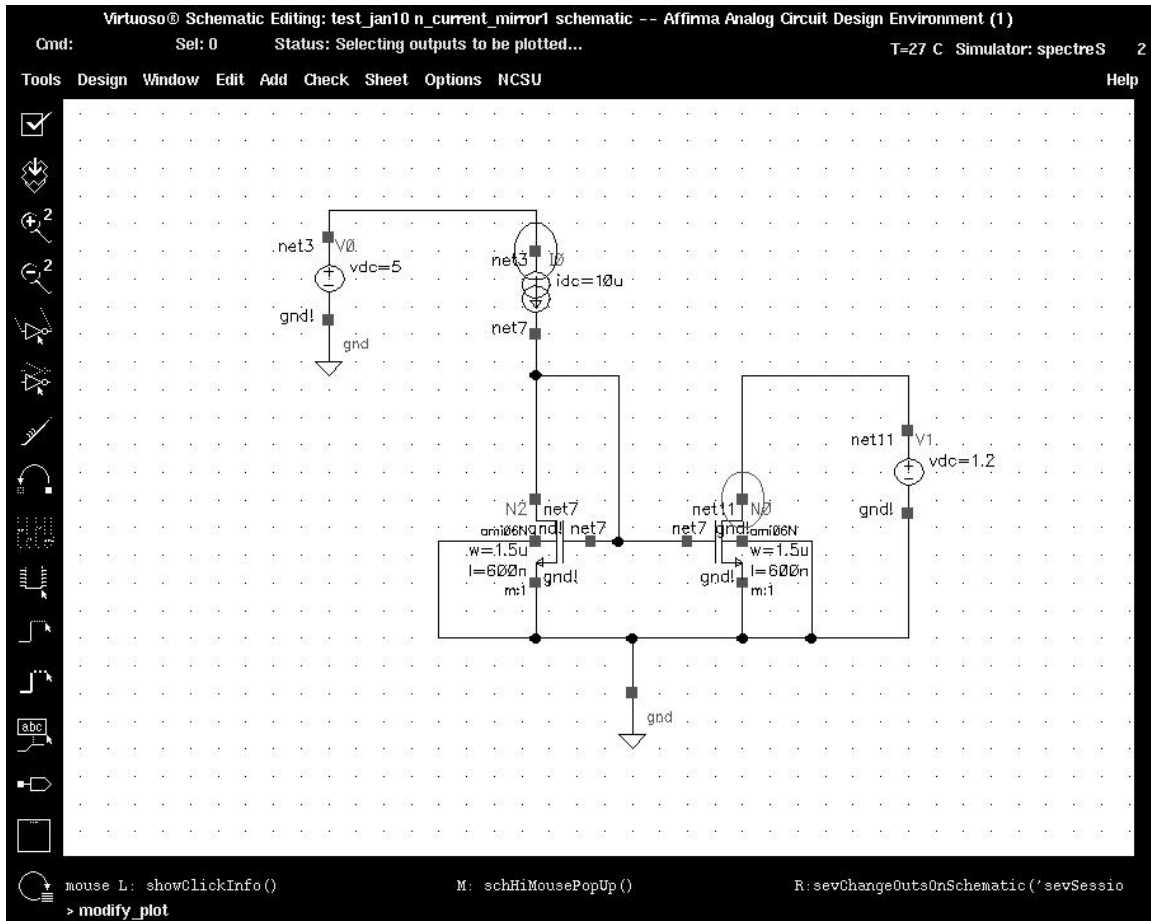
The body/well of a PMOS device can be set to any potential, unlike that of an NMOS device. In most cases, the well potential will be set to Vdd.

Instance for Current Source:

Select **NCSU_Analog_Parts** library and choose **Current_Sources** from the menu below. This will lead to a sub-menu where you would choose **idc**.

NMOS current mirror in Virtuoso Schematic Editor:

Your schematic should be similar to the one shown in the figure below:



You will have to access the properties of Q2 to change settings as per the problem.

Note: In Problems 2 and 3 of CAD Assignment 1, you are not asked to create a symbol for the basic current mirror circuit and then to create a new schematic for testing the circuit. Thus, you can build and test the circuit in the same schematic as shown above.

Selecting currents to be plotted:

In the tutorial, you always selected voltages at different nodes to be plotted. In this problem, you need to observe the currents coming into or going out of a node. For this, once you have selected **Outputs → To Be Plotted → Select on Schematic** from the **Affirma Analog Circuit Design Environment**, you click on the terminal where you want to observe the current. If selected properly, a circle will appear around that terminal as seen in the above schematic.

Design		Analyses			
Library	test_jan10	#	Type	Arguments.....	Enable
Cell	n_current_mirror1	1	tran	0 10u	yes
View	schematic	2	dc	0 5 100m..	yes

Design Variables			Outputs					
#	Name	Value	#	Name/Signal/Expr	Value	Plot	Save	March
			1	IO/PLUS		yes	no	no
			2	NO/D		yes	no	no

> Select on Schematic Outputs to Be Plotted

When you run the simulation having current waveforms to be plotted, the following Warning may appear:

Warning

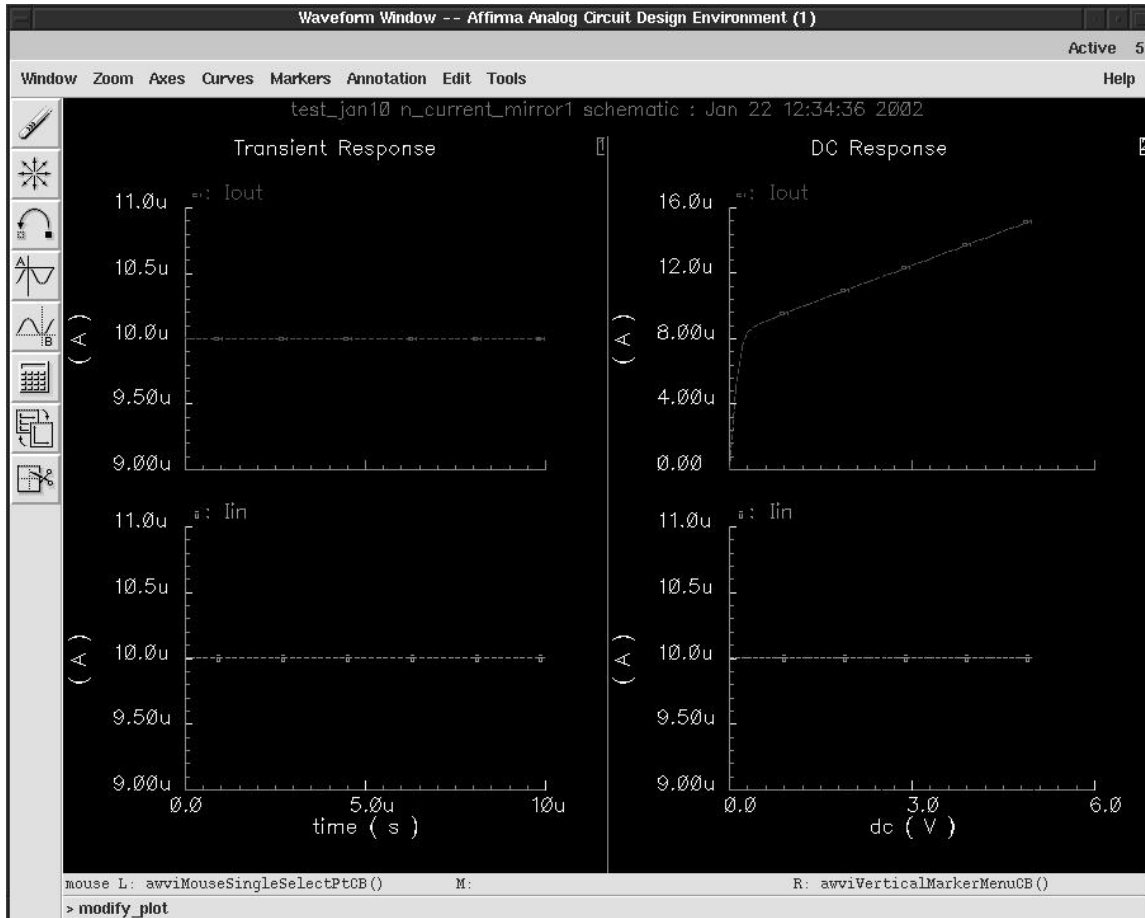
Some outputs to be plotted will not be saved.
Add them automatically to the outputs to be saved before simulating?

Yes No Cancel Help

In that case, just click on **Yes** and proceed.

Output waveforms for the NMOS Current mirror:

Your output waveforms for the transient and DC analyses will look something like this:



Note: I have plotted waveforms from both analyses simultaneously.