Op-Amp Simulation
EE/CS 5720/6720

- Read Chapter 5 in Johns & Martin before you begin this assignment.

This assignment will take you through the simulation and basic characterization of a simple operational amplifier (“op amp”). Turn in a copy of this assignment with answers in the appropriate blanks, and Cadence printouts attached. All problems to be turned in are marked in boldface.

A word on dual-polarity power supplies

While most digital circuits use a single-polarity power supply (e.g., $V_{DD}$ and ground), many analog circuits – especially op amps – are powered by a dual-polarity power supply (e.g., $V_{DD}$, $V_{SS}$, and ground). By convention, $V_{DD}$ is positive relative to ground (e.g., +2.5V) and $V_{SS}$ is negative relative to ground (e.g., -2.5V). The use of dual-polarity power supplies allows us to center ac signals at ground and build circuits capable of generating signals that swing above and below ground by a few volts.

At first glance, it appears that negative power supplies are a bad idea for CMOS circuits, since the source-substrate and drain-substrate $p$-$n$ junctions must remain reverse biased at all times. However, there is an easy solution to this problem: Tie the substrate to $V_{SS}$ instead of ground. The rule we must always obey is this: Always tie substrate to the most negative voltage in the circuit.

For the problems presented below, we will power our op amp with a dual-polarity ±2.5V power supply, and center most of our signals around ground (zero volts). If you get confused by negative voltages, you can think of the substrate being at zero volts, “ground” being +2.5V, and “$V_{DD}$” being +5.0V.

Remember, when using dual-polarity power supplies in simulation, always tie the bodies of all $n$MOS transistors to $V_{SS}$, not ground!

1. Basic op amp simulation

In the Cadence simulation environment, construct the two-stage op amp circuit shown below. (Note that this circuit is very similar to Figure 5.4 in Johns & Martin.) Make all transistors in the circuit have $W = 99\mu m$ and $L = 1.2\mu m$. The bodies (wells) of all $p$MOS transistors are connected to $V_{DD}$.

Note: Why are we using a width of 99µm instead of a nice round number like 100µm? Because the Cadence technology file we are using only allows us to enter widths that are integer multiples of the minimum transistor width (which is 1.5µm in this technology) and lengths that are integer multiples of the minimum transistors length (which is 0.6µm
in this technology). This is a strange rule, and not the standard way things are done, but it’s not a serious limitation.

Use an ideal dc current source to provide the reference bias current, as shown above. In a real circuit, we would build a bias generator circuit to create this reference current (this is covered on pp. 248-250 of Johns & Martin), but there is no point in complicating our design at this point; we only want to focus on the op amp. Set the reference current to 100µA.

You may wish to create a symbol for the op amp so you can insert the circuit hierarchically into other cells where you add inputs, loads, power supplies, etc.

Use two dc voltage sources to provide the power supply voltages $V_{DD} = +2.5V$ and $V_{SS} = -2.5V$.

**Turn in a plot of the op amp schematic.**

2. **Loading the op amp**

In any real circuit, our op amp’s output will drive some other circuit or instrument either on-chip or off-chip. The addition of another circuit (or just an oscilloscope probe) will load the op amp with some capacitance and resistance. We can represent this in simulation by adding a resistor and capacitor in parallel to the op amp output as shown below.
If we are driving the gate of a CMOS transistor (a typical on-chip load), the load is purely capacitive, and we can leave out the load resistor. The capacitance can be computed based on the gate area of the transistor being driven.

The most common off-chip load (for circuit designers and testers) is an oscilloscope probe. Typical oscilloscope inputs have an input resistance of 1MΩ and an input capacitance of 15pF. In addition to the oscilloscope capacitance, basic packaging and cables add additional capacitance. If our chip is packaged in a standard DIP (Dual-Inline Package) ceramic package, the packaging alone will add 1-4pF to any on-chip node connected to a pin. If we plug our chip into a breadboard for testing, the breadboard may add 1-2pF of additional capacitance to each pin. The coaxial “BNC” cables we use to connect the chip to an oscilloscope add even more capacitance. Standard coax cables have a capacitance of about 30pF/foot (about 100pF/meter). We can decrease the loading effect of the oscilloscope by using a “10× probe”, which increases the input resistance by a factor of 10 to 10MΩ. In theory, the input capacitance is decreased by a factor of 10, but in practice it remains close to 15pF (but at least we don’t add the extra capacitance of a coaxial cable!).

For all of our simulations below, let’s use a load of \( R_L = 1 \text{MΩ} \) and \( C_L = 30 \text{pF} \). This approximates the loading caused by typical packaging and a typical oscilloscope with cables. A common mistake among novice chip designers is to simulate circuits with no loading and then be surprised when the chip is manufactured and the measured results don’t match the simulations due to the loading caused by packaging and measurement devices.

(There is nothing to turn in from this part.)

3. Unity-gain buffer; input common-mode range

Let’s check to see if our op amp can function as a basic unity-gain buffer. Connect the negative input to the output, and apply a sine wave (1V amplitude, 1kHz, centered at ground) to the positive input. Run a transient simulation that captures 2-3 complete cycles of the sine wave, and plot the input and output waveforms. The output should follow the input closely. Turn in this plot.

Now let’s measure the op amp’s input common-mode range. Ideally, an op amp should work the same regardless of the dc levels of the input voltages; only the difference in voltages between the two inputs should affect the output. Of course, real circuits never behave this well. With the op amp still configured as a unity-gain buffer, run a dc simulation where the input voltage is swept from -2.5V to +2.5V. Plot \( v_{OUT} \) vs. \( v_{IN} \) and
determine the input common-mode range – the range of input voltage where the circuit has a gain of approximately one. **Turn in this plot.**

**The input common-mode range of this op amp extends from _________ to ___________.**

(Don’t forget to include appropriate units in all answers.)

4. **Open-loop gain measurement**

Let’s measure the open-loop gain of our op amp. Tie the negative input of the op amp to ground, and connect a dc voltage source to the positive input terminal as shown below. We will perform a dc sweep of this input voltage while observing the output node.

![Op Amp Circuit Diagram]

First, sweep the input voltage source from -2.5V to +2.5V. You will see the output voltage swing between its minimum and maximum values.

**The output voltage range of this op amp extends from ___________ to ___________.**

Next, concentrate your input voltage sweep over a very small voltage range so that you zoom in on the “interesting” part of the output voltage curve – the quick transition from minimum to maximum output. You should use enough points in your simulation to observe this transition region in great detail. (For example, don’t just step from -10mV to +10mV in 2mV increments. Use increments at least 100 times smaller than your total sweep range so that you get many points in your graph. Don’t skimp on data; computers are fast nowadays.) The -10mV to +10mV range is just an example. You will probably need to use a smaller range than this to see the slope clearly.

From this graph, you can measure two important characteristics of op amps:

a. **Input offset voltage.** In other words, what does the differential input voltage have to be in order to make the output voltage equal zero? Ideally, the answer should be zero.

   **What is the input offset voltage for this op amp? _______________.**

b. **Open-loop gain.** Estimate the slope of the linear region of your plot of \( v_{OUT} \) vs. \( v_{IN} \). This is the open-loop gain.

   **What is the open-loop gain of this op amp? _______________.**

   Hint: It should be greater than 1000.

   **Now express this gain in terms of dB: _______________.**
5. Transfer function and phase margin

The input offset voltage measured in the previous problem is very useful for the measurements we are about to make. For these measurements, we want the dc level of $v_{OUT}$ to be very close to zero, since this is the typical value the output will have in closed-loop circuits, assuming the input is centered around ground. However, we need to make our measurements in the open-loop condition, so we have to “balance” our high-gain op amp very carefully to keep $V_{OUT} \approx 0$. We do this by adding a dc voltage source $V_{OS}$ in series with one of the inputs. This voltage source is set to the input offset voltage so that if no other signal is present, the output voltage will be approximately zero. (We’ll never make the output exactly zero volts, but as long as we’re within 100mV of zero, that’s fine for these simulations.)

Add a dc voltage source $V_{OS}$ to the positive input of the op amp. Run a dc simulation to verify that $V_{OUT}$ is within 100mV of ground.

![Op Amp Diagram](attachment:opamp_diagram.png)

You are now ready to measure the open-loop gain and phase of the op amp as a function of frequency (i.e., the op amp transfer function). Add an ac voltage source to the positive input terminal of the op amp (in series with $V_{OS}$). We’re going to sweep the frequency of this input voltage and then measure the amplitude and phase of the output voltage. What should the amplitude of this input voltage be? You might think that we would have to keep the input voltage amplitude very small. After all, the open-loop gain of our op amp is very high, so a large voltage at the input would surely saturate the output at the limits you measured in a previous problem.

Actually, since we are going to perform an ac simulation, it doesn’t matter what the amplitude is. When you perform an ac simulation, the simulator first calculates the dc operating point (with all ac sources set to zero), which is why it’s important to set $V_{OS}$ correctly. From the dc operating point, the simulation constructs a linear, small-signal model of the circuit, just as you have done in homework problems. Since this small-signal circuit is linear, it doesn’t matter what the ac voltages are. If the op amp has a gain of 5,000 (for example), you could put in an ac signal with an amplitude of 2V, and the simulation would tell you that the output is a sine wave of amplitude 10,000V. This is completely unrealistic, of course, but that’s the way ac simulation works. Transient simulation is much more “realistic” since it doesn’t linearize the circuit, but it’s not the most convenient way to measure transfer functions. Indeed, the entire concept of a transfer function assumes that your circuit behaves linearly so that if you put a sine wave in, you get a sine wave out, and only the amplitude and phase have changed.

To measure transfer functions, we need to plot $V_{OUT}(s)/V_{IN}(s)$. If we make $v_{IN}$ have an amplitude of 1V and zero phase, $V_{OUT}(s)/V_{IN}(s) = V_{OUT}(s)$, which makes the post-
processing of the data a bit easier. I recommend taking this approach. Just remember
that you’re applying this “large” 1V signal to the linearized version of the circuit, so
don’t worry about absolute amplitudes.

Plot the gain (in dB) and phase (in degrees) transfer function of the op amp over the
frequency range 100Hz – 100MHz. Plot at least 50 points per decade of frequency for
good resolution. **Turn in this plot.**

**The low-frequency gain of the op amp is ________________.**

**Does this agree with the open-loop gain measured in problem 4? ________________
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What is the **phase margin** of the amplifier? To measure the phase margin, find the unity-
gain frequency of the amplifier (the frequency at which the gain drops to one, or 0 dB).
Now find the phase at this frequency. The phase margin equals 180° plus the phase at the
unity gain frequency. For example, if the gain drops to 0 dB at 3MHz, and the phase at
3MHz is -150°, then the phase margin is +30°. If the gain drops to 0 dB at 5MHz, and
the phase at 5MHz is -190°, then the phase margin is -10°. Graphically, the phase margin
is the distance between the phase and the -180° line, where phases above this line are
reported as positive numbers.

**Note:** Don’t be fooled if the phase plot suddenly jumps from -180° to +180°. Most
simulations restrict phase angles within this range, since -181° is mathematically
equivalent to +179°. However, for measuring phase margin, you should “unwrap” the
phase for your calculations. In other words, if the phase has just jumped from -180° to
+180°, begin subtracting 360° from the phase angle to preserve the continuity of the
phase lag vs. frequency. Real circuits exhibit smooth, continuous phase changes with
frequency. The sudden 360° “jumps” are a numerical artifact.

**The unity-gain frequency of the op amp is ________________.**

**The phase margin of the op amp is ________________.**

6. **Amplifier Compensation – Part I**

(Read Section 5.2 in Johns & Martin if you have not already done so.)

If the phase margin of an op amp is less than zero, it will be unstable in closed-loop
situations. (This means it will be a pretty useless op amp.) This is because giving a sine
wave a phase shift of 180° is equivalent to multiplying it by -1. This turns nice, stable
negative feedback into bad, unstable positive feedback. Positive feedback causes a
system to oscillate or “blow up” (hit to power supply rails) if the loop gain of the system
is one or greater. If the loop gain is less than one, positive feedback may cause a bit of
oscillation, but this oscillation will be damped, and the system will settle to a stable point.

A phase margin of exactly zero means that the loop gain (in the unity-gain situation
where the output is fed back directly to the input) reaches unity *exactly* when the phase
lag reaches the “dangerous” 180° mark. This is marginally stable, but no one would ever
design a circuit this close to instability. Most circuit designers try to design for phase
margins of between $+60^\circ$ and $+75^\circ$ so that the circuit will remain stable in the face of temperature changes or processing inaccuracies. The process of modifying an amplifier to improve its phase margin is called compensation.

We are going to add a Miller compensation capacitor $C_C$ (see Sedra & Smith pp. 613-615, and Johns & Martin p. 226) to create a dominant pole in our amplifier and improve its phase margin. Hint: Try capacitor values between 1pF and 500pF. (Note that adding a capacitor has no effect on the dc operating point of the circuit, so we don’t have to compute a new value for $V_{OS}$ to keep the output near zero volts. If we had changed some other aspect of the circuit to improve phase margin, like the bias current or some of the transistor sizes, we would have to run a new dc simulation to find the new value for $V_{OS}$ before re-running the ac simulation.)

![Circuit Diagram]

The op amp achieves a phase margin of $+20^\circ$ with $C_C =$ ________________.

The op amp achieves a phase margin of $+60^\circ$ with $C_C =$ ________________.

Now configure the op amp as a unity-gain buffer (as in problem 3) and run a transient simulation with a square wave input (amplitude = 5mV, period = 2µs, dc level = 0) for both cases: phase margin = $+20^\circ$ and phase margin = $+60^\circ$. Show 2-3 cycles of the input and output waveforms in each simulation. (Use a “pulse” voltage source to create a square wave.) Turn in both plots (labeled).

What is the effect of low phase margin on the transient response?

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7. Amplifier Compensation – Part II

We will now use a technique called lead compensation (see Johns & Martin, pp. 242-246) to improve the phase margin of our op amp while limiting the compensation capacitor to a reasonable size. Configure the op amp as in the first part of the previous
problem, but set $C_C = 5\text{pF}$ initially. Follow steps 1-6 on Johns & Martin, pp. 243-244, adding a resistor $R_C$ in series with $C_C$ (step 4), then replacing it with an $n$MOS transistor in step 6 (i.e., $Q_{16}$ in Johns & Martin, Figure 5.7). Tie the gate of the $n$MOS transistor to $V_{DD}$. The value of $\mu_nC_{ox}$ in this process is approximately $115\mu\text{A/V}^2$, and $V_{tn0} = 0.73\text{V}$. You should limit transistor widths to no less than $1.8\mu\text{m}$ and transistor lengths to no less than $1.2\mu\text{m}$.

Final compensation network: $C_C = \underline{\phantom{115\mu\text{A/V}^2}}, R_C = \underline{\phantom{115\mu\text{A/V}^2}}$.

Using $Q_{16}$ in place of $R_C$: $W_{16} = \underline{\phantom{115\mu\text{A/V}^2}}, L_{16} = \underline{\phantom{115\mu\text{A/V}^2}}$.

Phase margin = \underline{\phantom{115\mu\text{A/V}^2}}

Turn in a plot of the transfer function: gain (in dB) and phase (in degrees)

As in the previous problem, configure the op amp as a unity-gain buffer and run a transient simulation with a square wave input (amplitude = $5\text{mV}$, period = $2\mu\text{s}$, dc level = $0$). Show 2-3 cycles of the input and output waveforms in each simulation. Turn in this plot.

8. Power dissipation

Configure the op amp as a unity-gain buffer (as in problem 3) and set the input to ground. Measure the dc current from $V_{DD}$ ($I_{DD}$) and from $V_{SS}$ ($I_{SS}$). The total power dissipation is given by

$$P = |V_{DD}I_{DD}| + |V_{SS}I_{SS}|$$

The power dissipation of this amplifier is \underline{\phantom{115\mu\text{A/V}^2}}.

(Include appropriate units in this and all other answers.)