EE 5720/6720 Process Parameters

For all the Cadence-based assignments and projects in the class, you will be designing circuits in a 0.5µm CMOS process. This means that the minimum allowable transistor gate length is 0.5µm. We will be designing circuit layout using lambda rules, similar to those discussed in Chapter 2 of Johns & Martin. This means that all design rules (e.g., minimum widths of certain layers, minimum spacing between certain layers, etc.) are integer multiples of lambda (λ), a unit measure of distance. By convention, the minimum gate length in a process is 2λ. In other words, we will be working at a resolution of half the minimum gate length.

You might think that lambda for a 0.5µm process would be 0.25µm, but our rules use λ = 0.3µm, so in practice the shortest transistor we can actually draw has L = 0.6µm.

Our Cadence configuration also includes Spice-based simulation models the particular 0.5µm CMOS process we are using – one manufactured by Idaho/Utah-based AMI Semiconductor (www.amis.com) and commonly available through the MOSIS fabrication service (www.mosis.com).

For some of the projects you will undertake in the class, it will be useful to have a list of "first-order" model parameters for the transistors manufactured in this process. Modern Spice simulation files contain dozens or hundreds of parameters, and are far too complex and detailed to be useful for the type of hand calculations used by engineers *designing* circuits. Below is a list of useful parameters for this process:

<u>*n*MOS transistors</u>

$V_{tn0} = 0.73\text{V}$

$\mu_n C_{ox} = 115\mu\text{A/V}^2$

$\gamma_n = 0.47\ \text{V}^{1/2}$

<u>*p*MOS transistors</u>

$V_{tp0} = -0.94\text{V}$

$\mu_p C_{ox} = 37\mu\text{A/V}^2$

$\gamma_p = 0.58\ \text{V}^{1/2}$

<u>Gate capacitance (both *n*MOS and *p*MOS)</u>

$C_{ox} = 2.4\text{fF}/\mu\text{m}^2$

<u>Poly/Poly2 capacitance</u>

$C_{p1p2} = 0.90\text{fF}/\mu\text{m}^2$