Last class: → Low Noise Amplifiers
- Short input resistor
- Short-series amplifier (feedback)
- common-gate amplifier
- common-source with inductive source degeneration.

LNA Design Procedure

- Last class we identified the common-source amplifier as yielding the best noise performance.

- Now we will discuss how to size the transistor.

- Technique we will discuss is called "power-constrained noise optimization" for a given power budget, how do we size the transistor to achieve the best possible noise performance?

- Involve a somewhat lengthy derivation, we will just outline the most important elements of it here.
  - back analysis is taken from a paper:
  - back analysis is confusing because a number of steps are not described.
  - For a good understanding of it read the paper.

- First let us outline the basic premise of the optimization procedure:
  - consider the small signal noise model for the LNA:

\[
\begin{align*}
E_{\text{in}} & \rightarrow \text{L}_{3} \rightarrow \text{G}_{\text{m}} \rightarrow \text{C}_{\text{s}} \rightarrow \text{G}_{\text{os}} \rightarrow \text{L}_{\text{in}} \frac{1}{\text{L}_{3}}
\end{align*}
\]

- We neglect noise contribution from the inductors (assume ideal components)

- Initially neglect the induced gate noise \( \text{i}_{\text{ng}} \)

- series \( Q_{\text{s}} \) of the resonant input circuit is

\[
Q_{\text{s}} = \frac{1}{\text{W}(\text{bulk}+\text{L})}
\]

- Recall that the effective transconductance is given by

\[
\text{g}_{\text{m}} = Q_{\text{s}} \cdot \text{g}_{\text{m}}
\]
- So, gain is given by: $A = -\frac{Q_0 \cdot g_m \cdot Z_L}{\text{load impedance}}$

- For small transistor widths, $C_{gs}$ will be reduced, so $Q_0$ will increase.
- $g_m$ must be increased to maintain some resonant frequency.
- $g_m$ will also be reduced (assuming constant bias current).

> BUT... recall that drain noise $I_{dn} = 4kT \cdot g_m \cdot \Delta f$, so as transistor is made smaller, $g_m$ is reduced, reducing the drain noise at the output and improving the noise figure.

- This leads us to believe we should size the transistor as small as possible.

- Now let's include the induced gate noise in the analysis.

- As the device size is reduced, $L_g$ is increased ($L_s$ is fixed for input match), impedance at gate node increases.
- More noise appears due to $I_{ns}$. $I_{ns}$ appears at the output.
- At some point this will overwhelm the O/P noise due to $I_{dn}$.

- This implies that there is some optimum $Q_0$ that will balance the output noise due to $I_{ns}$. The goal is to find $Q_0$.

- Since $Q_0 = \frac{1}{4 L_s C_{gs}}$, find $Q_0$ to minimize the NF.

- This sums up the essence of this strategy, now we will give a rough outline of the derivation.

- It can be shown that the noise factor for this circuit can be expressed as:

$$ F = 1 + \frac{1}{\alpha \cdot Q_0} \left( \frac{G_m}{G_{ds}} \right) $$

- Complicated expression that depends on $C_s, S, F$, etc.

- We want like to reformulate this so that the power consumption shows up explicitly.

- Definitions:

  - Bias current can be expressed as:

  $$ I_D = W \cdot L \cdot V_{DSAT} \cdot \frac{V_{DSAT}^2}{V_{DSAT} + L \cdot V_{DSAT}} $$

  - Drive voltage: $V_D = V_{DSAT} \cdot V_T$

  - Saturation velocity: $V_{SAT}$

  - Velocity saturation electric field strength

- This expression is based on fact that for a short channel device, the saturation current is reached not when the channel pinches off, but when the carrier velocity saturates.
From this expression we can express the trans-conductance as:

\[ g_m = \frac{2I_D}{\partial V_{G_S}} = \frac{W \cdot L \cdot C_{ox} \cdot V_{dd} \cdot \frac{1}{L} \cdot \frac{1 + P \rho}{(1 + P \rho)^2}}{I_{E_{sat}}} \]

We can now express the power consumption of the amplifier as:

\[ P_D = I_D \cdot V_{dd} = V_{dd} \cdot W \cdot L \cdot C_{ox} 
\frac{V_{dd} \cdot V_{dd} - V_{dd} \cdot V_{dd}}{V_{dd} + L \cdot E_{sat}} \]

We can now relate \( Q_S \) to power consumption, using the fact that \( Q_S = \frac{1}{W_0 \cdot A_{g_S}} \) and \( C_{gs} = \frac{2}{3} W \cdot L \cdot C_{ox} \):

\[ Q_S = \frac{P_o}{P_0} \cdot \frac{P_o}{1 + P} \]

where \( P_o = \frac{3}{2} \cdot W_0 \cdot V_{dd} \cdot V_{dd} \cdot E_{sat} \)

\( P_o \) being some impedance constant for our purposes.

We can now express the noise factor in terms of the power dissipation and overdrive voltage:

\[ F = 1 + \frac{V_{dd}}{2} \cdot W_0 \cdot V_{dd} \cdot P \left( P_0, P_o \right) \]

where \( P \) is the ratio of 2 sixth order polynomials (nasty!!)

Now, we would like to minimize \( F \) for a fixed power dissipation \( P_o \)

\[ \frac{\partial F}{\partial P} \bigg|_{P_o} = 0 \]

solve for \( P_o \) (assume \( P < 1 \) to enable a closed form solution).

We get an expression for \( P_o \) which is proportional to \( P_o \).

When we sub back into the expression for \( Q_S \), we get:

\[ Q_{S, opt} = 1C \sqrt{5 \frac{1}{8}} \left[ 1 + \left( 1 + \frac{3}{1C^2} \left( 1 + \frac{d}{5A} \right) \right) \right] \approx 3.9 \]

for typical process values.

Pictorially, what we have done is:

- Finding \( P_o \):

- Finding \( Q_{S, opt} \):

\[ \frac{2AB}{3AB} \frac{4AB}{5AB} \]

\[ \frac{2\text{dB}}{3\text{dB}} \frac{4\text{dB}}{5\text{dB}} \]

\[ \frac{2\text{nw}}{4\text{nw}} \frac{6\text{nw}}{8\text{nw}} \]
Note that $Q_{opt}$ is not dependent on $P_0$ or $W_0$, but is fixed for a given process.

Now, since we know $Q_s = \frac{1}{2WPC_{gs}}$, and $C_{gs} = \frac{2}{3}WLC_{ox}$, we can find:

$$W_{opt} = \frac{3}{2}\frac{1}{W_0LC_{ox}R_3 \cdot Q_{opt}} \approx \frac{1}{3W_0LC_{ox}R_3}$$

So, this tells us how to size the drive transistor for a fixed power consumption to optimize noise performance—i.e., a bit counter-intuitive, that it does not actually depend on the power consumption, but that is how the math works out.

Since a number of simplifying assumptions have been made in deriving this result, it is a good idea to use this as a starting point and then use simulations to verify the sizing (i.e., parametric sweep).

**Design Example**

- Design an LNA to operate at 1.59 GHz.
- Use 0.5 μm process with $L_{eff} = 0.35 \mu m$, $C_{ox} = 3.8 \text{ nF/m}^2$, $I_{bias} = 5 \text{ mA}$.
- Assume it is driven by a 50Ω impedance.

1. **Choose an architecture**
   - Common source with inductive degeneration & cascade.

2. **Cascade is used to increase isolation**
   - $C_{gs}$ of transistor M1 introduced feedback which can lead to instability.
   - M2 reduces $S_{12}$ (reduce isolation), mitigating this effect.

3. M3 forms a current mirror with M1, setting the bias current.
   - $C_B$ and $R_B$ are blocking components which enable this.
   - M3 is sized as a fraction of M1 (replicate) to minimize power consumption.
2. Size Transistors

- Using power constrained noise optimization, for M1:

\[ W_{opt} = \frac{1}{3 \cdot W \cdot L \cdot C_{ox} \cdot R_s} = \frac{1}{3 \cdot 2 \cdot 1.5 \cdot 10^{-9} \cdot 0.35 \cdot 6 \cdot 3.3 \cdot 3.5} \approx 500 \, \mu \text{m} \]

- Choose \( W_{M3} = \frac{W_{M1}}{10} \) (somewhat arbitrary)

- Choose \( W_{M2} = W_{M1} \)
  - Two competing effects here:
    1. Want \( W_{M2} \) large to increase its \( G_m \), reducing the impedance at the drain of \( M1 \), reducing the signal swing there.
       - reduces feedback, as discussed
       - reduces Miller effect which causes input impedance (\( W_{L1} \)) to deviate from the expected value (calculated while neglecting \( G_m \)).
    2. Larger \( M2 \) increases the parasitic capacitance at \( M1 \) drain. \( M2 \) source
       - as seen in previous HW question, this leads to a degradation in the NF.

- Choosing \( W_{M1} = W_{M2} \) is convenient for layout, as \( M1 \) drain/\( M2 \) source can be combined.

3. Size Inductors for input match

- Find \( W_L \) for particular bias current.
  - through simulation, or estimate as \( W_L = \frac{g_m}{g_s} \)
  - Assume \( W_L = 3.5 \times 10^6 \, \text{rad/s} \)

- Find \( L_s \):
  \[ W_L \cdot L_s = 50 \Rightarrow L_s = 1.4 \, \text{nH} \]

- Find \( L_g \): need to resonate at \( C_g \) at 1.59 GHz.
  \[ L_g = \frac{1}{(2 \pi \cdot f)^2 \cdot C_g} \]
  \[ L_g = \frac{1}{(2 \pi \cdot 1.59 \times 10^9)^2 \cdot 0.5 \, \text{pF}} \]
  
  - Assume \( C_g = 0.5 \, \text{pF} \) (from process file or simulation)
  \[ L_g = 18.6 \, \text{nH} \]

4. Size Output Load

- Need to choose \( L_d \) to resonate with total capacitance at drain of \( M2 \).
  - Parasitic capacitance of \( M2 \) (from simulation), load capacitor \( C_L \)
  - (to sweep parasitics), and capacitive loading of next stage (for us, a mixer).
\[ C_{to} = 5 \ \mu F, \quad \text{then} \quad W_0 = \frac{1}{\sqrt{C_{to} L_0}} \implies L_0 = 2 \ \text{mH} \]

5. Sizing biasing components

- \( C_B \) needs to appear as a short at frequencies of interest.
  - Larger: more area consumption, more parasitic capacitance to ground (substrate).
  - Smaller: signal attenuation (gain reduction) through series voltage divider.

Metal-Insulator-Metal (MIM) Capacitor:

- \( R_B \) needs to be large enough to appear as an open circuit to the small signal.
  - Larger: more area consumption, settling time of bias.
  - Smaller: signal attenuation (gain reduction), increased noise contribution (alignment question).

- Choose \( C_B = 30 \ \mu F, \ R_B = 2 \ \text{K}\Omega \)

Parametric simulations are useful for evaluating these choices.

- Finally, choose \( R_{\text{ref}} \) to set desired current in M3.

6. Simulate

- All these first cut design choices must be evaluated and optimized through simulation.

- Can be time consuming.

- In a real design, these optimization simulations must be redone to adjust values (particularly passives) after layout and extraction.