Oscillator Topologies

1. One Transistor Topologies

- Consider a MOS transistor with an LC load.

\[ \text{From Barkhausen, we know that we need feedback with } \theta = 0 \degree \text{ of phase shift around the loop.} \]

- At resonance, LC tank provides no phase shift.

- Apply feedback to the gate?

  \[ \begin{align*}
  &\text{(a)} \quad \text{V} \text{out} = C \text{V} \text{in} \\
  &\text{(b)} \quad \text{increase in V} \text{out} \text{ leads to increase in I} \text{out} \\
  &\quad \text{this leads to decrease in V} \text{in, which is negative feedback} \\
  &\quad \text{if this is too applied to the gate, it doesn't work.}
  \end{align*} \]

(b) How about the source?

- Decrease in V \text{out} is applied to the source, leading to an increase in Vgs, in phase with the original Vgs increase which also increases Vgs.

  \[ \begin{align*}
  &\text{This is positive feedback, with } 0 \degree \text{ of phase shift, so as long as the loop gain is unity, this will oscillate.}
  \end{align*} \]

- Problem: recall the concept of loaded Q.

  \[ \begin{align*}
  &\text{we want the Q of the tank (parallel resistance at resonance) to be as high as possible} \\
  &\text{impedance looking into the source of a MOSFET is } Vg \text{r} \\
  &\text{this degrades the Q of the tank}
  \end{align*} \]

- We need to transform the Vgs input impedance so that it is a high impedance as seen from the LC tank.

- How about a tapped capacitor network?
- If we assume that the impedance looking into the drain of M1 is high, this is approximately equal to:
  (considering the tank only)

  \[ R = \frac{1}{g_m \left( \frac{C_1 + C_2}{C_1} \right)^2} \]

  \[ C_{eq} = \frac{C_1 C_2}{C_1 + C_2} \]

- So, by appropriate choice of \( C_1 \) and \( C_2 \), we can make the tank see a large \( R \) and achieve a good loaded \( Q \).

- This is called a Colpitts oscillator.

- A similar oscillator can be built using a tapped inductor network.
  This is called a Hartley oscillator.

\[ \text{(2) Negative-} \quad g_m \text{ Oscillator) } \]

- Recall that in the one-port view of oscillators we needed a negative real resistance to cancel out the losses of the LC tank.

- Consider a cross coupled MOS pair:

\[ \Delta I = g_m \Delta V \]

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- For a differential small signal voltage \( \Delta V \):

- Consider the one-sided input impedance:

\[ R = \frac{V}{I} = \frac{-\Delta V}{g_m \Delta V} = -\frac{1}{g_m} \]

- So, now we can use this to compensate the losses of an LC tank, and create an oscillator.

- Many different permutations of this, here is one example:

- This creates an inherently differential topology.

- We can also use additional parasitic pairs on top for more negative \( g_m \).

- To allow tuning, tank can be configured:

\[ \text{here the capacitors are varactors whose capacitance varies with the DC voltage} \]

\[ V_{\text{out}} \]
Inductor in tank is chosen according to desired voltage swing.
Capacitor is chosen to resonate with inductor.
- must also consider tuning range required, as C gets small.
- parasitic capacitances can dominate, reducing tuning range.

- How do we size & bias the transistors?
- Assume inductive losses dominate the tank Q:

\[ C \frac{1}{\tau} \Rightarrow \frac{1}{\frac{1}{R_L} + \frac{R_p}{R_C} + \frac{R_p}{R_L}Q^2} \Rightarrow Q = \frac{1}{R_p} \]

- For resonance, we need \( \frac{1}{R_p} + (-Q_m) = 0 \)  \( \Rightarrow R = \frac{1}{Q_m} = \infty \)

So, \( Q_m = \frac{1}{R_p} = \frac{1}{R_LQ^2} \)  \( \Rightarrow Q = \frac{R_L}{R_p} \frac{1}{Q_m} = \frac{R_L}{R_p} \frac{L}{L_C} \)

- Now, since \( Q_m \) depends on device W/L and bias current, use this constraint to size the transistors.

- In practice, to guarantee start-up, we need \( Q_m > \frac{1}{R_p} \)

- Choosing \( Q_m = \frac{2}{R_p} \) is a typical value.

- Ring Oscillators

- Ring oscillators can be implemented using inverters, leading to a compact design:

- With an odd number of stages we have 180° of phase shift around the loop.
- From Barkhausen, we need 0° (or 360°) for oscillation, so the other 180° comes from the cumulative delay of the inverters.

\[ 180° = N \cdot T_d \]

- 1 period is 360° \( \Rightarrow \) \( f_o = \frac{1}{360°} \)

\[ f_o = \frac{1}{2 \cdot N \cdot T_d} \]
So, choose number of stages according to desired oscillation frequency.

Advantage over LC tank oscillator is compactness due to no inductors.

Disadvantage is higher phase noise (more noisy devices = more phase noise) and higher power consumption (VCC nodes oscillating at 2 as opposed to 1 for a negative-gm LC tank design).

How do we change the frequency?

- Tuning techniques fall into 2 categories: capacitive & resistive.
  - Both operate by changing the RC0 time constant of the node being charged or discharged.

(C) Capacitive methods:

- Limits maximum frequency.

- All is in triode region, acts as a variable resistor. Changing the effective time constant.
  - Kn is not very linear.

(b) Resistive methods:

- Loads operate in triode region, Vout changes their impedance, change time constant at that node.
- Need to make sure gain of the stage stays above unity (Bode Hansen).

- Fixed loads, but adjust the bias current, changing load impedance in that way (Vgm).
- Gain of each stage stays more constant than in the previous technique.
Integrated Inductors

- Fully integrated inductors require inductors to be integrated on the die.
  - Many modern processes have a thick top metal layer to facilitate this.

- Circular or octagonal inductors generally have lower resistance and higher Q.
  - Design parameters:
    - # of turns
    - Diameter
    - Turn spacing
    - Metal width

- If no thick top metal layer is available sometimes the top 2 metal layers will be used and stepped together with vias.

For an RF specific process, fab will provide models based on fitting to characterized inductors.

Otherwise, next most accurate option is to use a E-M field solver, some IC specific tools are available (ASIC)

Alternatively, a number of analytical formulae are available for estimating inductance, see the text for a number of these.

Inductor loss mechanisms:

1. Metal wire resistance
   - Increased at higher frequencies due to skin effect.
   - Need thick metal to minimize this.

2. Capacitive coupling to substrate
   - Capacitive coupling to substrate leads to losses.
   - Worse for more conductive substrates (CMS vs. GaAs).
   - Don't put substrate ties near inductors.

3. Magnetic coupling to substrate
   - Magnetic field leads to eddy currents induced in the substrate, again leading to losses.

Some improvement can be gained through the use of a patterned ground shield.

- Created on metal layer below the inductor.
- Reduces capacitive coupling.
- Broken up to reduce effects of eddy currents (3 above).
Integrated Varactors

- To tune the VCO we need to change the resonant frequency of the tank, \( f_0 = \frac{1}{2\pi \sqrt{LC}} \)
- Most common way is to adjust \( C \) through use of a varactor.

Diode Varactors

- Recall that when a diode is reverse biased, depletion layers form with fixed charge.
- This exhibits some capacitance akin to the parallel plate or \( C \) capacitor.
- As reverse bias increases, depletion layer widens, increasing the plate separation and reducing the capacitance.

- Integrated diode:

- Tuning range of the diode will depend on the grading at the junction.
- Good RF processes will have Hyper-Abrupt Junction Varactors available, with tuning ranges of \( \pm 2.2 \).
- If these are not available, the MOS Varactors are typically used.

MOS Varactors

- We know that a MOS transistor exhibits capacitance between the gate and channel.
- If we connect \( D, S, B \) together, we can create a capacitor:

- When \( V_{SB} < V_T \), an accumulation layer will form, with mobile charge buildup, leading to a capacitance of:
  \[ C_{ox} = \text{Exx} \cdot \frac{A}{L} \]
- When \( V_{SB} > V_T \), an inversion layer will form, with mobile charge and the same capacitance as above.
- In between these operating regions, a depletion layer will be present, with reduced mobile charge and therefore reduced capacitance.
Plotted, this appears as below:

\[
\begin{align*}
V_{GS} & \quad \Rightarrow \quad \text{Linear region} \\
& \quad \Rightarrow \quad \text{Saturation region} \\
& \quad \Rightarrow \quad \text{Active region}
\end{align*}
\]

- Monotonic behaviour for \( V_{GS} > 0 \) can be achieved for a pMOS by inhibiting accumulation by disconnecting the P, S from B and tying B to Vdd.
  - For an nMOS this is the default condition since it is always grounded.
  - This leads to the behaviour shown by the dotted line in the figure above.
- This can also be achieved in the accumulation mode through proper biasing.
- Series resistance of the varactor (and structure Q) changes depending on region of operation.
  - For a pMOS, lower resistance in accumulation, since electrons act as charge carriers, with higher mobility.
  - Q's in excess of 100 can be achieved, far superior to integrated inductors.


**Quadrature Local Oscillators**

- In our discussion of transceiver architectures, we saw that in many cases we require quadrature LOs.
  - We saw that these can be created through R-C C-R filters
  
\[
-\frac{\pi}{4} - 45^\circ \quad 0 \quad +\frac{\pi}{4} +45^\circ
\]

- Or through poly-phase filters (we didn't really talk about these)
- Or through use of a higher freq. LO that is then divided down to provide quadrature outputs.