Last class: VCOs
- noisy control voltage appears as phase noise at output.
- Topologies
  - 1-transistor VCOs (colpitts)
  - negative gm VCOs
  - ring oscillators
  - integrated inductors

resume at arrow on next page.
Integrated Inductors

- Fully integrated receivers require inductors to be integrated on the die.
- Many modern processes have a thick top metal layer to facilitate this.
- Circular or octagonal inductors generally have lower resistance and higher Q.
- Design parameters:
  - Number of turns
  - Diameter
  - Turn spacing
  - Metal width
- If no thick top metal layer is available sometimes the top 2 metal layers will be used and stepped together with vias.

For an RF specific process, EDA will provide models based on fitting to characterized inductors.

Otherwise, the next most accurate option is to use an EM field solver, some IC specific tools are available (ASICs).

Alternatively, a number of analytical formulae are available for estimating inductance, see the key text for a number of these.

Inductor loss mechanisms:

1. Metal wire resistance:
   - Increased at higher frequencies due to skin effect.
   - Need thick metal to minimize this.

2. Capacitive coupling to substrate:
   - Capacitive coupling to substrate leads to losses.
   - Worse for more conductive substrates (CMOS vs. GaAs).
   - Don't put substrate traces near inductors.

3. Magnetic coupling to substrate:
   - Magnetic field leads to eddy currents.
   - Reduce capacitive coupling.
   - Eddy currents in the substrate lead to losses.

Some improvement can be gained through the use of a patterned ground shield:

- Created on metal layer below the inductor.
- Reduces capacitive coupling.
- Broken up to reduce effect of eddy currents (3 above).
Integrate Varactors

To tune the VCO we need to change the resonant frequency of
the tank, \( f_c = \frac{1}{2\pi\sqrt{LC}} \)
- most common way is to adjust C through use of a varactor.

Diode Varactors
-Recall that when a diode is reverse biased, depletion layers form with fixed charge.
-These exhibit some capacitance akin to the parallel plate or C capacitor.
-As reverse bias increases, depletion layer widens, increasing the plate separation and reducing the capacitance.

- Integrated diode:

- Use large blocking capacitance (short at AC) to set the dc bias

- Tuning range of the diode will depend on the grading at the junction,
  with more TR for more abrupt junctions.
- Good RF processes will have Hyper-Abrupt Junction Varactors available, with tuning ranges of \( \pm 2\% \).
- If these are not available, the MOS varactors are typically used.

MOS Varactors
- We know that a MOS transistor exhibits capacitance between the gate and channel.
- If we connect D, S, B together, we can create a capacitor:

PMOS:

- When \( V_{SB} > V_T \), an inversion layer will form with mobile charge
  buildup, leading to a capacitance of:
  \[ C_{ox} = \text{Erm. A} \]
- When \( V_{SB} < V_T \), an accumulation layer will form with mobile charge
  and the same capacitance as above.
- In between these operating regions, a depletion layer will be present, with reduced mobile charge & therefore reduced capacitance.
In our discussion of transceiver architectures, we saw that in many cases we require quadrature LOs.

- We saw that these can be created through R-C-C-R filters
  \[ \frac{1}{45^\circ} \quad \frac{1}{45^\circ} \quad \frac{1}{45^\circ} \quad \frac{1}{45^\circ} \]

- Or through poly-phase filters (we didn't really talk about these)

- Or through use of a higher freq. to that is then divided down to provide quadrature outputs.


Quadrature Local Oscillator

Monotonic behavior for VGS > 0 can be achieved for a pmos by inhibiting accumulation by disconnecting the D, S from B and tying B to VDD.

- For an nmos this is the default condition since it is always grounded.

- This leads to the behavior shown by the dotted line in the figure above.

This can also be achieved in the accumulation mode through proper biasing.

Series resistance of the varactor (and structure Q) changes depending on region of operation.

- For a pmos, lower resistance in accumulation, since electron but as charge carriers, with higher mobility.

- Q's in excess of 100 can be achieved, far superior to integrated inductors.
An alternative is to use a VCO topology that inherently provides quadrate outputs:

- two identical LC oscillators with additional cross coupling transistors M1-M4
- if oscillators are in phase, coupling transistors inhibit oscillation, same for anti-phase
- oscillation can only occur when two oscillators are in quadrature.

Quadrate outputs can also be provided by a ring oscillator with the appropriate # of stages
- must be a differential design (why?)

Tank Loading

- In many cases it is undesirable to load the VCO tank directly since this can degrade the quality factor and also introduce disturbances - phase noise
- In these cases a buffer can be interposed between the tank and what it is driving
  - common source if gain is needed
  - common drain for high freq. and low output impedance
- For the project you probably don’t have to worry about this

Phase-Locked Loops (PLL)

- What is a PLL?
  - a negative feedback system that forces the input & output signals to have a constant phase offset (often 0°).
  - this forces the input & output frequencies to be exactly equal.

Block diagram:

\[ \phi_{in} \rightarrow \text{Phase Detector} \rightarrow \text{Loop Filter} \rightarrow \text{VCO} \rightarrow \phi_{out} \]

\[ \phi_{in} = \phi_{out} \quad \therefore \quad \phi_{in} = \phi_{out} \]

(In the "locked" condition)

Analogy:

- PLL provides a "virtual ground" for the phase.
Uses of PLLs in transceiver:

1. Frequency Demodulation

- If $f_{VCO}$ has a linear relationship between $V_{out}$ and $f_{in}$, we can use this to demodulate an FM signal.

- PLL loop must have sufficient bandwidth to track changes in $f_{in}$.

2. Frequency Synthesis (more relevant for us)

- Now input is a fixed frequency from a clean source (e.g., a crystal); we change the output freq. by inserting a divider in the feedback path.
  - freq. "amplification" in the same way that an op-amp amplifier works.

- $f_{out} = f_{in} \times N$; work backwards to show that $f_{in} = N \times f_{out}$.
- Very $N$ to very fast.

PLL Modeling

- A PLL is basically a feedback system, which we are accustomed to modeling in the $s$-domain. Using Laplace transforms,
  - so, we would like to have $s$-domain models for each of the blocks in the PLL.
  - Can be confusing since we are used to thinking of feedback voltages/currents, but here the variable of interest is phase.
  - Also, the variable of interest changes as we move around the loop.

- Conversion:
  - PD takes phase to voltage.
  - VCO takes voltage to phase.
Now let's create models for each block.

1. Phase Detector: converts difference in phase of the two inputs to a dc voltage with some gain.

   \[ \text{Model as: } V_{pp} = K_{pp} (\phi_1 - \phi_2) \]

   A practical phase detector will have a characteristic that wraps around at some point, since a phase offset of 200° looks the same as a phase offset of 380°.

   - So a phase detector is non-linear, but we can approximate it as being linear when the PLL is locked.

2. Loop Filter: Same as any filter you have already seen, takes input voltage \( V_{in} \) and creates output voltage \( V_{out} \) according to some transfer function.

   \[ \frac{V_{out}(s)}{V_{in}(s)} = F(s) \]

3. VLO: In our prior analysis, we saw that VLO behavior can be modeled as:

   \[ V_{out} = A \cdot \cos \left( \omega_{L1} t + K_{vlo} \int V_{out}(t) \, dt \right) \]

   - We care about the phase of the output, so we want a transfer function from \( V_{out} \) to the phase of the output.
   - We deal with the second of the phase terms (excess phase) since this is the component that can be varied under the influence of the control voltage.

   \[ \phi_{out} = K_{vlo} \int V_{out}(t) \, dt \]

   - Take Laplace transform:

     \[ \Phi_{out}(s) = K_{vlo} \frac{1}{s} \cdot V_{out}(s) \]

     (since \( L\{s\} = \frac{1}{s} \))

     \[ \therefore \Phi_{out}(s) = \frac{K_{vlo}}{s} \]

   - It is important to understand this relationship (questions?)
Divide: (not shown in diagram) \[ \text{fout}(t) = \text{fin}(t) / N \]

- Phase is integral of freq. so integrate both sides:

- Using Laplace:

\[ \frac{\phi_{out}(s)}{\phi_{in}(s)} = \frac{1}{N} \]

Linear PLL Analysis:

- Now we have S-domain models for all of the PLL blocks, so assuming the PLL is locked (so that the PD remains linear), we can substitute model the system dynamics:

\[
\begin{align*}
\phi_{in} & \rightarrow + \phi_{PD} \rightarrow K_{PD} \rightarrow \text{LPF} \rightarrow \frac{1}{N} \text{Divider} \\
\phi_{div} & \rightarrow \phi_{out}
\end{align*}
\]

- We can write the loop transfer function as:

\[ G(s) = \frac{\phi_{out}(s)}{\phi_{in}(s)} = \frac{K_{PD} \cdot K_{VCO} \cdot F(s)}{N \cdot s} \]

- Now, for closed-loop transfer function:

\[ H(s) = \frac{\phi_{out}(s)}{\phi_{in}(s)} = \frac{K_{PD} \cdot K_{VCO} \cdot F(s)}{s + \frac{K_{PD} \cdot K_{VCO} \cdot F(s)}{N}} \]

- The denominator of the closed-loop transfer function is referred to as the "characteristic equation" of the PLL.

- It is also common to express an error transfer function:

\[ E(s) = \frac{\phi_{e}(s)}{\phi_{in}(s)} = 1 - \frac{\phi_{out}}{\phi_{in}} = \frac{s + \frac{K_{PD} \cdot K_{VCO} \cdot F(s)}{N}}{s + \frac{K_{PD} \cdot K_{VCO} \cdot F(s)}{N}} \]

(simpler if \( N = 1 \).)