Phase Detectors

0. Multiplier Phase Detectors

- This is just a mixer, most common is to use a double-balanced mixer.

- Recall that for a mixer, we have:

\[
\text{Out} = A \cos(w_1 t) \cdot B \cos(w_2 t + \Delta \phi)
\]

- For simple constant, \( \frac{1}{2} \) for square wave

\[
= \alpha A B \left\{ \cos \left[ (w_1 + w_2) t + \Delta \phi \right] + \cos \left[ (w_1 - w_2) t + \Delta \phi \right] \right\}
\]

- Filtered out by loop filter

- In locked condition, \( w_1 = w_2 \):

\[
\text{Out} = \alpha A B \cos(\Delta \phi)
\]

- Non-linear PLL gain, but if we assume phase steps around \( \frac{\pi}{2} \), we can approximate behavior as linear.

\[
K_{PD} = \frac{\alpha A B}{2}
\]

- Gain depends on input signal amplitude.

- Good for small or noisy input signals (demodulation)

1. XOR Phase Detector

- If above circuit is driven hard, we get an XOR behavior.

\[
\begin{array}{ccc}
A & B & Y \\
0 & 0 & 0 \\
0 & 1 & 1 \\
1 & 0 & 1 \\
1 & 1 & 0 \\
\end{array}
\]
Draw Waveform: A

B

\[ Y = \text{output is some level of pulse train} \text{ (need low-pass filtering in the loop filter)} \]

- Phase change leads to change in pulse width \( \Rightarrow \) change in dc level.

- Draw phase characteristics:

\[ \Delta \Phi \]

- Linear phase characteristic over range from \( \Delta \Phi = 0 \) to \( \pi \) (better than multiplier).
- Susceptible to change in duty cycle of one of the inputs:

\[ A \quad B \quad \text{Out} \]

\[ \text{Every 2nd pulse is smaller.} \]

\( \theta \)

2-5 Latch Phase Detector

\[ \text{A} \quad \text{B} \quad \text{Out} \quad \text{DS} \quad \text{R} \quad \text{Q} \]

- Also needs a digital input, A sets output high, B resets it low (age): 

\[ \text{Phased Inputs:} \quad A \quad B \]

\[ \text{Out} \]

\[ \text{Phase Characteristic:} \]

\[ \Delta \Phi \]

- All the phase detectors discussed up to this point have an average output of zero if \( w_1 \neq w_2 \).
- How does the PLL acquire lock?
- This modelling has neglected non-linearities which lead to a non-zero output, allowing an (sometimes slow) acquisition.

- It would be nice to have a phase-detector which was also sensitive to a frequency offset, to speed the acquisition process.
- Such a component exists, and has been cleverly named the phase-frequency detector.
Tri-state Phase-Frequency Detector (PFD)

- Non-complementary outputs
- If \( W_A > W_B \), produces pulses at \( UP \)
- If \( W_A < W_B \), produces pulses at \( DN \)
- If \( W_A = W_B \), produces pulses at \( UP \) or \( DN \), depending on phase.

Example wave forms:

- Three different output states:
  - \( UP = DN = 0 \)
  - \( UP = 1 \), \( DN = 0 \)
  - \( UP = 0 \), \( DN = 1 \)

- Can use a state machine to summarize the operation:

From Characteristic:

- Frequency detection occurs when phase accumulates to more than one cycle
- Linear range from \(-2\pi\) to \(2\pi\)

To implement this, we can guess that we will need some storage element:

- Ideally \( UP \) & \( DN \) should never be high simultaneously, but due to delay in the reset path, there will be narrow pulses generated.
- Due to conventional way in which the FFs are used (\( Q \) tied to VDD), simplified topologies can be used.
**Charge-Pump PLLs**

- PMCs are most commonly used with charge pumps, to yield a type II PLL with a passive loop filter. This is the most common type of PLL used for freq. synthesis.

![Charge-Pump PLL Diagram](image)

- When UP is high, I_{up} is driven onto the filter node.
- When DN is high, I_{dn} is pulled off of the filter node.
- C integrates the charge added or removed.

**Waveform:**

![Waveform Diagram](image)

**Brief Analysis:**

- Assume PLL is locked, recall that \( \Phi_c = \Phi_{in} - \Phi_{out} \)

- Duration of current pulse from charge pump can be expressed as \( t_p = \frac{1}{2} \Phi_{el} T \) (where \( T \) is period of reference freq.)

- This is a discrete time system, but if we assume the PLL state is relatively constant over one period, we can look at the time averaged behaviour, and retain our continuous time Laplace analysis.

- Average current over one cycle: \( I_{dc} = \frac{I_{up} \cdot t_p + I_{dn} \cdot (\Phi_{el} T - t_p)}{T} = \frac{I_{up} \cdot \Phi_{el} T}{2\pi} \)

\[ \therefore \text{Phase detector gain is} \quad I_{dc} = \text{charge pump bias current}. \]

- We can substitute this back into our Laplace expressions for loop transfer functions.

- A capacitor will now provide an integration, but as seen previously a pure integration in the loop filter is unstable.

- Add a resistor to give a zero: \( \frac{I_{in}}{R} \cdot \frac{1}{\frac{1}{C_{out}} + \frac{1}{C}} \)

- Add another pole:

\[ \frac{I_{in}}{R} \cdot \frac{1}{C_{out}} \cdot \frac{1}{C_{1}} \cdot \frac{1}{C_{2}} \]
- Need to choose pole freq. to insure stability.
  - Continuous time analysis depends on the assumption that the input (reference) freqency is much greater than the PLL bandwidth.
  - As a general rule, keep B.w. \( \leq \frac{\text{freq}}{10} \), violating this could lead to instability as a result of the discretized operation.

**Charge Pump Implementations**

- **Simple Charge Pump**
  - Subject to charge-sharing from nodes A & B
  - Also charge injection from switches

- **To minimize charge sharing, can use current steering design**:
  - Prevents nodes A & B from accumulating charge
  - Need unity gain buffer
  - "During" transistors can be used to smoothen charge injection.

- **Accurate matching of UP & DN currents is important, as mismatches cause ripple on control voltage line of VCO, which leads to spurs in the output spectrum**

  - As recall process of noise on VCO

  | \( I_{UP} \) | \( V_{ref} \) | \( V_{out} \) |
  |\(--\)| \( \rightleftarrows \) | \( \rightleftarrows \) |

  - Approximate as first harmonic like putting a sinusoidal modulation at first \( f \) on the VCO control voltage.

**Output Spectrum**

- Spurs lead to downconversion of unwanted interferers (Similar to phase noise)
Loop-Filter

- Can be categorized into ones for use with standard P.D. or PFD.
- Can be further categorized into active or passive.
- Many different designs possible, we will just mention a few.

1. For use with standard P.D.

   (a) Passive: low-pass: \( F(s) = \frac{1}{1 + sRC} \)

   (b) Active: - Useful to get an integration for a type II PFD if a PFD/CP is not being used.

     \[ F(s) = \frac{1}{RC} \left( \frac{1 + sR_2C}{s} \right) \]

     - Assumes up-pump has infinite gain at dc.
     - For inverting loop filter need to flip inputs to P.D.

2. For use with Charge-pumps

   (a) Passive: - As mentioned:

     \[ \frac{1}{R} \left( \frac{C_1}{C_2} \right) \]

   (b) Active: - Can be useful to hold C.P. at Vref at a fixed voltage, making it easier to match UP/DN current.

     \[ F(s) = \frac{1 + sR_2(C_2 + C_3)}{C_2(1 + sR_1C_1)} \]

VLO - Already done!

Dividers

- There are many types of freq. dividers, we will cover a couple here.

- Most use digital logic.
  - Simplest is to just implement a counter that counts up (or down) and then resets.
  - Counters can be synchronous or asynchronous.
  - Synchronous are usually preferred for reduced jitter.