Design Considerations:

Using the Rule of Thumb as outlined in the laboratory experiment, VD=Vs=5V. I setup the equations in excel but they can also be setup using Matlab. I am assuming that I measured $V_t = 1V$ and $k_n'\left(\frac{W}{L}\right) = 700\mu\frac{A}{V^2}$. I then used $V_{GS} = V_t + \frac{2(15-V_D)}{gain}$(this equation used the assumption that the load did not alter the gain), $I_D = \frac{1}{2}k_n'\left(\frac{W}{L}\right)(V_{GS}-V_t)^2$, $R_D = \frac{(15-V_D)}{I_D}$ and $R_S = \frac{V_S}{I_D}$. I then found V_G from the V_{GS} value. I selected one value of the RG resistors (just make them larger than 10k) and solved for the other. {NOTE: when measuring in lab, the lab equipment has an internal R of 3Meg on the multimeters so take that into account when measuring the VG value.}

Using these equations in excel resulted in

Gain	VGS	VG	ID	RD	Rs	RG1(top)	RG2(bottom)
101	1.19802	4.19802	1.37E-05	7.29E+05	2.19E+05	5.15E+05	2.00E+05

checking the values of VD, VS, $gain = g_m R_D||R_L$ with RL=10Meg(assuming negligible load) gave

VG	Vs	VD	ID	Gain with RL
6.20E+00	5	5	1.37E-05	9.41E+01

Checking VGS>Vt (YES) and VDS=0>(VGS-Vt)=1.2-1=0.2 (NO!)

To make it into saturation, either VD can be raised or VS lowered. Raising VD=6V and VS=4V:

VG	Vs	VD	ID	Gain with RL
5.18E+00	4	6	1.11E-05	9.34E+01

RD	Rs	RG1(top)	RG2(bottom)
8.10E+05	3.60E+05	3.79E+05	2.00E+05

I also want to check the effects of RL. Changing RL to a lot lower value, RL=10k:

Gain with RL
1.23E+00

This is really bad! Not all is lost though because I know that Mosfet's can have a "high" input resistance so if I cascade another amplifier, the input resistance to that amplifier will be high (which is the load resistance here for this amplifier) and thus will not effect the gain.

Now I can use those values in PSpice as a starting point. Note that PSpice will simulate using a lambda value which was neglected in the hand calculations.

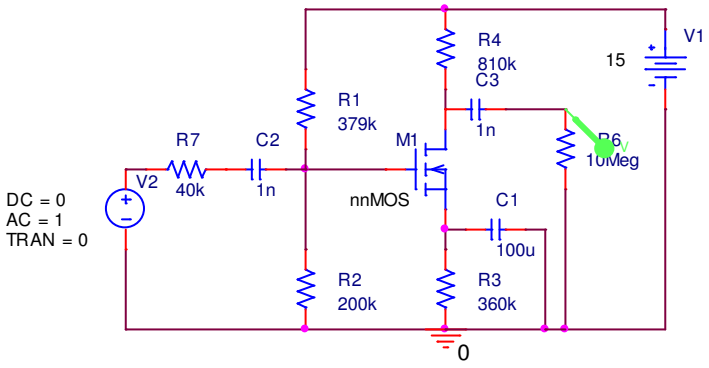
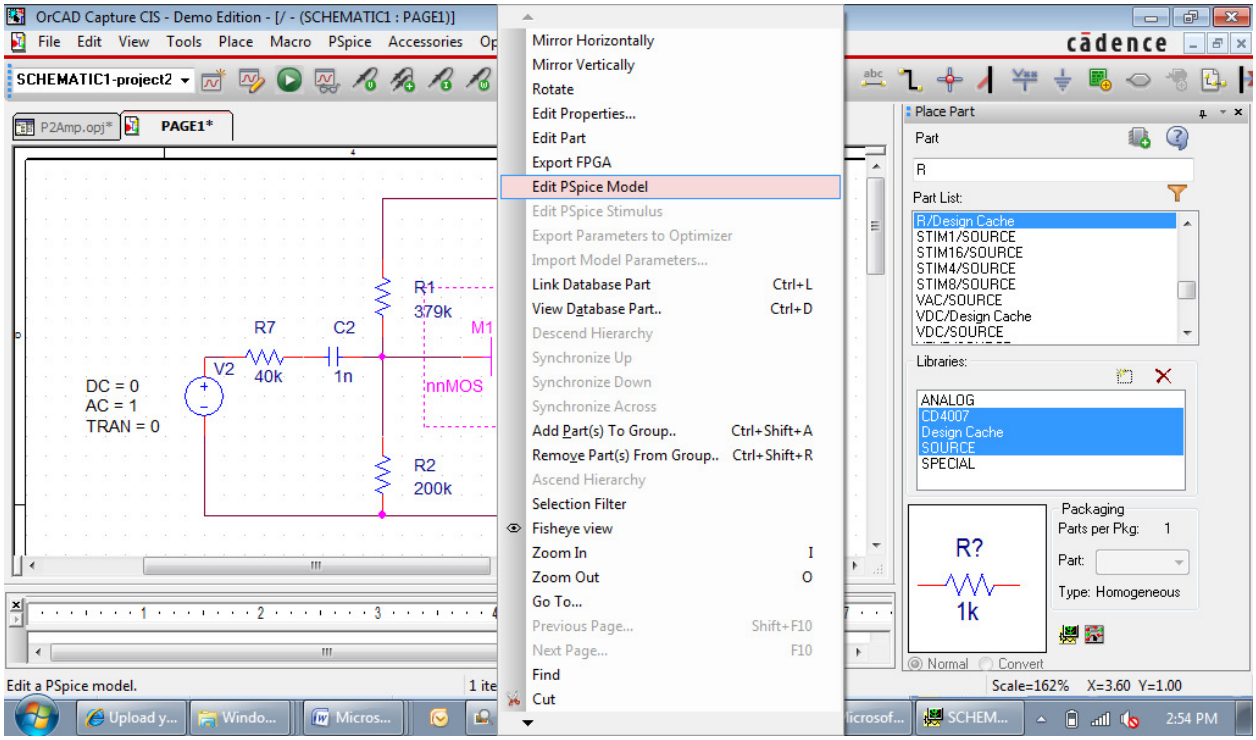
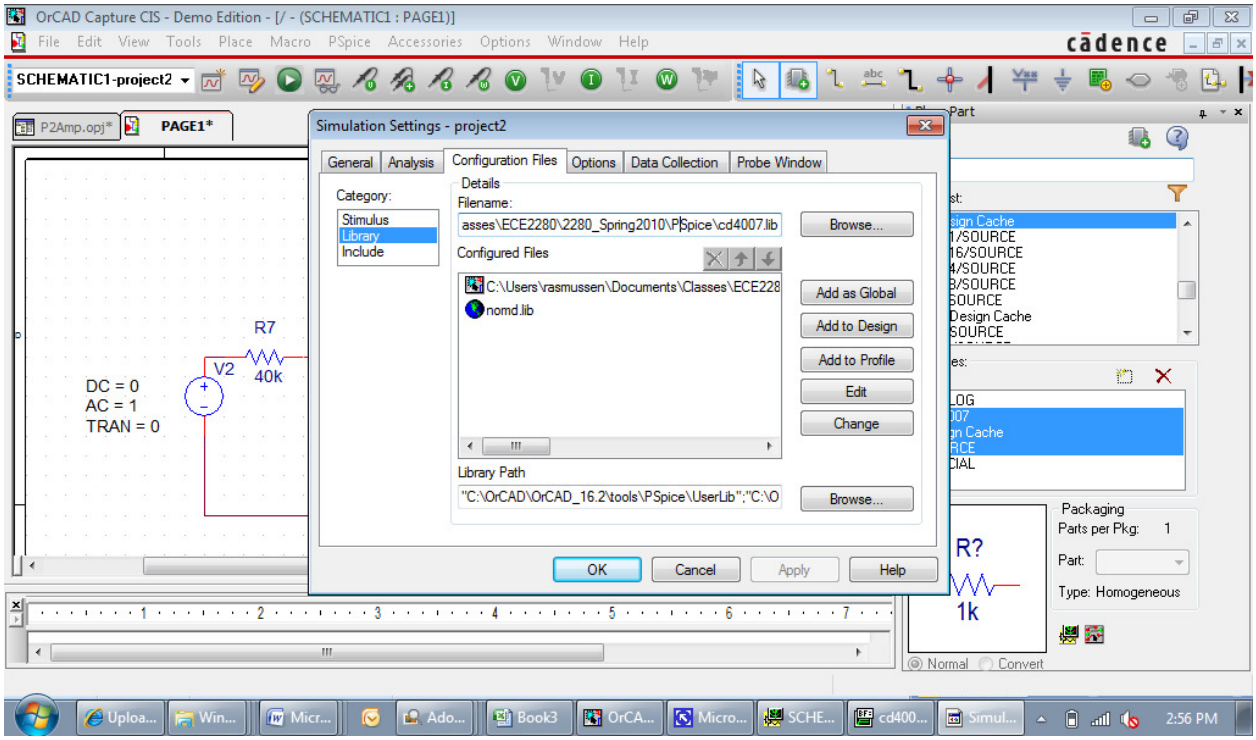


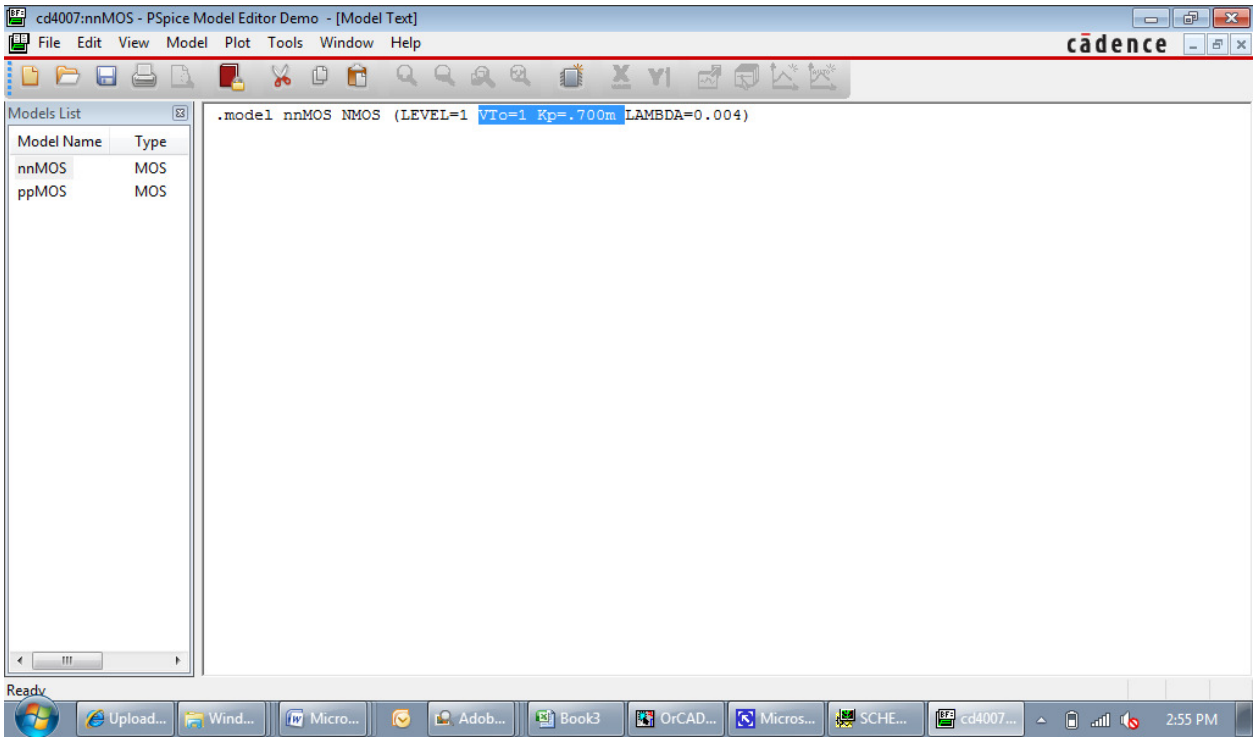
Fig. 1. Schematic of Single Amplifier

To change the values for V_t and $k_n'\left(\frac{W}{L}\right)$, right click on the transistor and select edit PSpice Model:

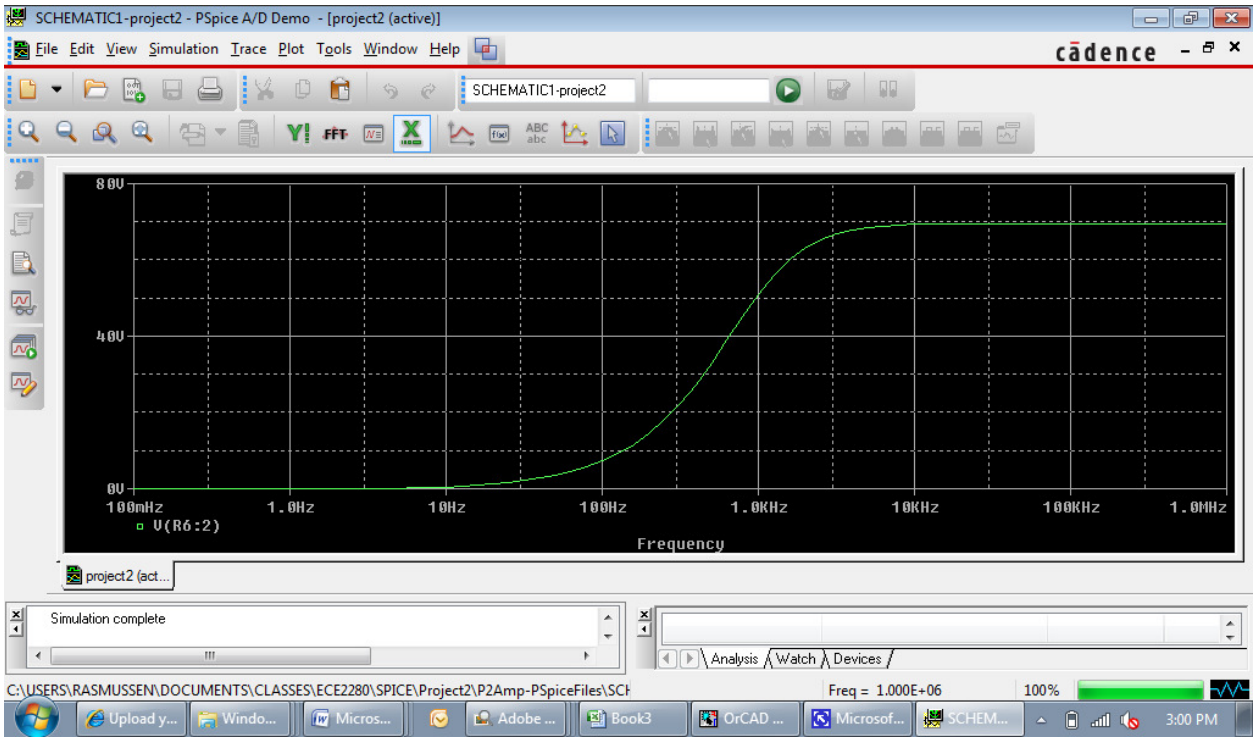


The following window pops up: *(If it does not, go to Edit Simulation File and then the configuration files tab. Go to Library and browse to where you saved the cd4007.lib file from the class website). Make sure to hit "Add to Design". Then Apply.*

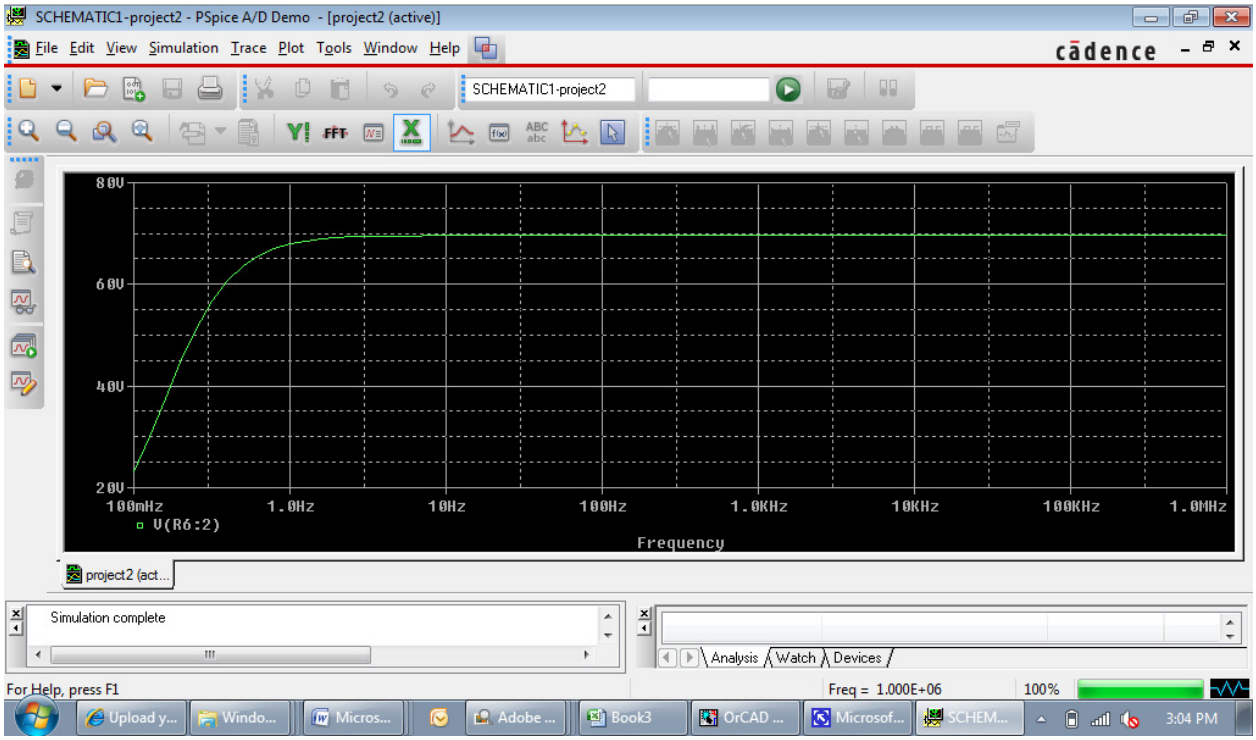




The VTo value is the value you measured in the lab experiment and the Kp is $k_n'\left(\frac{W}{L}\right)$ that you measured. Change these values to what you measured to get more accurate results. Next, I ran an AC sweep. I got the following results:



This shows that the frequency is not correct and the gain is not as high as I had designed. Therefore, I need to change the capacitors so that it will give me a lower starting frequency. Each capacitor contributes a pole value for the amplifier. You can do a trial and error analysis to see which capacitors effect the range along with changing them larger and smaller and seeing what effect they have. Note that the pole location is usually approximately 1/Req*C. Doing this resulted in:



The gain is still smaller than I want and so I know that I need at least 2 stages. I can use the same configuration twice and a “buffer” or source follower (gain of 1 with low output R) as the last stage.