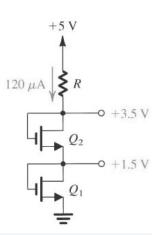
Problem Session 4

Problem 1:

The NMOS transistors in the circuit at right have $V_t=1V$, $\mu_n C_{ox}=120~\mu\text{A/V}^2$, $\lambda=0$, and $L_1=L_2=1\mu\text{m}$. Find the required values of gate width for each Q_1 and Q_2 , and the value of R, to obtain the voltage and current values indicated.



Solution:

$$V_{D2} = 3.5 \text{ V}$$
 $R = \frac{V_{DD} - V_{D2}}{I_D}$
 $R = \frac{5 - 3.5}{120 \mu \text{A}}$
 $R = 12.5 \text{ K}\Omega$

Gate and drain Q_2 at same potential, hence Q_2 in saturation region

$$V_{02} = V_{D2} = 3.5 \text{ V}$$

$$V_{02} = V_{02} - V_{22} = 3.5 - 1.5 \text{ V}$$

$$V_{02} = 2 \text{ V}$$

$$I_n = \frac{1}{2} \times \mu_n C_{0x} \frac{W_2}{L_2} (V_{02} - V_t)^2$$

$$120 = \frac{1}{2} \times 120 \times \frac{W_2}{1 \text{ µm}} (2 - 1)^2$$

$$W_2 = 2 \mu m$$

Gate and drain of Q1 01 same potential, henace Q2 in saturation regilon

$$V_{\text{CS}1} = 1.5 \text{ V}$$

$$I_{\text{D}} = \frac{1}{2} \mu_{\text{n}} C_{\text{ox}} \frac{W_{1}}{L_{\text{c}}} (V_{\text{CS}1} - V_{\text{t}})^{2}$$

$$120 = \frac{1}{2} \times 120 \times \frac{W_1}{1 \text{ um}} (1.5 - 1)^2$$

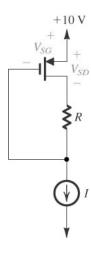
$$W_1 = 8 \mu m$$

Problem 2:

The PMOS transistor in the circuit shown at right have $k_p = 8\mu A/V^2$, W/L = 25, and $|V_{tp}| = 1V$. For I=100mA, find the voltages V_{SD} and V_{SG} for R=0, $10k\Omega$, $30k\Omega$, and $100k\Omega$. What value of R is $V_{SD}=V_{SG}$?

Also,
$$V_{SD} + IR = V_{SG}$$

 $\Rightarrow V_{SD} = V_{SG} \cdot I_R$
 $\Rightarrow IR \le |V_t|$ For PMOS to be in saturation



(A) R=0
IR = 0 <
$$|V_t|$$

Saturation:
I = 100 = $\frac{1}{2}$ ×8×25× $(V_{sg} - |V_t|)^2$
 $V_{sg} - 1 = \pm 1$
 $V_{sg} = 2 V = V_{sD}$

(B)
$$R=10 \text{ K}\Omega$$

 $IR=10\times0.1=1 \text{ V}$
 $\Rightarrow \text{Saturation}$
 $V_{\text{SG}}=2 \text{ V}$
 $V_{\text{CD}}=2-1=1 \text{ V}$

(C)
$$R = 30 \text{ K}\Omega$$

 $IR = 30 \times 0.1$
 $= 3 \text{ V}$
 $\Rightarrow \text{Triode region}$
 $100 = 8 \times 25 \left[\left(V_{\text{se}} - |V_{\text{t}}| \right) V_{\text{sD}} - \frac{1}{2} V_{\text{sD}}^2 \right]$
 $0.5 = \left[\left(V_{\text{se}} - 1 \right) \left(V_{\text{se}} - 3 \right) - \frac{1}{2} \left(V_{\text{se}} - 3 \right)^2 \right]$
 $0.5 = 0.5 V_{\text{se}}^2 - V_{\text{se}} - 1.5$
 $V_{\text{se}}^2 - 2 V_{\text{se}} - 4 = 0$
 $V_{\text{se}} = 3.24 \text{ V}, -1.2 \text{ V}$
 $V_{\text{sD}} = 3.24 - 3 = 0.24 \text{ V}$

(D) R= 100 K
$$\Omega$$

IR= 100×0.1
= 10 V
 \Rightarrow Triode region

$$100 = 8 \times 25 \left[(V_{se}-1)(V_{se}-10) - \frac{1}{2}(V_{se}-10)^2 \right]$$

$$0.5 = 0.5 \ V_{se}^2 - V_{se} - 40$$

$$V_{se}^2 - 2V_{se} - 81 = 0$$

$$V_{se} = 10.1 \ V$$

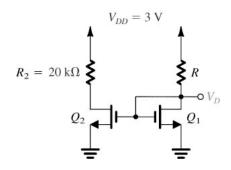
$$V_{sp} = 0.1 \ V$$

 $V_{SD} = V_{SG}$ when R = 0

Problem 3:

Let Q1 and Q2 have V_t =0.6V, $\mu_n C_{ox}$ =200 μ A/V², λ =0, L_1 = L_2 =0.8 μ m, and W_1 =8 μ m.

- (a) Establish a current 0.2mA in Q₁. Find R.
- (b) Find W_2 and a new value for R_2 so that Q_2 operates in the saturation region with a current of 0.5mA and drain voltage of 1V.



(a)
$$i_{B} = \frac{1}{2} \mu_{B} C_{ox} \frac{W}{L} (V_{GS} - V_{f})^{2}$$
We know that $i_{DI} = 0.2 \text{mA}$

$$0.2 \times 10^{-3} = \frac{1}{2} \times 200 \times 10^{-6} \times \frac{8}{0.8} (V_{GSI} - 0.6)^{3}$$

$$V_{GSI} - 0.6 = \sqrt{0.2}$$

$$V_{GSI} = 1.047V$$

$$V_{GSI} = 1.05V$$
From the circuit the value of R is
$$R = \frac{3 - 1.05}{0.2 \times 10^{-3}}$$

$$R = 9750\Omega$$

$$R = 9.75k\Omega$$

(b)
For
$$Q_2$$
 to conduct with 0.5 mA

$$R_2 = \frac{3-1}{0.5 \times 10^{-3}}$$

$$R_2 = 4000\Omega$$

$$R_2 = 4 k\Omega$$

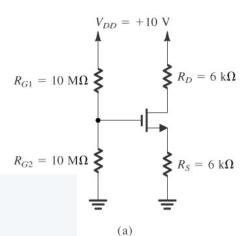
Since the gates are connected together, both transistors have the same V_{GS} and hence same i_D . In order to conduct $0.5\,\mathrm{mA}$ or multiply i_D by 2.5.

$$\begin{aligned} &\frac{W_2}{W_1} = 2.5 \\ &W_2 = 2.5 \times 8 \times 10^{-6} \\ &W_2 = 20 \, \mu \text{m} \end{aligned}$$

Problem 4:

Let $V_t=2V$, $\mu_n C_{ox}(W/L)=2mA/V^2$, and $\lambda=0$

- (a) Find I_D and V_D.
- (b) Compare these answers to the solution (Example 4.5) was found when $V_t=1V$, $\mu_n C_{ox}(W/L)=2mA/V^2$, and $\lambda=0$ that $I_D=0.5mA$ and $V_D=7V$. Comment on how tolerant (or intolerant) the circuit is to changes in device parameters.



Since the gate current is zero, the voltage at the gate is

$$V_{G} = V_{DD} \frac{R_{G2}}{R_{G1} + R_{G2}}$$

$$V_{g} = 10 \times \frac{10}{10 + 10}$$

$$V_{G} = +5 \text{ V}$$

$$V_s = 6I_D V$$

$$V_{os} = V_{os} - V_{s} = (5 - 6I_{D}) V$$

Thus ID, when transistor rreplace with another transistor

having
$$V_t = 2 \text{ Vand } K_n \frac{W}{L} = 2 \text{ mA/V}^2$$
. Then I_D

$$I_{D} = \frac{1}{2} K_{\mathbf{n}}^{'} \frac{W}{L} (V_{\mathbf{\infty}} - V_{\mathbf{t}})^{2}$$

$$I_{D} = \frac{1}{2} \times 2 \times (5 - 6I_{D} - 2)^{2}$$

$$36I_{D}^{2} - 37I_{D} + 9 = 0$$

 I_D have two values $I_D = 0.632$ not possible

Then

$$I_D = 0.4 \text{ mA}$$

$$V_D = V_{DD} - 6I_D$$

$$V_{\rm p} = 10 - 6 \times 0.4$$

$$V_D = 7.6 \text{ V}$$