Class Load

Syllabus & tentative schedule outline the workload for this semester. This is a very busy class. Every week will require **AT LEAST 10 HOURS** of outside studying to pass class.

ECE3700 + ECE2280 = Very busy semester – **Organize your time!**

How can you survive??

1. Easiest way to get through school is to actually learn and try to retain what you are asked to learn.
   - Even if you're too busy, don't lose your good study practices. What you "just get by" on today will cost you later.
   - Don't fall for the "I'll never need to know this" trap. Sure, much of what you learn you may not use, but some you will need, either in the current class, or future classes, or maybe sometime in your career. Don't waste time second-guessing the curriculum, It'll still be easier to just do your best to learn and retain.

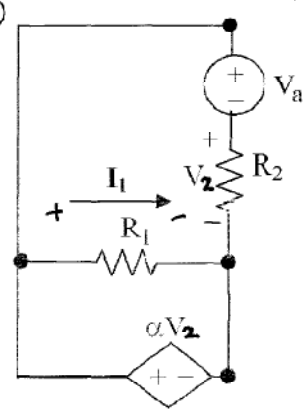
2. Don't fall for the "traps".
   - Homework answers, Extra problem solutions, Posted solutions, Lecture notes.

3. KEEP UP! Use calendar.

4. Make **"PERMANENT NOTES"** after you've finished a subject and feel that you know it.

REVIEW:

- KVL, KCL, OHM'S LAW, THEVENIN EQUIVALENCE, OPAMPS
  a. Derive an expression for I_1. The expression must not contain more than the circuit parameters α, V_a, R_1, and R_2. **(Make sure to eliminate V_2 from the answer) ($\alpha \neq 1$)**



voltage loop: $+\alpha V_2 - V_a - V_2 = 0$

$V_2(\alpha - 1) = V_a$

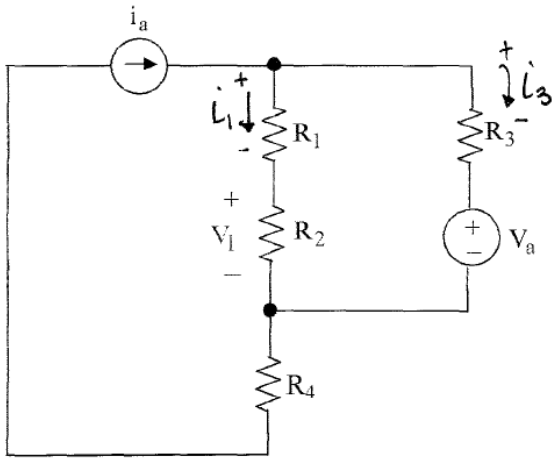
$V_2 = \frac{V_a}{(\alpha-1)}$

voltage loop: $-I_1 R_1 + V_2 + V_a = 0$

$I_1 = \frac{V_2 + V_a}{R_1} = \frac{V_a}{(\alpha-1)R_1} + \frac{V_a(\alpha-1)}{R_1(\alpha-1)}$

$I_1 = \frac{V_a + V_a\alpha - V_a}{(\alpha-1)R_1} = \boxed{\frac{V_a\alpha}{(\alpha-1)R_1}}$

Derive an expression for v_1. The expression must not contain more than the circuit parameters V_a, i_a, R_1, R_2, R_3, and R_4. *(Hint: It is not just a simple voltage divider)*



Ohm's Law: V=I*R

$$V_1 = i_1 R_1$$

KCL: Summation of currents: $i_a - i_1 - i_3 = 0$ ①

KVL: voltage loop: $+i_1(R_2) + i_1(R_1) - i_3(R_3) - V_a = 0$ ②

From ① $\Rightarrow$ $i_3 = i_a - i_1$ (plugging this into ②)

$$i_1(R_1+R_2) - (i_a - i_1)(R_3) - V_a = 0$$

$$i_1(R_1+R_2+R_3) = i_a R_3 + V_a$$

$$\therefore\ i_1 = \frac{i_a R_3 + V_a}{R_1+R_2+R_3}$$

$$V_1 = i_1 R_1 = \boxed{\frac{i_a R_3 R_1 + V_a R_1}{R_1+R_2+R_3}}$$

Thevinen Equivalence:

CASE 1: Thevenin Equivalent (circuit with only independent sources)

Step 1. Turn off all independent sources. (This means V=0 (short) and I=0 (open))

Step 2. Rth=equivalent R seen between the two desired nodes a-b.

Step 3. Vth= open circuit voltage between a-b.

CASE 2: Thevenin Equivalent (circuit with dependent sources)
Step 1. Calculate the open circuit voltage, Vth.
Step 2. Calculate Rth. Use only one of the methods below:

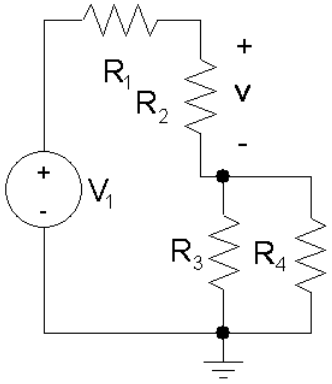
Method 1: TEST SOURCE
(a) Remove all independent sources.
(b) Apply a voltage source *Vtest* between *a-b* and determine the resulting current *Itest*. {OR apply a current source *Itest* between *a-b* and determine the resulting voltage *Vtest*. Using 1V or 1A as the value of the applied test sources allow easy multiplication or division)
(c) Rth=Vtest/Itest

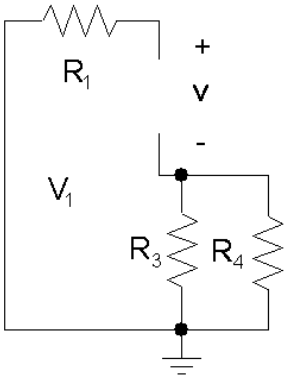
Method 2: SHORT CIRCUIT
(a) Short circuit between a-b and find Isc, short circuit current.
(b) R_{Th} = Vth/*Isc*

Example, Case 1: (independent sources) Find Thevenin across R2(Removing R2 from the circuit).

< http://en.wikibooks.org/wiki/Electronics/Thevenin/Norton_Equivalents>

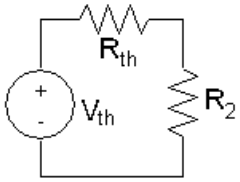
independent sources.
hort) and I=0 (open))
R.



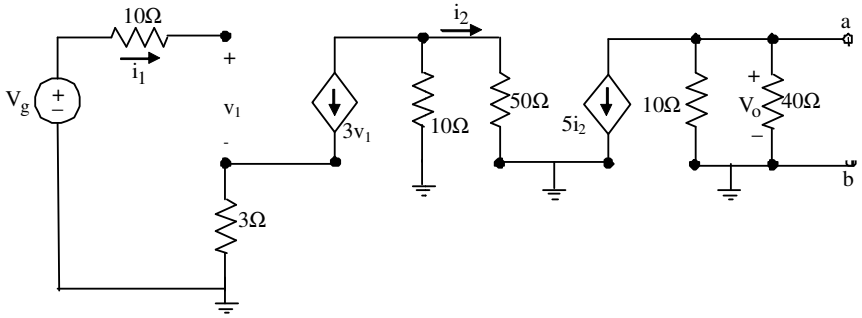


Step 2 and Step 3:

$$R_{th} = R_1 + R_3||R_4$$
$$V_{th} = V_1$$



Example Case 2:
Find Thevenin between a-b.



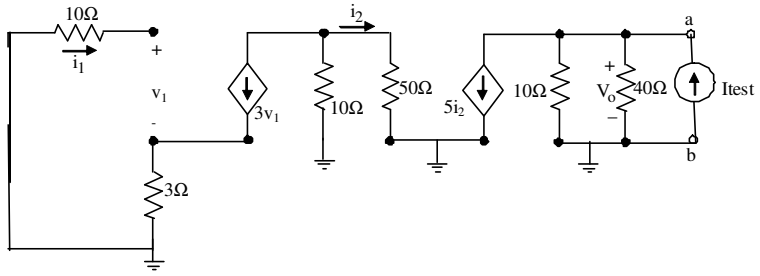
Step 1: (Find Vo(open circuit voltage))

) = -40i2

· 10v1=Vg

ʳth

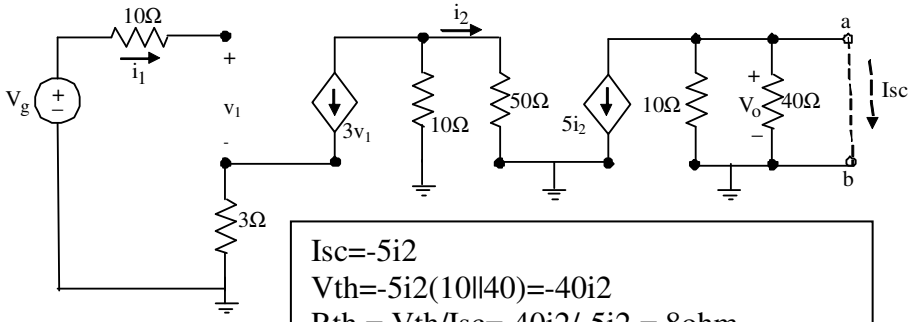
(a) Remove all independent sources.
(b) Apply a test source (Itest in this case). Analyze circuit for Vtest=Vo in this case.

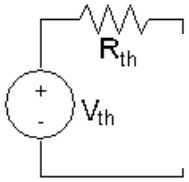


Vo=Vtest = (10||40)*(Itest-5i2)

i1=0
v1=-3v1(3) => v1+9v1=0=> v1(10)=0 => v1=0
i2=0
Vtest = 8Itest
Rth = 8Itest/Itest = 8ohm

Step 2:
Method 2: SHORT CIRCUIT





Isc=-5i2
Vth=-5i2(10||40)=-40i2
Rth = Vth/Isc=-40i2/-5i2 = 8ohm

SAME

Note: Use of the Isc is sometimes easier than the test source. Suggest trying that method first. Both method's can be used to "check" the other one.

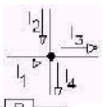
DC Review Notes

ECE 2100 A.Stolp 2/27/00

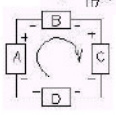
Basic electrical quantities

		Unit
Charge, actually moves	Q	Coulomb (C)
Current, like fluid flow	$I = \frac{Q}{s}$	Amp (A, mA, μA,...)
Voltage, like pressure	V	volt (V, mV, kV,...)
Resistance	$R = \frac{V}{I}$	Ohm (Ω, kΩ, MΩ,...;
Power energy/time	P = V·I	Watt (W, mW, kW, MW,...)

KCL, Kirchoff's current law
$I_{in} = I_{out}$ of any point, part, or section

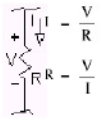


KVL, Kirchoff's voltage law
$V_{gains} = V_{drops}$ around any loop

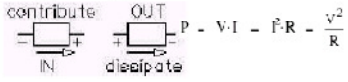


Node = all points connected by wire, all at same voltage (potential)

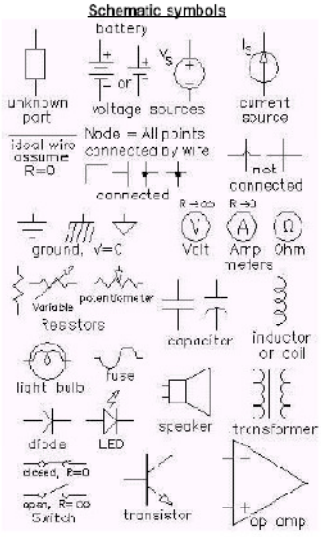
Ohm's law(resistors)
$V = I \cdot R$



Power $P_{IN} = P_{OUT}$ for resistor circuits



Schematic symbols

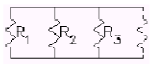


Maximum power transfer: $R_L = |Z_{Th}|$
Load = Thevenin's

Resistors and impedances

series: $R_{eq} = R_1 + R_2 + R_3 + \ldots$ Exactly the same **current** through each resistor

parallel: $R_{eq} = \frac{1}{\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3} + \ldots}$ Exactly the same **voltage** across each resistor



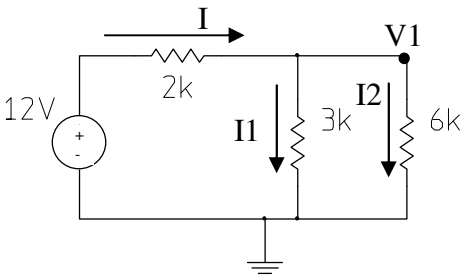
Voltage divider: $V_{Rn} = V_{total} \frac{R_n}{R_1 + R_2 + R_3 + \ldots}$

current divider: $I_{Rn} = I_{total} \frac{\frac{1}{R_n}}{\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3} + \ldots}$

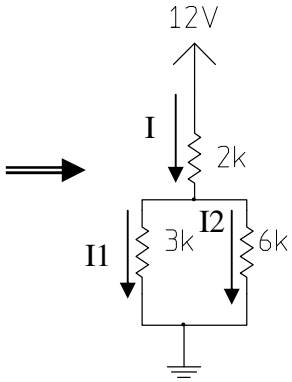
Multiple unknowns:
1. Combine resistors into equivalents where possible.
2. Use superposition if there are multiple sources and you know all the resistors.
3. Use KCL, KVL, & Ohm's laws to write multiple equations and solve.

Non-linear elements:
Assume a linear region and try to solve.

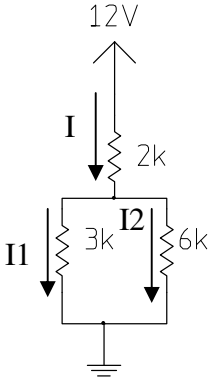
Example #3



Same as



Solve for I, I1, I2, and V1: $I = \frac{12V}{2k + 3k \| 6k} = \frac{12}{2k + \left(\frac{3k(6k)}{3k+6k}\right)} = \frac{12}{2k + 2k} = 3mA$



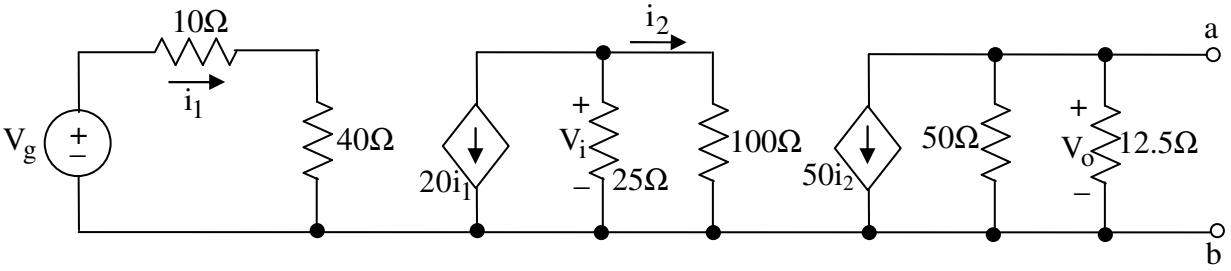
$I1 = \frac{V1}{3k}; I2 = \frac{V1}{6k}$

$I = I1 + I2 = V1\left(\frac{1}{3k} + \frac{1}{6k}\right) = V1\left(\frac{3k}{6k}\right) = V1\left(\frac{1}{2k}\right) \Rightarrow V1 = I \cdot 2k = 3m(2k) = 6V$

$I1 = \frac{6}{3k} = 2mA; I2 = \frac{6}{6k} = 1mA$

Example #4

Given V_g=6.25mV, find V_o. Find the Thevenin equivalent between terminals a-b.



$V_{th} = V_o$ → Therefore find V_o:

$V_o = (50\Omega \| 12.5\Omega) \cdot (-50 i_2) = -500\, i_2$ — unknown — find eq. for i_2

$\frac{50 \cdot 12.5}{12.5 + 50} = 10\Omega$

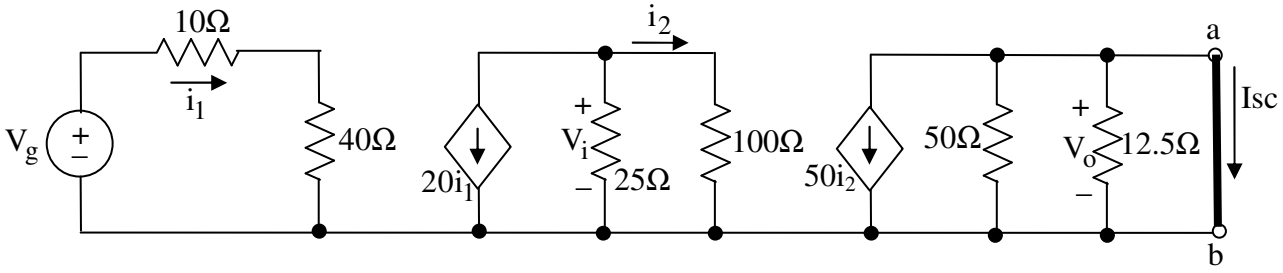
$\Rightarrow i_2 = \frac{V_i}{100} = \frac{-20i_1 \cdot (25 \| 100)}{100} = \frac{-20i_1}{100} \cdot \frac{25 \cdot 100}{100 + 25} = -4i_1$ — unknown find new eq

$\Rightarrow i_1 = V_g/(10+40) = \frac{6.25m}{50} = .125m$ — No unknowns plug into previous equations

$i_2 = -4i_1 = -4(.125m) = -.5m$

$V_{th} = V_o = -500 i_2 = +500(+.5) = .250V$

$R_{th} = \frac{V_{th}}{i_{sc}}$ where i_{sc} is the short circuited current =>



From the analysis for Vth (above). Vth=-500i2
Isc=-50i2 so

Rth=-500i2/-50i2=10ohm
(note that for this circuit configuration, it appears that the output R (Rth) that the "top" of the dependent current source looks like an "open" so that the equivalent R is 50||12.5=10ohm).

Signals

A ***DC*** (direct current) signal refers to a fixed voltage whose polarity never reverses. {Ex. 5V,-15V}

An ***AC*** (alternating current) occurs when charge carriers periodically reverse their direction of movement. {Ex. Sinusoid => 5sin(10t), Square Waves, Sawtooth-shaped}

- The voltage of an AC power source changes from instant to instant in time.
- Wall plug is AC with a frequency of 60 hertz and 120V
  - 120*(1.414) peak value
- RMS value = peak value/$\sqrt{2}$

Real signals such as your voice, environmental sensors, etc. are time-varying voltages or currents that carry information.

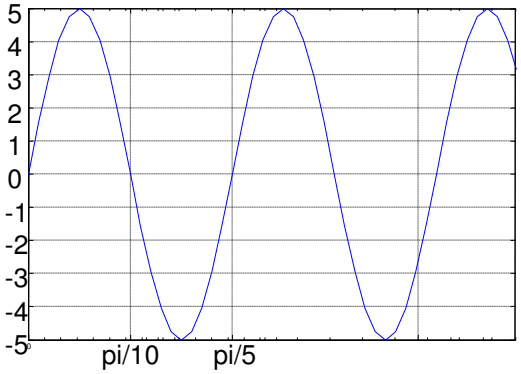
- Transducers transform one form of energy into another:
  - Ex: Microphone, Camera, Thermistor or other thermal sensor, Potentiometer, Light sensor, Computer, etc.
- **Sine waves are "pretend" signals**
  - Although sine waves are not *real* signals, we use them to simulate signals all the time, both in calculations and in the lab. This makes sense because all signals can be thought of as being made up of a spectrum of sine waves.

These types of signals can be hard to characterize mathematically. If a signal is periodic but arbitrary in amplitude, recall that it can be expressed by the Fourier series(a series of sinewaves of different frequencies and amplitudes).

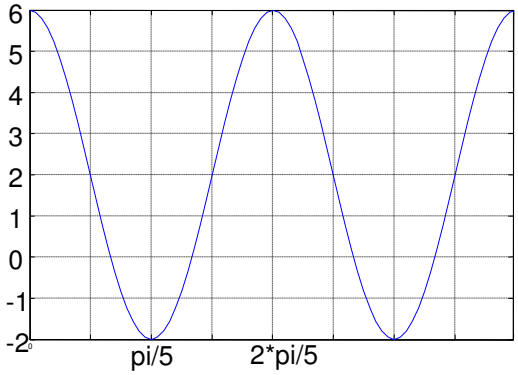
Example #5

Sketch the following waveforms. Identify the dc component of the waveform and the ac component of the waveform.

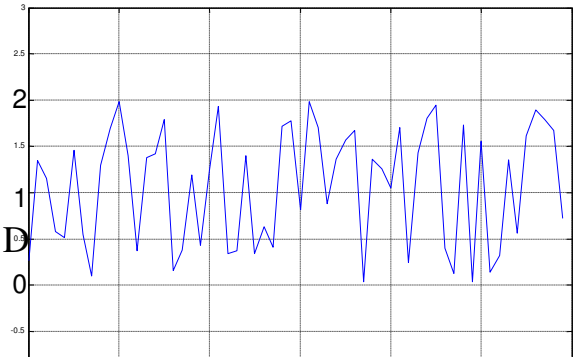
a. Vs=5sin(10t) V



b. Vs=2V +4sin(5t+90^o) V

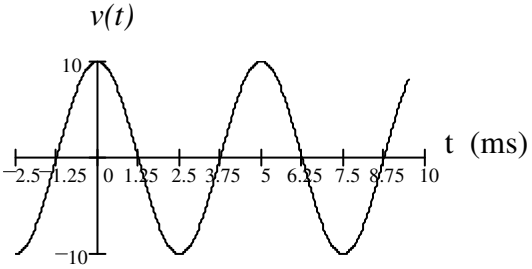


c. Vs= 1V ± 1V

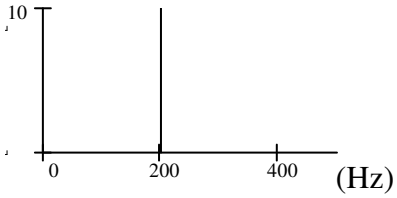


Sine wave:

Time domain:



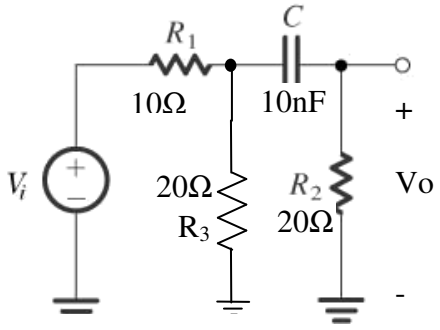
Frequency domain:

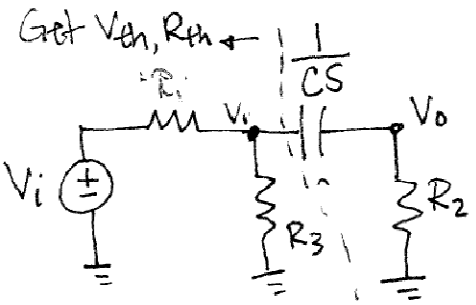


amplitude := 10·V $V_{RMS} := \frac{10 \cdot V}{\sqrt{2}}$ f = 200·Hz T := 5·ms $f := \frac{1}{T}$ ω := 2·π·f

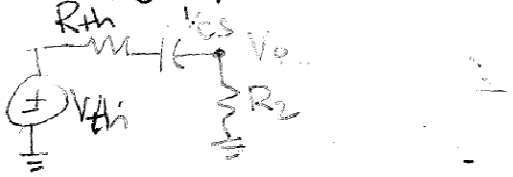
Example #6

When analyzing a time dependent element(capacitors), translate into frequency domain => $C = \frac{1}{jwC} = \frac{1}{sC}$ and then analyze the circuit using normal circuit analysis techniques. Analyze the circuit to the right to find the transfer function $\frac{Vo}{Vi}$. Solve the circuit symbolically first (with R_1, R_2, R_3, C) and then plug in their values.





$V_{th} = \frac{R_3 \cdot V_i}{R_3 + R_1}$, $R_{th} = R_1 \| R_3$



$$\frac{V_o}{V_i} = \frac{R_2 C \cdot S \cdot R_3 \cdot V_i}{(R_1 + R_3)([R_2 + R_1 \| R_3]CS + 1)} = \frac{20(10n)\,S(20)}{(10+20)(266.7 \cdot 10n \cdot S + 1)}$$

$$\frac{V_o}{V_i} = \frac{4\times10^{-6} \cdot S}{30(266.7n\,S + 1)} = \frac{(133n) \cdot S}{(266.7n \cdot S + 1)}$$

What does this equation mean? By substituting s=jω in the above equation. The magnitude of the equation is:

$$\left|\frac{133n(\omega)j}{(266.7n(\omega)j + 1)}\right| = \frac{|133n(\omega)j|}{|(266.7n(\omega)j + 1)|} = \frac{133n(\omega)}{\sqrt{(266.7n(\omega))^2 + 1^2}}$$

This magnitude can now be graphed with the x-axis as ω and the y axis as the calculated value. This is one of the graphs used for the Bode plots. To plot this, an understanding of dB is needed.

Decibels

Your ears respond to sound logarithmically, both in frequency and in intensity.
Musical octaves are in ratios of two. "A" in the middle octave is 220 Hz, in the next, 440 Hz, then 880 Hz, etc...
It takes about ten times as much power for you to sense one sound as twice as loud as another.

10x power ~ 2x loudness

A bel is such a 10x ratio of power. Power ratio expressed in bels = $\log\left(\frac{P_2}{P_1}\right)$ bels — The bel is named for Alexander Graham Bell.

It is a logarithmic expression of a unitless ratio (like gain).

The bel unit is never actually used, instead we use the decibel (dB, 1/10th of a bel).

Power ratio expressed in dB = $10\cdot\log\left(\frac{P_2}{P_1}\right)$ dB

dB are also used to express voltage and current ratios, which related to power when squared. $P = \frac{V^2}{R} = I^2\cdot R$

Voltage ratio expressed in dB = $10\cdot\log\left(\frac{V_2^2}{V_1^2}\right)$ dB = $20\cdot\log\left(\frac{V_2}{V_1}\right)$ dB

Current ratio expressed in dB = $20\cdot\log\left(\frac{I_2}{I_1}\right)$ dB

These are the most common formulas used for dB

Some common ratios expressed as dB

$20\cdot\log\left(\frac{1}{\sqrt{2}}\right) = -3.01\cdot dB$	$10^{-\frac{3}{20}} = 0.708$	$20\cdot\log\left(\sqrt{2}\right) = 3.01\cdot dB$	$10^{\frac{3\cdot dB}{20}} = 1.413$
$20\cdot\log\left(\frac{1}{2}\right) = -6.021\cdot dB$	$10^{-\frac{6}{20}} = 0.501$	$20\cdot\log(2) = 6.021\cdot dB$	$10^{\frac{6\cdot dB}{20}} = 1.995$
$20\cdot\log\left(\frac{1}{10}\right) = -20\cdot dB$	$10^{-\frac{20}{20}} = 0.1$	$20\cdot\log(10) = 20\cdot dB$	$10^{\frac{20\ dB}{20}} = 10$
$20\cdot\log\left(\frac{1}{100}\right) = -40\cdot dB$	$10^{-\frac{40}{20}} = 0.01$	$20\cdot\log(100) = 40\cdot dB$	$10^{\frac{40\ dB}{20}} = 100$

We will use dB fairly commonly in this class, especially when talking about frequency response curves.

Example #7

The frequency domain expression for the output over the input of a circuit is solved to be $\frac{\text{output}}{\text{input}} = \frac{10^5(s+5)}{(s+1)(s+5000)}$ Substitute s=jω into the above equation and calculate the magnitude(dB) and phase (degrees). Plug in values for ω equal to 10^{-1}, 0.8, 0.9, 10^{-0}, 2, 3, 4, 5, 6, 7, 10^1, 10^2, 10^3, 3000, 4000, 5000, 6000, 7000, 10^4, 10^5 rad/sec and plot these values on a semilog graph for both magnitude and phase. Recall that magnitude, |a+bj| = $\sqrt{a^2+b^2}$ and the phase, $\angle(a+bj) = \tan^{-1}(b/a)$

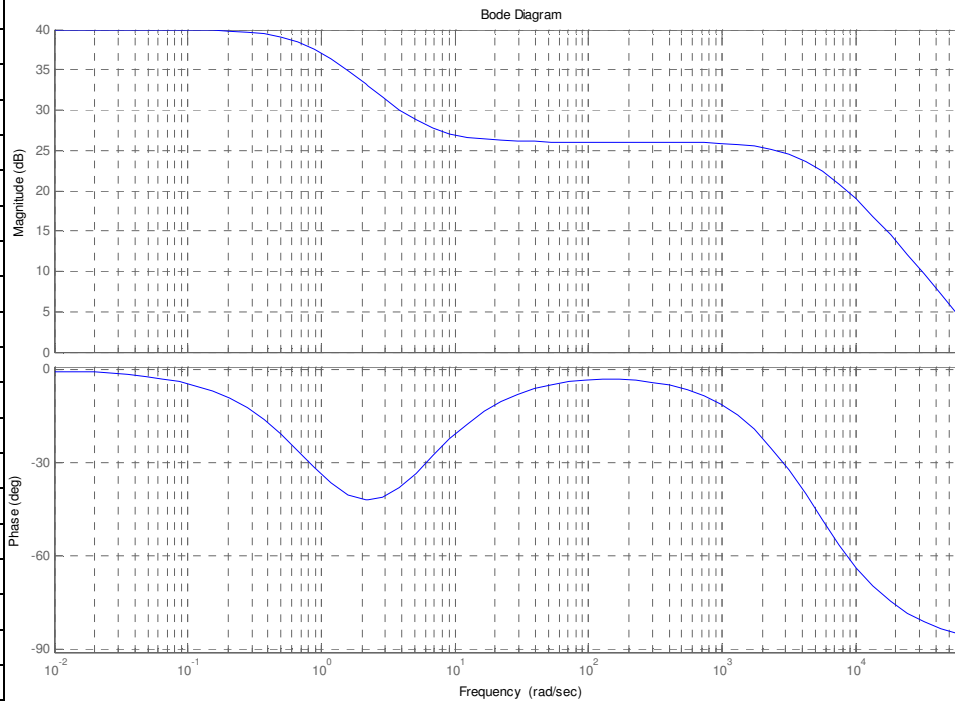
Magnitude: $\left|\frac{\text{output}}{\text{input}}\right| = \left|\frac{10^5(j\omega+5)}{(j\omega+1)(j\omega+5000)}\right| = \frac{\left|10^5\right|\left|(j\omega+5)\right|}{\left|(j\omega+1)\right|\left|(j\omega+5000)\right|} = \frac{\sqrt{(10^5)^2+0^2}\sqrt{5^2+\omega^2}}{\left(\sqrt{1^2+\omega^2}\right)*\left(\sqrt{5000^2+\omega^2}\right)}$

Phase: $\angle\left(\frac{\text{output}}{\text{input}}\right) = \angle\left(\frac{10^5(j\omega+5)}{(j\omega+1)(j\omega+5000)}\right) = \frac{\angle 10^5 * \angle(j\omega+5)}{\angle(j\omega+1)*\angle(j\omega+5000)} =$

$=0+\tan^{-1}(\omega/5)-\tan^{-1}(\omega/1)-\tan^{-1}(\omega/5000)$ {@ω=0.1rad/sec =>

magnitude=99.5V/V=20*log(99.5V/V)=39.96dB; phase=0+1.15-5.7-0.001=-4.6 degrees

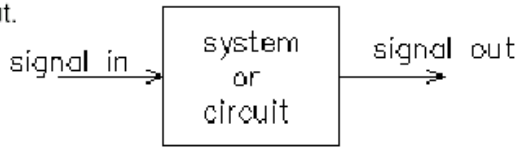
ω (rad/sec)	Mag(dB)	Phase(Degrees)
.1	39.95852	-4.56598
0.8	37.96134	-29.5787
0.9	37.56169	-31.7936
1	37.16003	-33.7015
2	33.65488	-41.6565
3	31.33539	-40.6357
4	29.84395	-37.3498
5	28.86056	-33.7474
6	28.19187	-30.412
7	27.72321	-27.4878
10	26.94647	-20.969
100	26.02927	-3.43523
1000	25.85037	-11.5391
3000	24.68522	-31.0402
4000	23.87217	-38.7171
5000	23.0103	-45.0458
6000	22.1467	-50.2326
7000	21.30768	-54.4951
10000	19.0309	-63.4579
100000	-0.01084	-87.1399
1000000	-20.0001	-89.7138



Frequency response

The "response" of a system or circuit is the output for a given input.

A "transfer function" is a mathmatical description of how the output is related to the input.



"Block diagram"

output = Transfer function x input

or... Transfer function = $\frac{\text{output}}{\text{input}}$

No real system or circuit treats all frequencies the same, so all real transfer functions are functions of frequency.

Transfer function = H(ω) or H(f) or, Transfer function = H(s)

The transfer function can be used to describe the "frequency response" of a circuit. That is, how does the circuit respond to inputs of different frequencies.

Bode Plots

- 2 plots – both have logarithm of frequency on x-axis
  - y-axis magnitude of transfer function, H(s), in dB
  - y-axis phase angle, in degrees

The plot can be used to interpret how the input affects the output in both magnitude and phase over frequency. To sketch the graphs, the circuit is first analyzed to find output/input (transfer function). This equation is used as the basis for the plots. The equation is analyzed for magnitude and phase as shown in the previous example (#5)

Is there a **shortcut** to graph the Bode plots?

MAGNITUDE PLOT:

1) Determine the Transfer Function of the system:

$$H(s) = \frac{K(s+z_1)(s+z_2)\cdots}{(s+p_1)(s+p_2)\cdots}$$

2) Rewrite it by factoring both the numerator and denominator into the **standard** form

$$H(s) = \frac{Kz_1z_2\cdots(s/z_1+1)(s/z_2+1)\cdots}{p_1p_2\cdots(s/p_1+1)(s/p_2+1)\cdots}$$

where the z s are called zeros and the p s are called poles.

3) Replace s with $j\omega$. Then find the **Magnitude** of the Transfer Function.

$$H(jw) = \frac{Kz_1z_2\cdots(jw/z_1+1)(jw/z_2+1)\cdots}{p_1p_2\cdots(jw/p_1+1)(jw/p_2+1)\cdots}$$

If we take the $\log_{10}$ of this magnitude and multiply it by 20 it takes on the form of

$$20\log_{10}(H(jw)) = 20\log_{10}\left(\frac{Kz_1z_2\cdots(jw/z_1+1)(jw/z_2+1)\cdots}{p_1p_2\cdots(jw/p_1+1)(jw/p_2+1)\cdots}\right) =$$

$$20\log_{10}|K| + 20\log_{10}|z_1| + 20\log_{10}|z_2| + \cdots + 20\log_{10}\left|(jw/z_1+1)\right| + 20\log_{10}\left|(jw/z_2+1)\right| + \cdots - 20\log_{10}|p_1|$$

$$- 20\log_{10}|p_2| - \cdots - 20\log_{10}\left|(jw/z_1+1)\right| - 20\log_{10}\left|(jw/z_2+1)\right| - \cdots$$

*Recall => log(a*b) = log(a)+log(b) and log(a/b)=log(a) - log (b)*

You can see from this expression that each term contributes a number to the final value at a specific frequency. Therefore, each of these individual terms is very easy to show on a logarithmic plot. The entire Bode log magnitude plot is the result of the superposition of all the straight line terms. This means with a little practice, we can quickly sketch the effect of each term and quickly find the overall effect. To do this we have to understand the effect of the four different types of terms.

These include: 1) Constant terms K

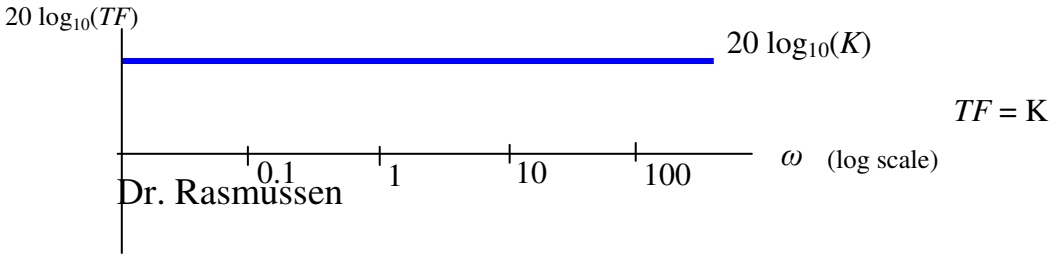
2) Poles and Zeros at the origin $|j\omega|$

3) Poles and Zeros not at the origin $\left|1 + \frac{j\omega}{p_1}\right|$ or $\left|1 + \frac{j\omega}{z_1}\right|$

4) Complex Poles and Zeros (not addressed at this time)

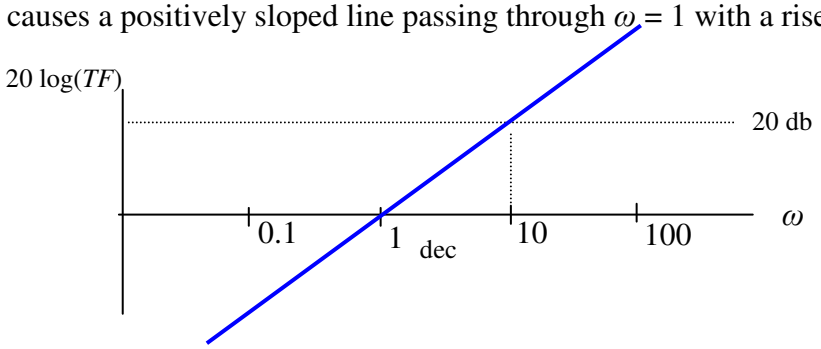
Effect of Constant Terms:

Constant terms such as K contribute a straight horizontal line of magnitude $20\log_{10}(K)$ (not dependent on frequency)



Effect of Individual Zeros and Poles at the origin:

A **zero** at the origin occurs when there is an ***s*** or ***jω*** multiplying the numerator. Each occurrence of this causes a positively sloped line passing through $\omega = 1$ with a rise of 20 db over a decade.



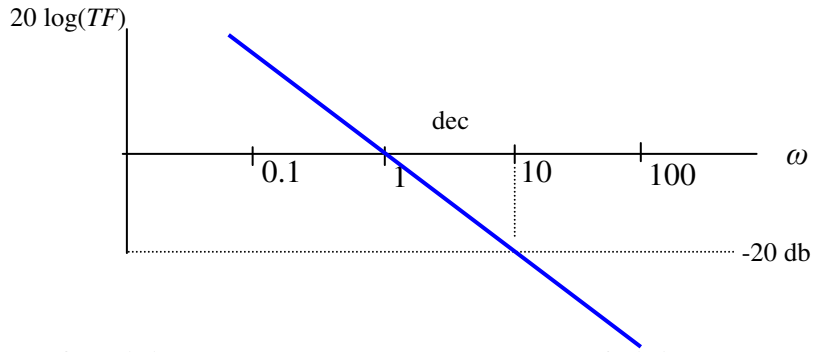
$TF = |\ j\omega\ |$

If ω=0.1 => |j0.1| = 0.1V/V=20log(0.1)=-20dB

If ω=1 => |j1| = 1V/V=20log(1)=0dB

If ω=10 => |j10| = 10V/V=20log(10)=20dB

A pole at the origin occurs when there are ***s*** or ***jω*** multiplying the denominator. Each occurrence of this causes a negatively sloped line passing through $\omega = 1$ with a drop of 20 db over a decade.



$$TF = \frac{1}{j\omega}$$

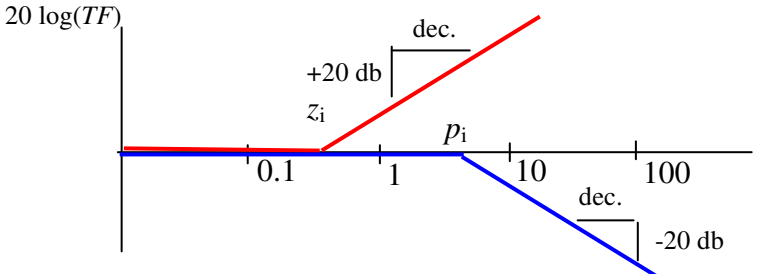
If ω=0.1 => $|\frac{1}{j0.1}|$ = 10V/V=20log(10)=20dB

If ω=1 => $|\frac{1}{j1}|$ = 1V/V=20log(1)=0dB

If ω=10 => $|\frac{1}{j10}|$ = 0.1V/V=20log(0.1)=-20dB

Effect of Individual Zeros and Poles Not at the Origin

Zeros and Poles **not at the origin** are indicated by the $(1+j\omega/z_i)$ and $(1+j\omega/p_i)$. The values z_i and p_i in each of these expression is called a **break frequency**. Below their break frequency these terms do not contribute to the log magnitude of the overall plot. Above the break frequency, they represent a ramp function of 20 db per decade. Zeros give a positive slope. Poles produce a negative slope.



$$TF = \frac{\left|1 + \frac{j\omega}{z_i}\right|}{\left|1 + \frac{j\omega}{p_i}\right|}$$

Before looking at the effect of the 2nd order terms, let's learn how to plot with the three terms already described. We will work several examples where we show how the Bode log magnitude plot is sketched. To complete the **log magnitude vs. frequency plot** of a Bode diagram, **superposition** all the lines of the different terms on the same plot.

PHASE PLOT:

For our original transfer function,

$$H(jw)=\frac{Kz_1z_2\cdots(jw/z_1+1)(jw/z_2+1)\cdots}{p_1p_2\cdots(jw/p_1+1)(jw/p_2+1)\cdots}$$

the cumulative phase angle associated with this function are given by

$$\angle H(jw)=\frac{\angle K\angle z_1\angle z_2\cdots\angle(jw/z_1+1)\angle(jw/z_2+1)\cdots}{\angle p_1\angle p_2\cdots\angle(jw/p_1+1)\angle(jw/p_2+1)\cdots}$$

Then the cumulative phase angle as a function of the input frequency may be written as

$$\angle H(jw)=\angle[K+z_1+z_2+\cdots-p_1-p_2-\cdots]+\tan^{-1}(w/z_1)+\tan^{-1}(w/z_2)+\cdots-\tan^{-1}(w/p_1)-\tan^{-1}(w/p_2)-\cdots$$

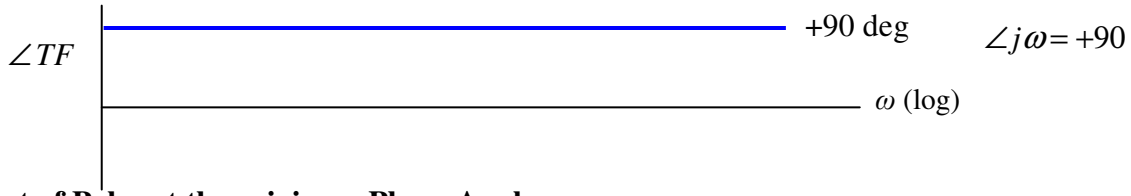
Once again, to show the phase plot of the Bode diagram, lines can be drawn for each of the different terms. Then the total effect may be found by superposition.

Effect of Constants on Phase:

A **positive** constant, ***K*>0,** has no effect on phase. A **negative** constant, ***K*<0,** will set up a phase shift of $\pm 180^o$.

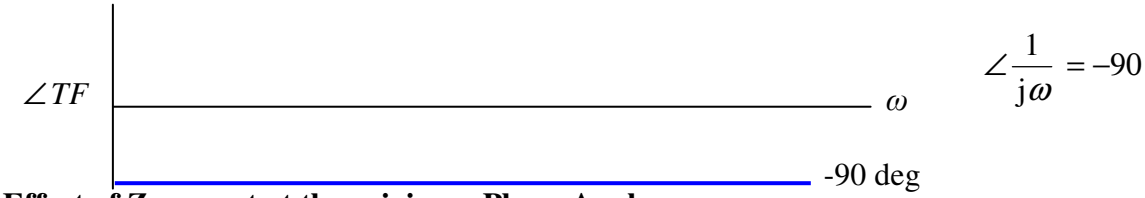
Effect of Zeros at the origin on Phase Angle:

Zeros at the origin, *s*, cause a constant **+90 degree shift** for each zero.



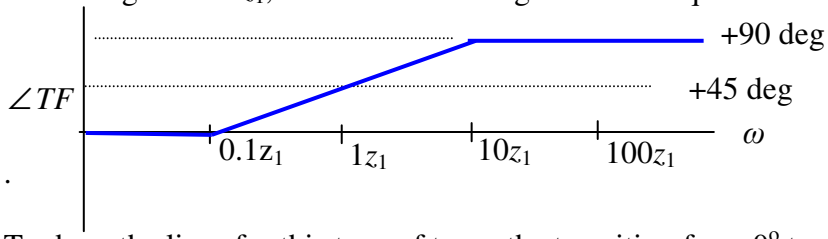
Effect of Poles at the origin on Phase Angle:

Poles at the origin, s^{-1}, cause a constant **-90 degree shift** for each pole.



Effect of Zeros not at the origin on Phase Angle:

Zeros not at the origin, like $\left|1+\frac{j\omega}{z_1}\right|$, have no phase shift for frequencies **much lower** than z_i, have a + 45 deg shift at z_1, and have a +90 deg shift for frequencies **much higher** than z_1.



If $z_1=1 \Rightarrow \angle(1+j\omega)=\tan^{-1}\left(\frac{\omega}{1}\right)$

If ω=0.1 => $\tan^{-1}(0.1)=5.7^o$

If ω=1 => $\tan^{-1}(1)=45^o$

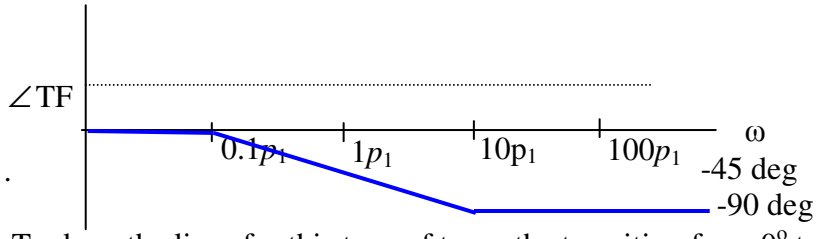
If ω=10 => $\tan^{-1}(10)=84^o$

If ω=100 => $\tan^{-1}(100)=89^o$

To draw the lines for this type of term, the transition from 0^o to $+90^o$ is drawn over 2 decades, starting at $0.1z_1$ and ending at $10z_1$.

Effect of Poles not at the origin on Phase Angle:

Poles not at the origin, like $\frac{1}{\left|1+\frac{j\omega}{p_1}\right|}$, have no phase shift for frequencies **much lower** than p_i, have a -45 deg shift at p_1, and have a -90 deg shift for frequencies **much higher** than p_1.



.

To draw the lines for this type of term, the transition from 0^o to -90^o is drawn over 2 decades, starting at $0.1p_1$ and ending at $10p_1$.

When drawing the phase angle shift for **not-at-the-origin zeros and poles**, first locate the break frequency of the zero or pole. Then start the transition 1 decade before, following a slope of $\pm 45^o$ /decade. Continue the transition until reaching the frequency one decade past the break frequency.

SUMMARY OF STRAIGHT-LINE APPROXIMATION PROCEDURE STEPS(NO COMPLEX):

(Note that a decade is a **multiple** of 10 – 1,10,100,1000,etc)

1. Rearrange the equation into standard form:

$$H(s)=\frac{Kz_1z_2\cdots(s/z_1+1)(s/z_2+1)\cdots}{p_1p_2\cdots(s/p_1+1)(s/p_2+1)\cdots}$$

where K, z_1, z_2, etc are all constant values.

2. Determine the poles and zeros.

*Note: If there are more than one poles/zeros at the same break frequency(say there are r), just multiply the slope/phase changes by r. (ex. $(1+s/10)^2$ => it is a negative zero(numerator) and so it will change the slope by 2*20dB/dec and have a 2*45^{o}slope/dec.*

3. Draw the magnitude plot:

   a. Determine starting value:

   Case 1: No pole or zero at the origin:

$$\text{starting value} = 20\log_{10}\left(\frac{Kz_1z_2\cdots}{p_1p_2\cdots}\right)$$

   Case 2: A pole or zero at the origin:

   - Pick a frequency value less than the lowest pole or zero value.

- Plug in the frequency in the standard form equation above and take the magnitude. *This value is for that frequency only.* There is a constant slope going through this point. +20dB/dec slope if the location is a zero. -20dB/dec slope if the location is a pole.

b. Begin at the starting point. Start with the slope (0 slope if a constant, +20dB/dec slope if zero at origin, -20dB/dec slope if pole at origin). From left to right, at each zero add +20dB/dec to the current slope and at each pole -20dB/dec. Continue through each frequency.

4. Draw the phase plot:

a. Determine the starting value:

Case 1: No pole or zero at the origin:

If constant>0 then starting value = 0^o

If constant<0 then starting value = $\pm 180^o$

Case 2: A pole or zero at the origin:

starting value = $+90^o$ if zero at origin

starting value = -90^o if pole at origin

b. Label each range of frequency according to the following(suggest putting on graph):

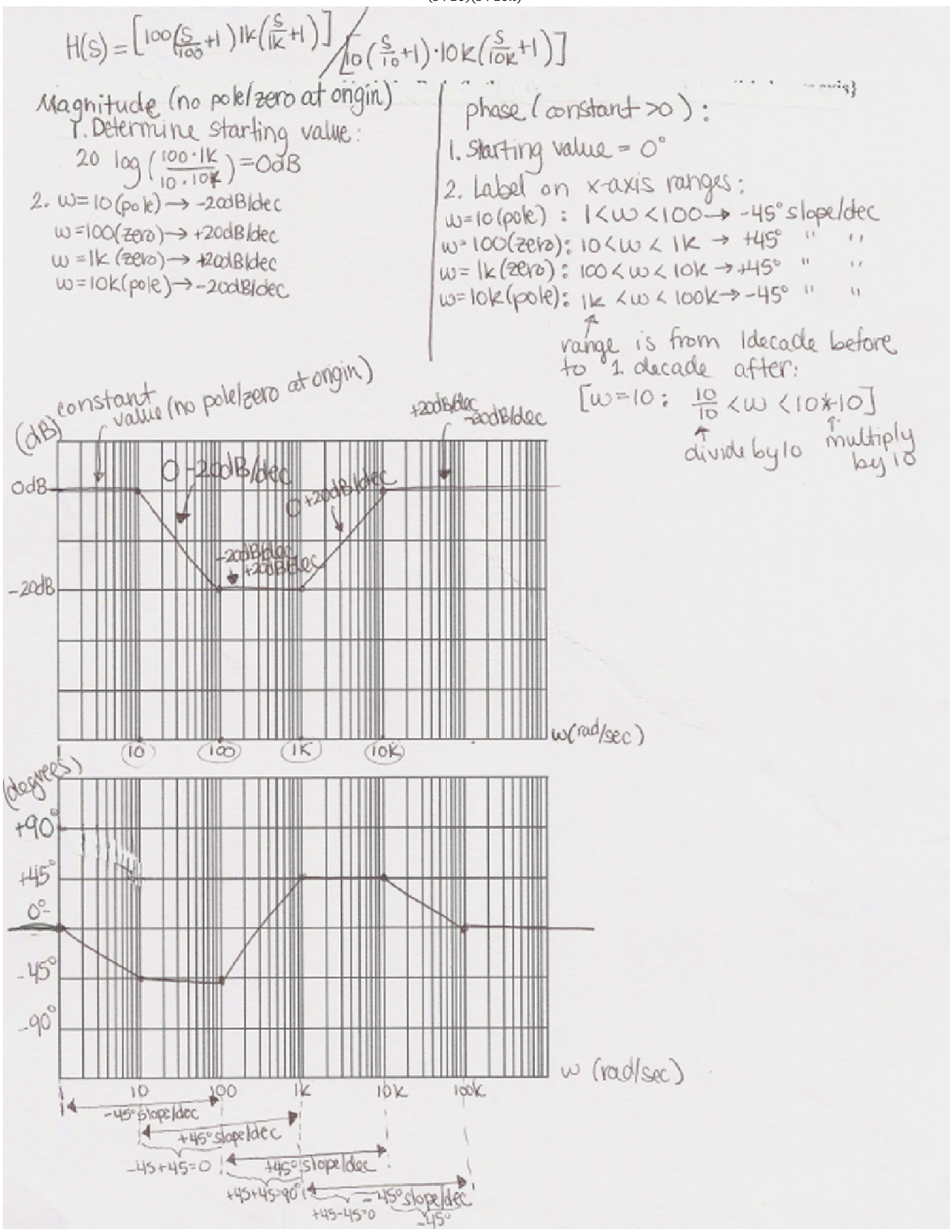
zero => from 1 decade before frequency to 1 decade after frequency: $+45^o$slope/dec

pole => from 1 decade before frequency to 1 decade after frequency: -45^oslope/dec

(eg if ω=10 and is a pole then range is $1<\omega<100$ with a slope of -45^oslope/dec)

c. Look at each frequency range that has a slope. Add all slopes within that region. From left to right: start with starting value and slope of 0, continue until first region of change. Add all slopes within that region. Continue until the end is met. If no slope during a region the slope is constant (0).

Example 8: Sketch the Bode plots for $\boldsymbol{H(s)} = \frac{(s+100)(s+1k)}{(s+10)(s+10k)}$



Example 9: Sketch the transfer function for $\boldsymbol{H(s) = \frac{100(s+100)(s+10)}{(s^2)(s+10k)}}$

Use the straight-line approximation to sketch the Bode (both magnitude & phase) plot for. (label your axis)

$$H(s) = \frac{100(s+100)(s+10)}{s^2(s+10{,}000)} = \frac{100(100)\left(\frac{s}{100}+1\right)(10)\left(\frac{s}{10}+1\right)}{s^2(10k)\left(\frac{s}{10k}+1\right)}$$

magnitude (2 poles at origin)

1. Determine start value: (ω=1)

$$20\log\left[\frac{100(100)(10)}{10k}\cdot\frac{\sqrt{\left(\frac{1}{100}\right)^2+1^2}\cdot\sqrt{\left(\frac{1}{10}\right)^2+1}}{\sqrt{\left(\frac{1}{10k}\right)^2+1}}\right]$$

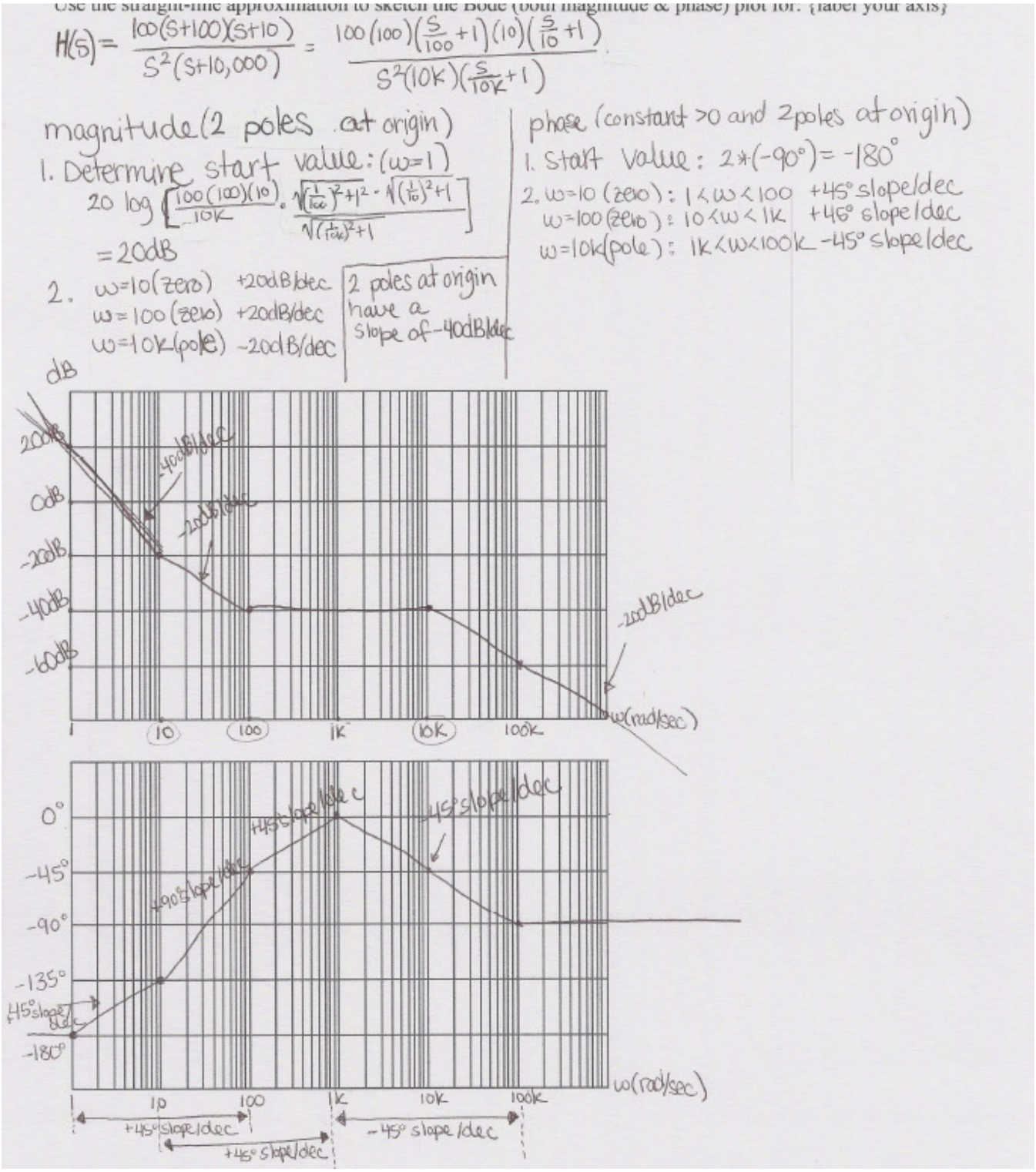
$= 20dB$

2. ω=10 (zero) +20dB/dec
   ω=100 (zero) +20dB/dec
   ω=10k (pole) -20dB/dec

2 poles at origin have a slope of -40dB/dec

phase (constant >0 and 2 poles at origin)

1. Start Value: $2*(-90°) = -180°$
2. ω=10 (zero): $1<\omega<100$ +45° slope/dec
   ω=100 (zero): $10<\omega<1k$ +45° slope/dec
   ω=10k (pole): $1k<\omega<100k$ -45° slope/dec



Example #10 Bode Plots:

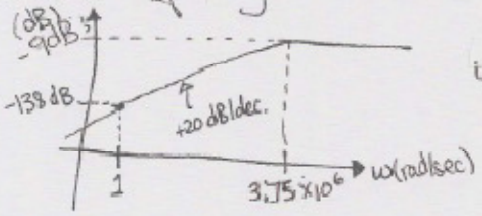
$$\frac{V_o}{V_i} = \frac{4\times10^6 \cdot S}{30(266.7n\,S+1)} = \boxed{\frac{(133n)\cdot S}{(266.7n\cdot S+1)}}$$

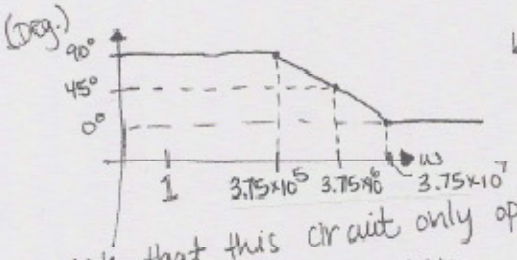
Break frequency $\Rightarrow$ $(266.7n\,s+1) \Rightarrow s = \frac{1}{266.7n} = 3.75\text{Meg}$

$w=1 \Rightarrow 20\log(133n) = -138\text{dB}$ ← with a zero at origin +20dB/dec slope

$w=3.75\text{Meg} \Rightarrow 20\log\left[\frac{133n\times 3.75\text{Meg}}{\sqrt{(266.7n\times3.75\text{Meg})^2+1}}\right]$

$= 20\log(.353) \cong -9\text{db}$



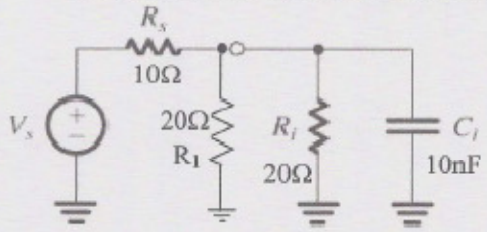


because of zero at origin: start phase at 90°

Note that this circuit only operates at frequencies above 3.75M rad/sec = 597 KHz

Example 11:

Analyze the following circuit to find the transfer function Vi/Vs. Solve the circuit symbolically first and then with their values. Sketch transfer function using a straight-line approximation procedure.



$$\frac{V_i}{V_s} = \frac{\left(R_1 \| R_i \| \frac{1}{C_i s}\right)\cdot V_s}{R_s + \left(R_1 \| R_i \| \frac{1}{C_i s}\right)}$$

$$R_1 \| R_i \| \frac{1}{C_i s} = \frac{1}{\frac{1}{R_1}+\frac{1}{R_i}+\frac{1}{\frac{1}{C_i s}}} = \frac{1}{\frac{R_i}{R_1 R_i}+\frac{R_1}{R_i R_i}+\frac{C_i s R_1 R_i}{R_1 R_i}}$$

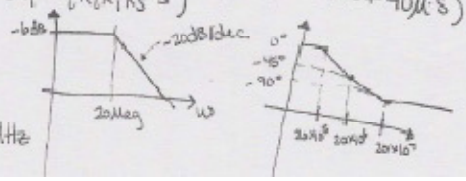
$$= \frac{R_1 R_i}{R_i + R_1 + C_i R_1 R_i \cdot s}$$

$$\frac{V_i}{V_s} = \frac{\frac{R_1 R_i}{(R_i + R_1 + C_i R_i R_1 s)}}{\frac{R_s(R_i + R_1 + C_i R_i R_1 s) + R_1 R_i}{(R_i + R_1 + C_i R_i R_1 s)}}$$

$$\frac{V_i}{V_s} = \frac{R_1 R_i}{(R_1 R_i + R_s R_i + R_s R_1 + C_i R_i R_1 R_s s)} = \frac{400}{(900+100+200+40\mu s)}$$

$$\frac{V_i}{V_s} = \frac{\frac{1}{2}}{\left(1+\frac{s}{20\text{Meg}}\right)}$$

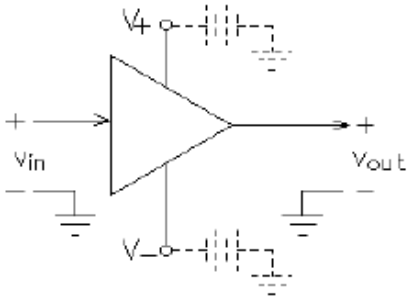
This circuit only operates below 20Meg rad/sec ≅ 3.2 MHz



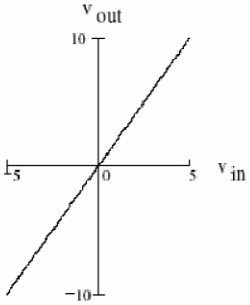
Amplifiers

Purpose: a weak signal is produced by a transducer (ex. Microphone) → too small for reliable processing, so amplify magnitude, i.e. make it larger

Amplifier → basic element of analog circuits



Transfer Characteristic:



voltage "gain" = 2 = $\frac{v_{out}}{v_{in}}$

Batteries or power supplies are rarely shown on the schematic.

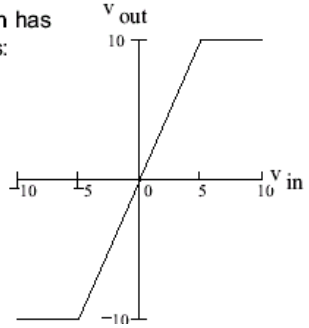
Signal voltages are assumed to be referenced to ground even if the grounds aren't shown.

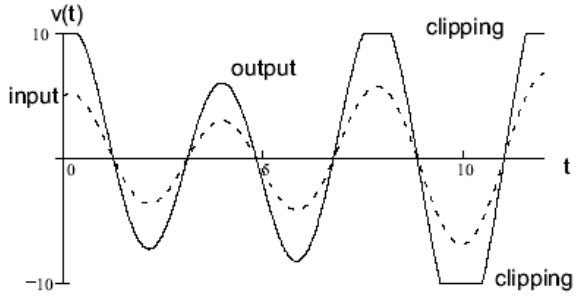
The output of all amplifiers are limited by the power supplies. Usually the limits are less than the power voltages.

Output limits, $L+ \leq V+$, $L- \geq V-$ (usually)

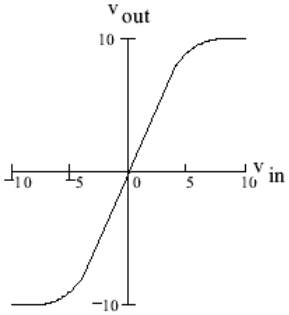
The output can't go beyond these limits no matter what the input does. If you want to avoid the "clipping" distortion in the output, you have to limit the input (make sure it's within an acceptable range).

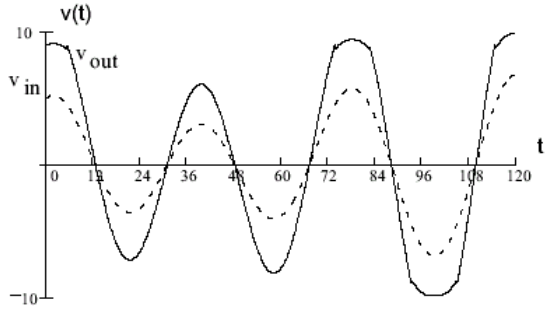
The transfer function has some non-linearities:



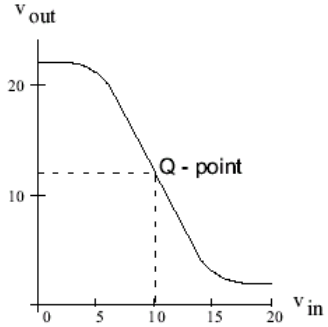


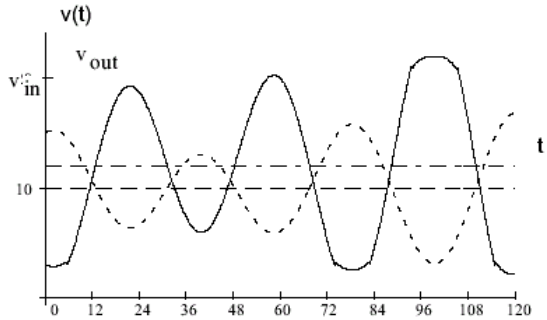
Often the clipping levels are not so well defined





Many of the transistor amplifier circuits that we'll see this semester will have DC offsets and will invert the signal.





The signal is considered the AC (changing) part of the waveform and the DC is called "bias" or the "quiescent - point" (Q - point) of the circuit.

Gain

voltage gain = $A_v = \frac{v_{out}}{v_{in}}$

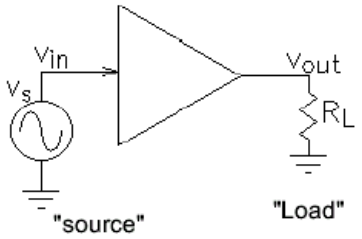
lower -case letters refer to signal values

DC: $\frac{V_{OUT}}{V_{IN}}$ is rarely gain

The two below require a load, otherwise there's no output current, & no output power.

current gain = $\frac{i_{out}}{i_{in}} = \frac{i_L}{i_{in}}$

power gain = $\frac{P_{out}}{P_{in}} = \frac{P_L}{P_{in}}$

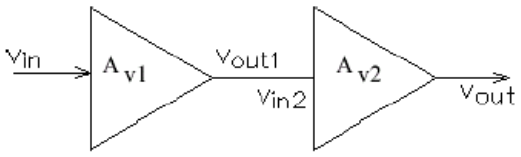


Gains are dimensionless numbers

Gain is just an idealized transfer function.

If only 1 input is shown, assume that other input is grounded.

Two stages

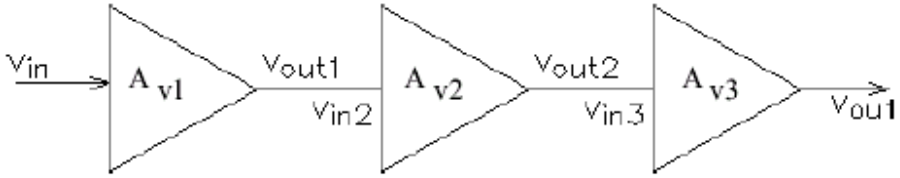


$v_{out} = v_{in2} \cdot A_{v2} = v_{out1} \cdot A_{v2} = v_{in} \cdot A_{v1} \cdot A_{v2}$

$A_{vtotal} = A_{v1} \cdot A_{v2}$

if $A_{v1} := 10$ & $A_{v2} := 4$ then $A_{vtotal} = A_{v1} \cdot A_{v2} = 40$ Same holds for multiple stages

Multiple Stages



Gain expressed as ratios: $A_{vtotal} = A_{v1} \cdot A_{v2} \cdot A_{v3}$

Gain expressed as dB: $A_{vtotal\_dB} = A_{v1\_dB} + A_{v2\_dB} + A_{v3\_dB}$

If $A_{v1} := 20$, $A_{v2} := 8$ & $A_{v3} := 4$ then $A_{vtotal} = A_{v1} \cdot A_{v2} \cdot A_{v3} = 640$

$A_{v1\_dB} := 20 \cdot \log(20)$ $A_{v2\_dB} := 20 \cdot \log(8)$ $A_{v3\_dB} := 20 \cdot \log(4)$

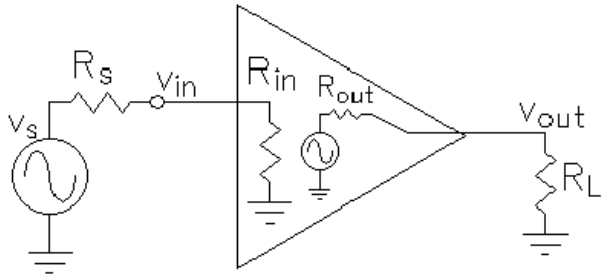
$A_{v1\_dB} = 26.021 \cdot dB$ $A_{v2\_dB} = 18.062 \cdot dB$ $A_{v3\_dB} = 12.041 \cdot dB$

$20 \cdot \log(640) = 56.124 \cdot dB$

$A_{vtotal\_dB} = A_{v1\_dB} + A_{v2\_dB} + A_{v3\_dB} = 56.124 \cdot dB$

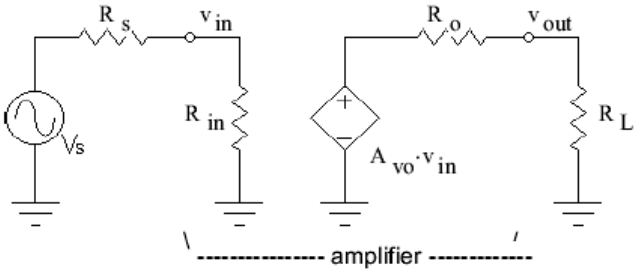
Amplifier Models

Up until now we haven't worried about the currents into and out-of our amplifiers. In reality, any source, including the amplifier, will have a source resistance (R_s or Z_s for the source and R_{out} or Z_{out} for the amp). Also any amplifier will let a little signal current flow in (modeled by an R_{in} or Z_{in}).



At this point, the triangle symbol gets to be a little cumbersome and is dropped.

Basic amplifier model:
Voltage amplifier
with source and load



Notice the dependent source inside the amplifier

A_{vo} is the "unloaded" gain or "open-circuit" gain because

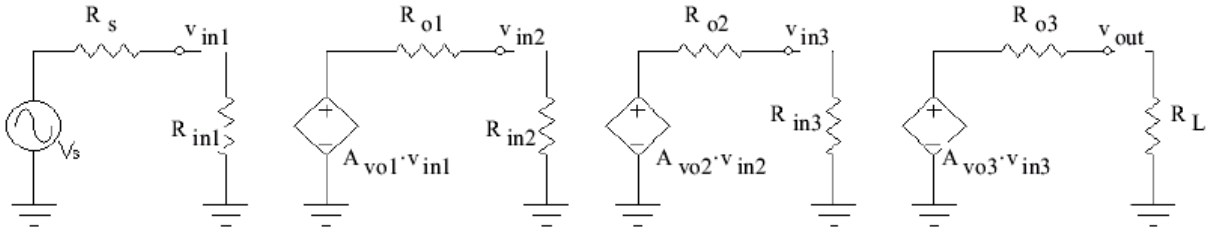
$A_{vo} \cdot v_{in}$ would be the output if there were no load resistor ($R_L = \infty$).

Overall gain: $$\frac{v_{out}}{v_s} = \frac{R_{in}}{R_s + R_{in}} \cdot A_{vo} \cdot \frac{R_L}{R_o + R_L}$$

or, in dB: $$20 \cdot \log\left(\frac{v_{out}}{v_s}\right) = 20 \cdot \log\left(\frac{R_{in}}{R_s + R_{in}}\right) + 20 \cdot \log\left(A_{vo}\right) + 20 \cdot \log\left(\frac{R_L}{R_o + R_L}\right)$$

- dB + dB - dB

Three stage amplifier



Overall gain: $$\frac{v_{out}}{v_s} = \frac{R_{in1}}{R_s + R_{in1}} \cdot A_{vo1} \cdot \frac{R_{in2}}{R_{o1} + R_{in2}} \cdot A_{vo2} \cdot \frac{R_{in3}}{R_{o2} + R_{in3}} \cdot A_{vo3} \cdot \frac{R_L}{R_{o3} + R_L}$$

Desirable characteristics

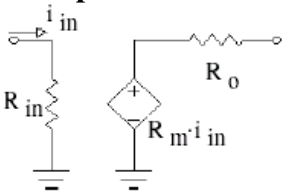
Want R_{in} --> ∝ High input resistance means the amplifier will not load down the source or previous stage.

Want R_c --> 0 Low output resistance means the amplifier supply lots of current to the load or next stage.

High R_{in} and low R_c means good current gain. In fact these terms are used much more often than "current gain".

At higher frequencies it may become more important to match impedances than to maximize R_{in} & minimize R_c.

Other Amplifier Models

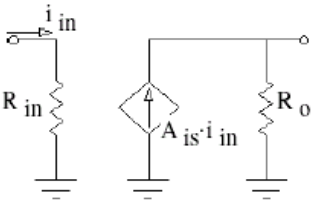


Transresistance amplifier

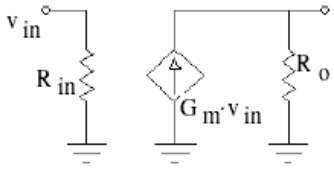
Instead of $A_{vc} = \frac{v_o}{v_{in}}$ (unloaded)

This amp has $R_m = \frac{v_o}{i_{in}}$ (unloaded)

$\frac{V}{I} = \Omega$, that's why it's called transresistance



Current amplifier



Transconductance amplifier

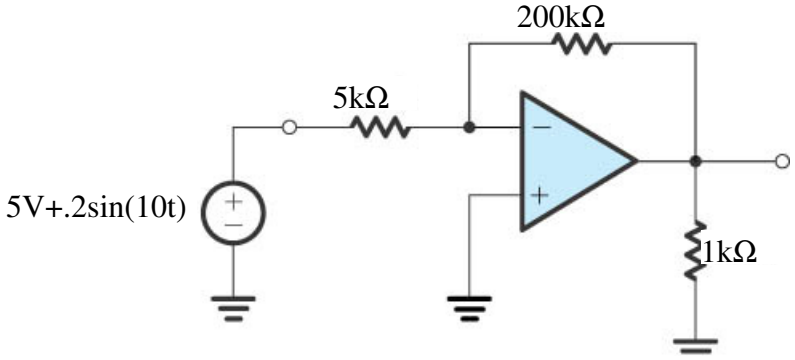
Insterad of $A_{vo} = \frac{v_o}{v_{in}}$ (unloaded)

This amp has $G_m = \frac{i_o}{v_{in}}$ (unloaded)

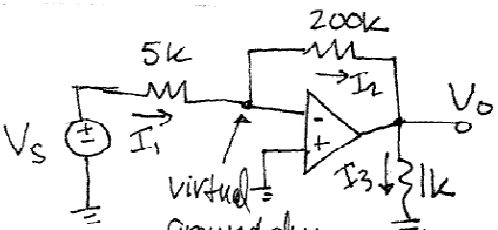
$\frac{I}{V}$ = conductance, that's why it's called transconductance, units mho or seimen

Procedure for solving ideal op-amp circuits:
1. If the noninverting terminal of the op-amp is at ground potential, then the inverting terminal is at virtual ground. Sum currents at this node, assuming zero current enters the op-amp itself.
2. If the noninverting terminal of the op-amp is not at ground potential, then the inverting terminal voltage is equal to that at the noninverting terminal. Sum currents at the inverting terminal node, assuming zero current enters the op-amp itself.
3. For the ideal op-amp circuit, the output voltage is determined from either step 1 or step 2 above and is independent of any load connected to the output terminal.

Example 12:
For the circuit below, assume an ideal op-amp. Find the currents through all branches and the voltages at all nodes. Since the current supplied by the op amp is greater than the current drawn from the input signal source, where does the additional current come from?



• The additional current is supplied from the supply power for the op amp.



$I_1 = I_2$

$I_1 = V_s/5k = \dfrac{5V + 0.2\sin(10t)}{5k}$

$I_1 = I_2 = 1mA + 40\mu(\sin(10t))$

$V_o = -I_2(200K)$

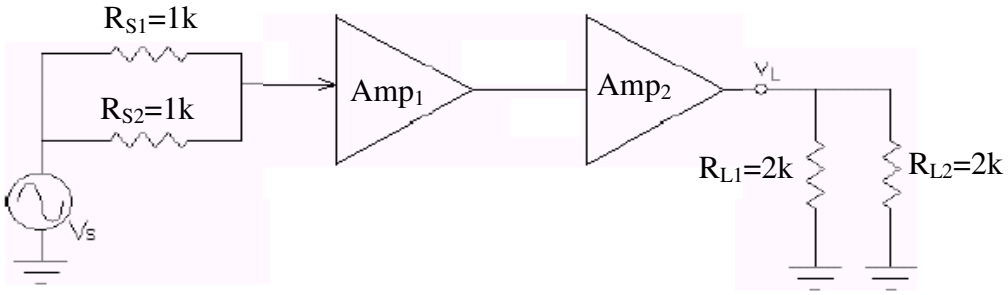
$\therefore V_o = -1m(200k) - 40\mu(200k)\sin(10t)$

$V_o = -200V - 8\sin(10t)$

$I_3 = \dfrac{V_o}{1k}$

$I_3 = -200mA - 8mA\sin(10t)$

Example 13: Use the following circuit.



You are given: Amp_1 has an $A_{vo}=5$, $R_i=500$, $R_o=12k$ Amp_2 has an $A_{vo}=20$, $R_i=3k$, $R_o=4k$

(a) Find $A_v=\frac{v_L}{v_s}$ Express your answer as a ratio in dB.

(b) Evaluate the overall current gain($\frac{i_L}{i_s}$). Express your answer as a ratio and in dB form.

(c) Evaluate the overall power gain ($\frac{P_L}{P_s}$). Express your answer as a ratio and in dB form

(d) If Vs=40mV$_{pp}$. What is the output voltage (peak-to-peak) at V_L?

(e) What value would R_o for Amp_2 need to be changed in order to get Av = 4?

1. $R_S=500\Omega$ 12k 4k V_L

V_s i_s V_1 500 $5V_1$ V_2 3k $20V_2$ i_L $R_L=1k=(2k\|2k)$

$V_L=\frac{20V_2\cdot 1k}{5k}=4V_2$

$V_2=\frac{5V_1\cdot 3k}{15k}=V_1$

$V_1=\frac{V_s(500)}{1k}=\frac{V_s}{2}$

$\left(\frac{V_L}{V_s}=\frac{1k(20)}{5k}\left(\frac{3k(5)}{15k}\right)\left(\frac{500}{1k}\right)\right.$
$\left.=2\,V/V\cong 6dB\right)$

(a) $\therefore V_L=4(1)\left(\frac{V_s}{2}\right)\Rightarrow \boxed{\frac{V_L}{V_s}=2\,V/V\cong 6\,dB}$

Once one quantity is found, the others can be found by their relationship to v_L and v_s $\Rightarrow$

(b) $\frac{V_L}{R_L}=i_L \Rightarrow V_L=(i_L\cdot R_L)$

$v_s=i_s(1k)$

$\frac{V_L}{V_s}=2=\frac{i_L(1k)}{i_s(1k)}$ $\therefore \boxed{\frac{i_L}{i_s}=2\,A/A\cong 6\,dB}$

(c) $P_L=i_L\cdot V_L$, $P_s=i_s\cdot V_s$

$\frac{P_L}{P_s}=\frac{i_L\cdot V_L}{i_s\cdot V_s}=2\cdot 2=\boxed{4\,V/V\cong 12dB}$

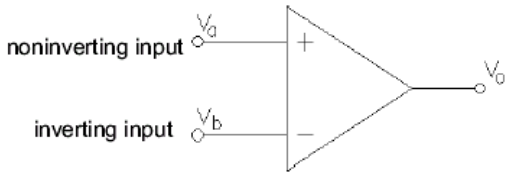
(d) $V_s=40mV_{pp}\Rightarrow \frac{V_L}{V_s}=2$ $\therefore V_L=2(40mV_{pp})=\boxed{80mV_{pp}}$

(e) $A_v=4=\frac{20\cdot 1k}{1k+R_o}(1)(\frac{1}{3})\Rightarrow \boxed{R_o=1500\,\Omega}$

Operational Amplifier:

An operational amplifier is basically a complete high-gain voltage amplifier in a small package. Op-amps were originally developed to perform mathematical operations in analog computers, hence the odd name. With the proper external components, the operational amplifier can perform a wide variety of "operations" on the input voltage. It can multiply the input voltage by nearly any constant factor, positive or negative, it can add the input voltage to other input voltages, and it can integrate or differentiate the input voltage. The respective circuits are called amplifiers, summers, integrators, and differentiators. Op-amps are also used to make active frequency filters, current-to-voltage converters, voltage-to-current converters, current amplifiers, voltage comparators, etc. etc.. These little parts are so versatile, useful, handy, and cheap that they're kind of like electronic Lego blocks — although somewhat drably colored.

Op-amp characteristics



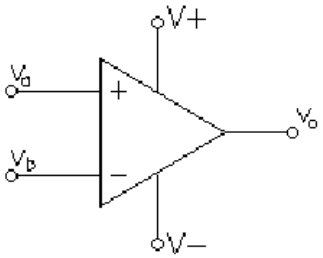
An op-amp has two inputs

Amplifies the voltage *difference* between those two inputs.

$$v_o = G\cdot(v_a - v_b)$$

G = voltage gain of the op-amp

G is usually very big, ≥ 100,000



The op-amp must be connected to external sources of power, V+ and V-.

The output voltage is limited by the power supply voltages.

$V- \le v_o \le V+$ (Usually even more limited than this)

So: $V- \le G(v_a - v_b) \le V+$

If the op amp is in its ***active*** region:

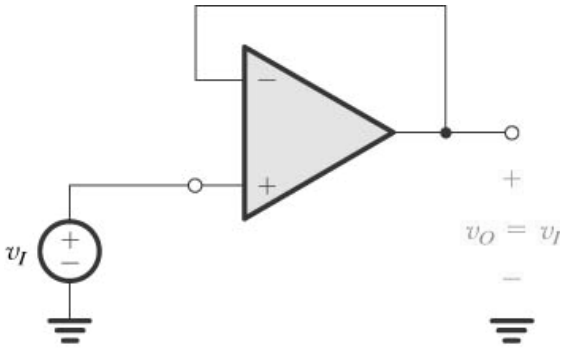
Since G is very big, $(v_a - v_b)$ must be very small, in fact the usual assumption is that

$V_a \sim V_b$ Active region ONLY

Op Amp Configurations:

1. Voltage Follower => $V_o=V_i$

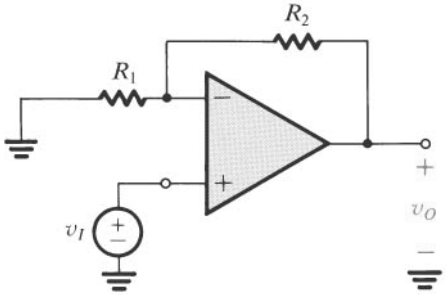
Used as a current amplifier



(a)

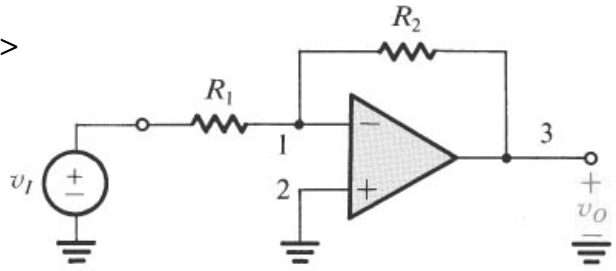
2. Noninverting amplifier =>

$$v_o=\left(\frac{R_2}{R_1}+1\right)\cdot v_i$$



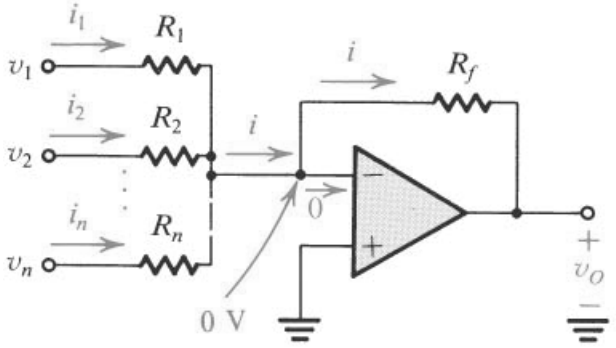
3. Inverting amplifier =>

$$v_o=-\frac{R_2}{R_1}\cdot v_i$$



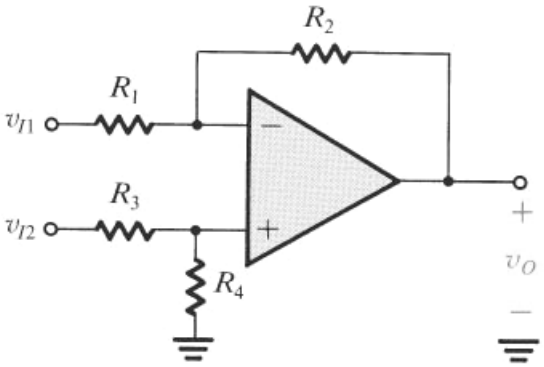
4. Summer =>

$$v_o = -\left(\frac{R_f}{R_1}v_1 + \frac{R_f}{R_2}v_2 + \frac{R_f}{R_3}v_3 + \cdots \frac{R_f}{R_n}v_n\right)$$



5. Differential Amplifier =>

$$v_o = \left(\frac{R_2}{R_1}(v_2 - v_1)\right)$$

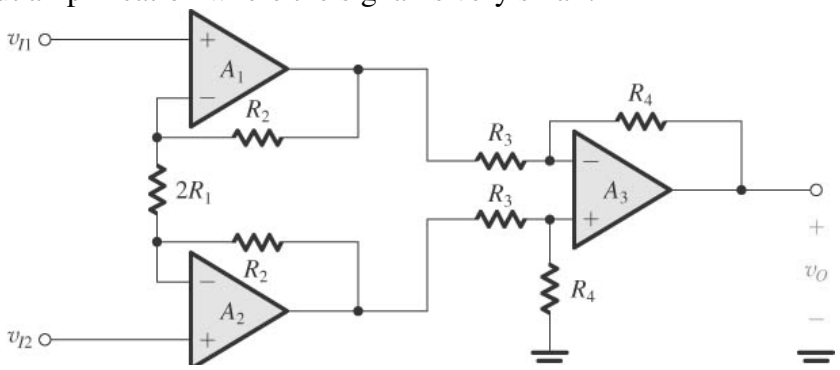


$$v_O = -\left(\frac{R_f}{R_1}v_1 + \frac{R_f}{R_2}v_2 + \cdots + \frac{R_f}{R_n}v_n\right)$$

6. Instrumentation Amplifier =>

* This amplifier configuration can have large gain because of the two stages. Lower noise. Typically used for sensors output amplification where the signal is very small.

$$v_o = \left(1 + \frac{2R_2}{R_1}\right)\left(\frac{R_4}{R_3}(v_2 - v_1)\right)$$



Internally Compensated Op Amp

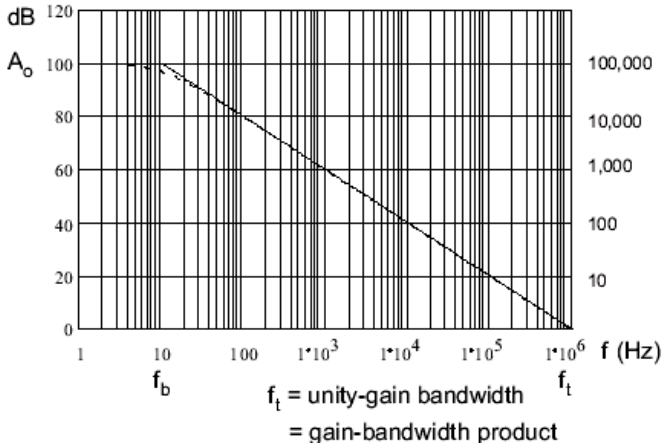
This is the open-loop gain (A) of a LM741 (worst case). Usually f_b and f_t are a little higher than those shown here, especially in better quality op-amps. you probably measured f_t somewhere between 1 & 2 MHz in the lab, even for a 741. They normally exceed their specifications a little.

$$A = \frac{A_o}{1 + j\cdot\frac{f}{f_b}} \simeq \frac{A_o \cdot f_b}{j\cdot f} = \frac{f_t}{j\cdot f}$$

above f_b

Other symbols for f_t: f_T, f_U, f_{Unity}, GB, Bandwidth

A (open-loop) gain



f_t = unity-gain bandwidth
= gain-bandwidth product

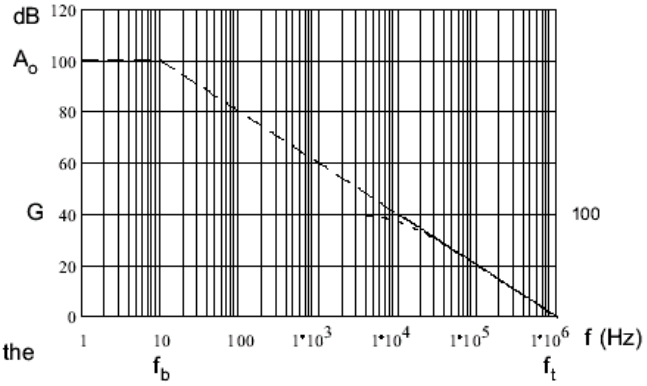
– gain-bandwidth product

Closed-loop (with negative feedback) Frequency Response

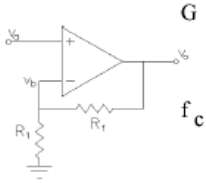
If your op-amp circuit is designed to have a gain of 100 (40dB) then a very good estimate of its frequency response is shown at right. To find the bandwith of your amplifier, you take the gain-bandwith product (f_t) and divide by the gain of your amp.

$$f_c \simeq \frac{A_o \cdot f_b}{G} = \frac{f_t}{G}$$

G = ideal gain of amplifier

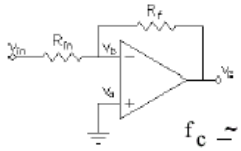


If you plug $A = \frac{f_t}{j \cdot f}$ into the finite-gain equations on the last page, you'll find that this estimate is exact for a noninverting amplifier, but not quite right for an inverting amplifier.



$$G = 1 + \frac{R_f}{R_1}$$

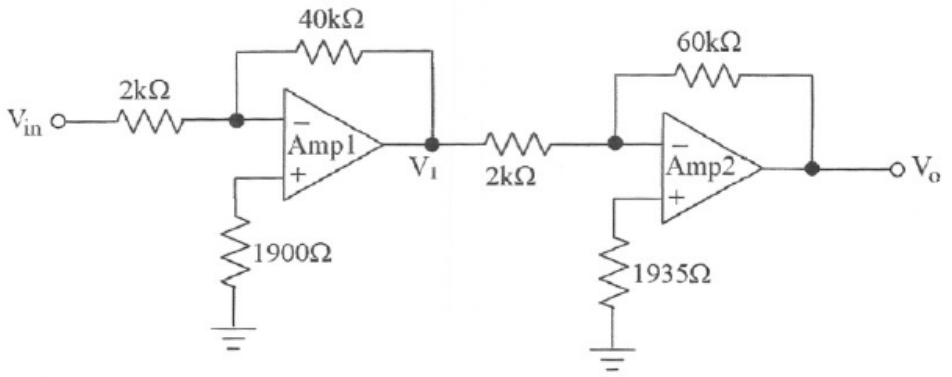
$$f_c \simeq \frac{A_o \cdot f_b}{G} = \frac{f_t}{G} = \frac{f_t}{1 + \frac{R_f}{R_1}}$$



$$G = \frac{R_f}{R_{in}}$$

$$f_c \simeq \frac{A_o \cdot f_b}{G+1} = \frac{f_t}{G+1} = \frac{f_t}{1 + \frac{R_f}{R_{in}}}$$

If G > 20 or so, you can usually neglect the + 1 in the denominator



Use the attached datasheet information. Amp1 is a CA3140 and Amp2 is an LM741.

(a) State each amplifiers frequency response transfer function (V_1/V_{in} and V_o/V_1)
(b) State the overall transfer function (V_o/V_{in})
(c) Write the equation to solve for the overall f_{3dB} of the circuit below. {Note you do not need to solve it}

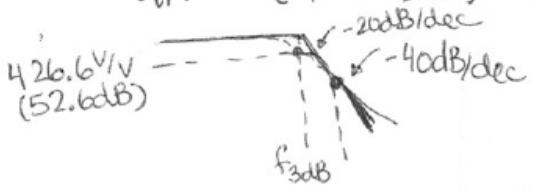
a) Amp 1 $\Rightarrow$ $\frac{V_1}{V_{in}} = -\frac{20}{(1+jf/200k)}$

$f_{3dB} = \frac{4MHz}{(20)} = 200k$ ← only for Amp1

Amp2 $\Rightarrow$ $f_{3dB} = \frac{1M}{(30)} = 33.3k$

$\frac{V_o}{V_1} = \frac{-33.3k}{(1+jf/33.3k)}$

b) $\frac{V_o}{V_{in}} = \frac{-20}{(1+jf/200k)} \cdot \frac{-30}{(1+jf/33.3k)} = \frac{+600}{(1+jf/200k)(1+jf/33.3k)}$



600dB $\Rightarrow 20\log(600) = 55.6dB$

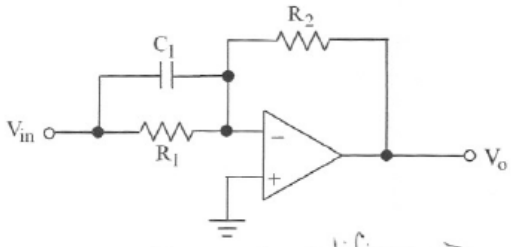
$55.6dB - 3dB = 52.6dB$

$52.6dB = 10^{\left(\frac{52.6}{20}\right)} = 426.6\ V/V$

c) $426.6 = \frac{600}{\sqrt{1^2+\left(\frac{f_{3dB}}{200k}\right)^2} \cdot \sqrt{1^2+\left(\frac{f_{3dB}}{33.3k}\right)^2}}$

Example 15:

Analyze the circuit below to obtain the transfer function, V_o/V_{in}. Assume ideal opAmp.



Inverting amplifier $\Rightarrow$

$$\frac{V_o}{V_{in}} = -\frac{R_2}{R_1 \| 1/C_1 s}$$

$$R_1 \| 1/C_1 s = \left[\frac{R_1(1/C_1 s)}{R_1 + \frac{1}{C_1 s}}\right]\frac{C_1 s}{C_1 s} = \frac{R_1}{(R_1 C_1 s + 1)}$$

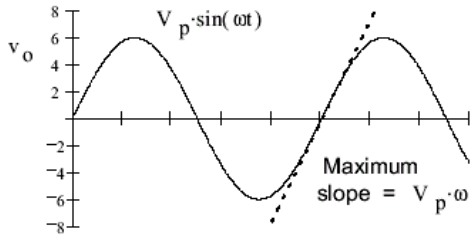
$$\therefore \quad \frac{V_o}{V_{in}} = -\frac{R_2(R_1 C_1 s + 1)}{R_1}$$

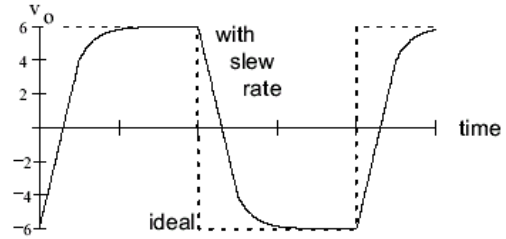
Op Amps output voltage can only change so fast. The maximum rate of change is called slew rate (SR)

Slew Rate continued

A square wa ing step function:

What if your output is a sine wave?

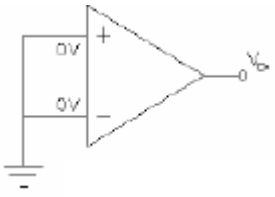


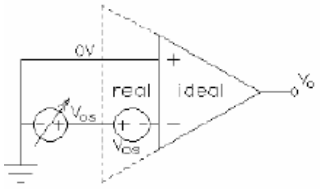


must be less than the slew rate, so: $f_{max} = \frac{SR}{V_p \cdot 2 \cdot \pi} = \frac{SR}{V_{pp} \cdot \pi}$

DC Imperfections:

Offset Voltage (Vos) The voltage for the output below should be zero, but almost always is not. The value when both inputs are grounded is called the voltage offset, Vos. To compensate for this offset =>





a fixed voltage can be placed at the input as shown below. Several op amps have an extra terminal in the package (offset null terminal) that can be adjusted so that the output will read zero when the inputs are both grounded. This value is also affected by temperature and so can not always be compensated.

Input bias currents (I_{B1}, I_{B2}, ave=I_B) The real op amp has currents as seen below. ($V_o = I_{B1} * R_f$)

The cure (if $I_{B1} = I_{B2}$):

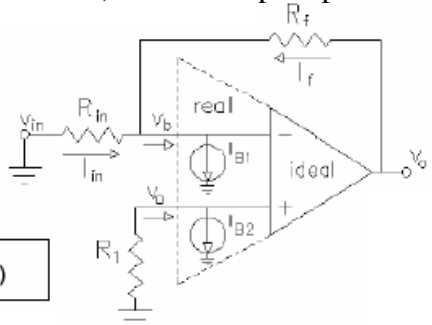
If $v_o = 0$

$v_b = (R_f \| R_{in}) I_{B1}$

if $R_1 = (R_f \| R_{in})$

then $v_a = (R_f \| R_{in}) I_{B2}$

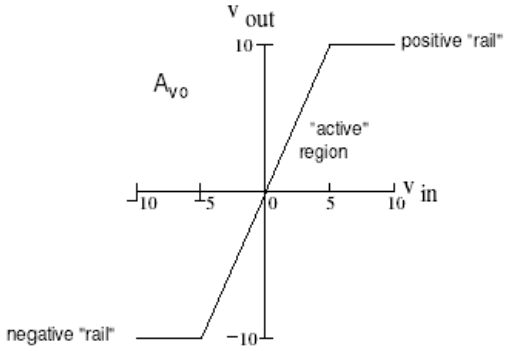
So: make $R_1 = (R_f \| R_{in})$

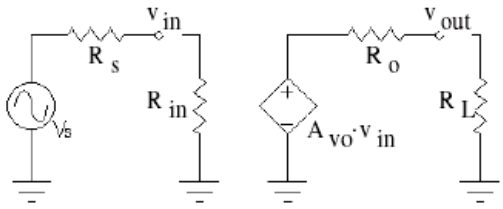


To reduce input bias current affect=> *match impedances seen at each terminal to be the same.*

Clipping

All real amplifiers will clip the output signal if the input is too big. Only one part in the model can possible account for the clipping-- a nonlinear A_{vo}.





Clipping level at the output (v_{out}) is less than that of A_{vo} ($\pm$ 10V) because of the R_c, R_L voltage divider.

The maximum allowable $v_{in} = \dfrac{10 \cdot V}{A_{vo}}$

The maximum allowable v_s is greater than this because of the R_S, R_{in} voltage divider.

Op Amp Imperfections Summary:

1. **Clipping**
   - **Increase DC voltage supply (increases power consumption)**
   - **Decrease input signal**
2. **Slew Rate**

$$f_{max} = \frac{SR}{V_p \cdot 2 \cdot \pi} = \frac{SR}{V_{pp} \cdot \pi}$$

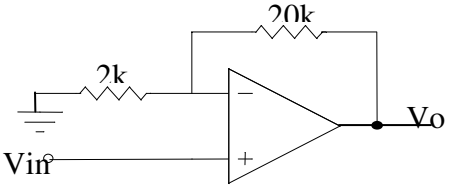
3. **Voltage offset**
   - **Use external voltage source to compensate**
4. **Input Bias Current**
   - **Match impendances at both inputs**

Example 16:

You are given the following characteristics for a real amplifier along with the circuit below.

Op amp Characteristics:

Input offset voltage:	V_{ios}=4.0mV	Open-loop gain:	A_o=100dB
Input offset current:	I_{os}=200nA	Unity-gain bandwidth:	f_T=2MHz
Input bias current:	I_{iB}=600nA	Output swing limits:(within 2V of supply)	$\pm$ 15V
Input resistance:	R_i=1MΩ	Slew rate:	4V/μs
Output resistance:	R_o=50Ω		



(a) What is the voltage gain of the circuit? Ignore Ri and Ro and only consider the finite gain, A_o.

(b) For small input signals, what is the 3db bandwidth of the circuit (in Hz)?

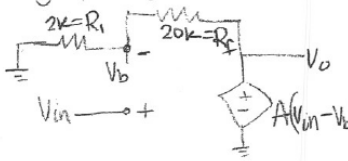
(c) For an output signal of 10Vpp, considering the slew rate effect, what is the limiting frequency of the circuit?

(d) What is the maximum peak-to-peak output you can get without clipping?

(e) Find the effect of the input offset voltage (v_{in}=0V). (i.e. find output value when input =0)

(f) How should the circuit be modified to minimize the effect of the input bias current? Show the modification on the schematic above and find the value of any added parts.

(a) Ignore R_i since it is large and R_o since it is small.



$V_b = V_{in} = \frac{V_o(R_1)}{R_1+R_f}$

$A\left(V_{in} - \frac{V_o(R_1)}{R_1+R_f}\right) = V_o$

$\frac{V_o}{A} = \left[V_{in} - \frac{V_o(R_1)}{R_1+R_f}\right] \Rightarrow V_o\left[\frac{1}{A} + \frac{R_1}{R_1+R_f}\right] = V_{in}$

$\therefore \frac{V_o}{V_{in}} = \frac{1}{\frac{1}{A} + \frac{R_1}{R_1+R_f}}$ {when A>> then $\frac{V_o}{V_{in}} = \left[\frac{R_1+R_f}{R_1}\right]$}

$A = 100dB = 10^{100/20} = 100K\ V/V$

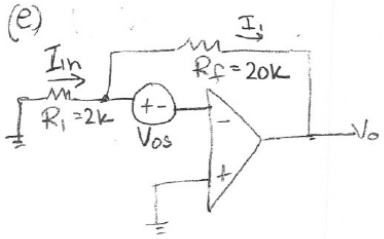
$\frac{V_o}{V_{in}} = \frac{1}{\frac{1}{100K} + \frac{2K}{22K}} = \boxed{10.999}$ without A $\Rightarrow \frac{V_o}{V_{in}} = \boxed{11V}$

(b) $f_c = \frac{f_T}{gain} = \frac{2MHz}{10.999} \cong \boxed{182KHz}$

(c) $f_{max} = \frac{SR}{V_{pp}\cdot\pi} = \frac{4V/\mu s}{10\cdot V\cdot\pi} = \boxed{127KHz}$

(d) $2(\pm 15V) = \boxed{30V_{pp}}$

(e)

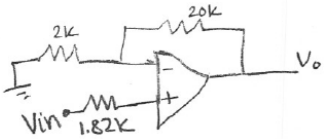


$I_{in} = \frac{-V_{os}}{R_1} = I_1$

$\frac{V_{os}-V_o}{R_f} = \frac{-V_{os}}{R_1}$

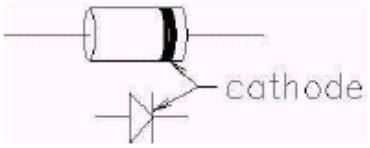
$R_f V_{os}\left(\frac{1}{R_f} + \frac{1}{R_1}\right) = \frac{V_o}{R_f} = V_{os}\left(1 + \frac{R_f}{R_1}\right) = 4m\left(1 + \frac{20K}{2K}\right) = \boxed{44mV}$

(f) Both terminals should have the same R seen by that terminal $\Rightarrow$ (-) terminal sees $(R_1 \| R_f) = 1.82K$



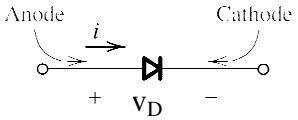
What are diodes?

Definition: A diode is a semiconductor device that passes current only in 1 direction. A "one-way" current valve



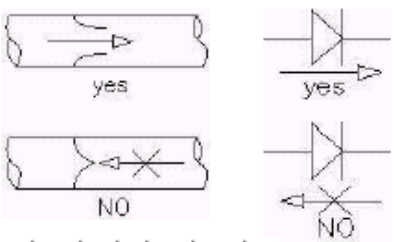
Ideal Diode

Circuit Symbol:



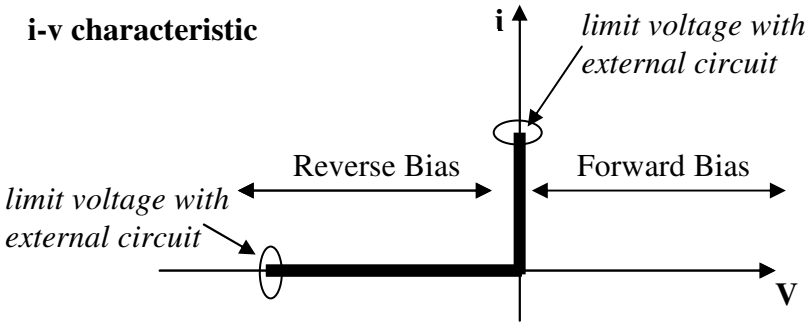
(a)

- Like resistors, they have 2 terminals



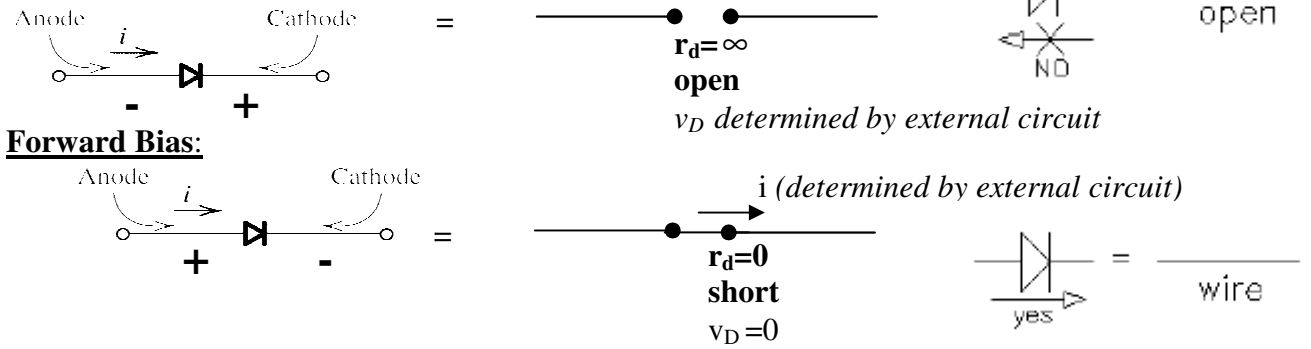
Mechanical check valve Diode

i-v characteristic



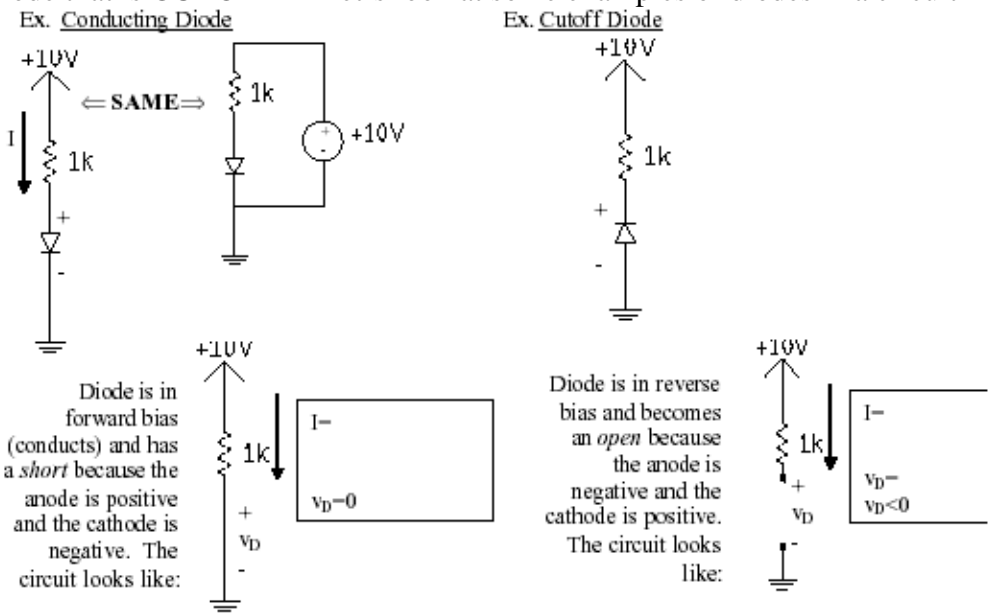
- Unlike resistors which have a linear relationship, the diode has a **nonlinear** characteristic

Reverse Bias:



Forward Bias:

External circuit – needs to limit the forward current through a diode that is ON and limit the reverse voltage across a diode that is CUTOFF → Let's look at some examples of diodes in a circuit



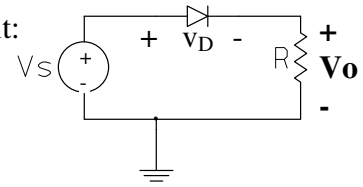
Summary of 2 modes of operation for Diode:

Forward-Biased	**Reverse-Biased**
Conducting (ON)	Cutoff (OFF)
Short Circuit	Open Circuit
i=value, v_D=0	i=none, v_D=open

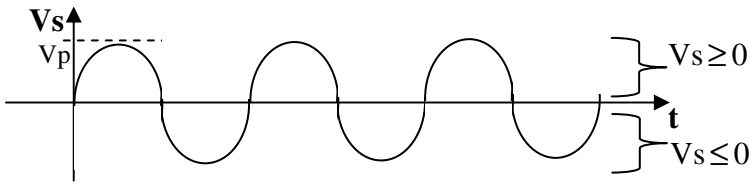
Example: Rectifier

- The word "rectify" means to make unidirectional → keep this in mind
- Makes use of nonlinear characteristic of diodes
- Assume ideal diode

1). Circuit:

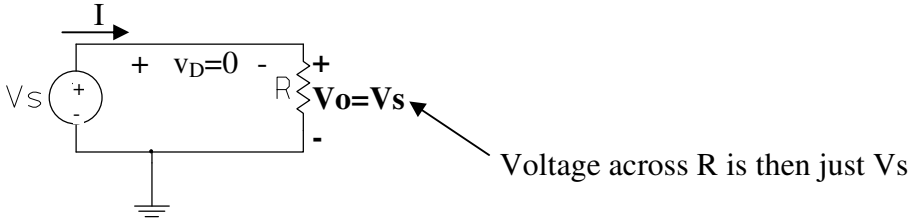


2). Input signal Vs: *sinusoid*

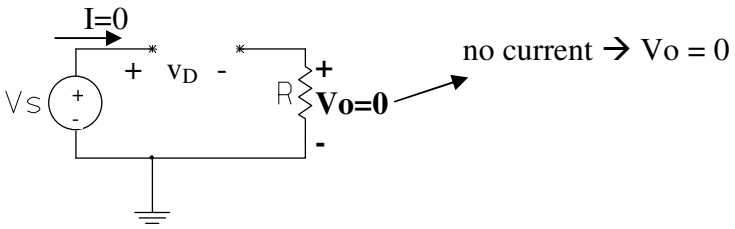


Two regions to consider:

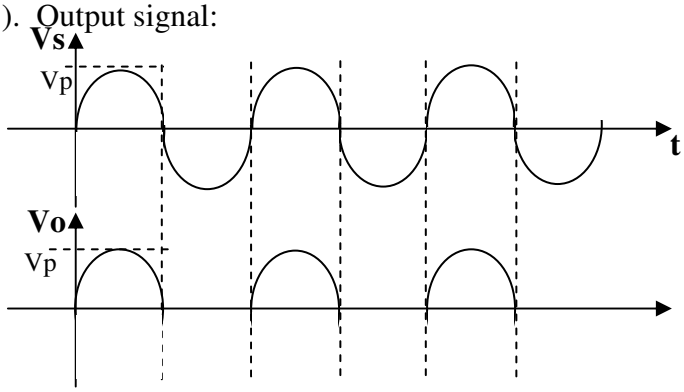
3). Vs>0 – ***Will diode be conducting or cutoff?*** Conducting because current flows through diode in its forward direction (or look at inconsistency if you assume cutoff)



4). Vs ≤ 0 – ***Will diode be conducting or cutoff?*** Cutoff (this is consistent)



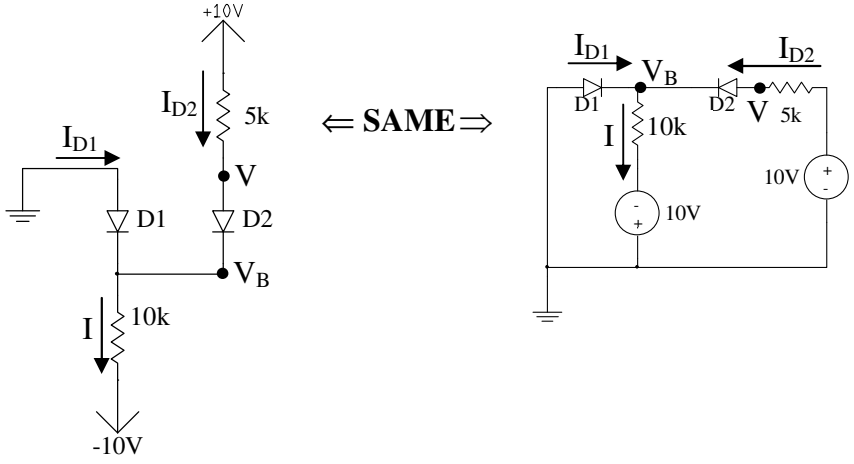
5). Output signal:



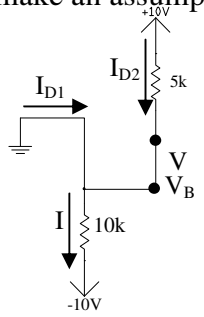
6). Used to convert ac→ dc Vs is ac with 0 average value. Can see Vo has a dc component.

t

Example 17: Two diodes



Find I and V. Assume the diodes are ideal.
Not always obvious if diodes are ON or OFF → make an assumption and test it!
Assume both are ON for starters → Short them



$V_B=0$
$V=0$
$I_{D2}=\frac{10-0}{5k}=2\text{mA}$
$I=\frac{0-(-10)}{10k}=1\text{mA}$
$I_{D1}+I_{D2}=I \Rightarrow I_{D1}=-I_{D2}+I=-2\text{m}+1\text{m}=-1\text{mA}$

Is this possible?
Diode ON: Need I>0 for V=0

We have V = 0, but I < 0 → contradiction
(Also think of it as saying a negative current is flowing through D1 → not possible)

Instead, say D1 is OFF and D2 is ON. Then $I_{D2}=\frac{10-(-10)}{15k}=1.33\text{mA}$
Voltage at B: $V = V_B = -10+10\text{k}(1.33\text{mA})=3.3\text{V}$

I = 0 and D1 is Reverse-biased
Is this consistent?
check:

D1: $I_{D1}=0$

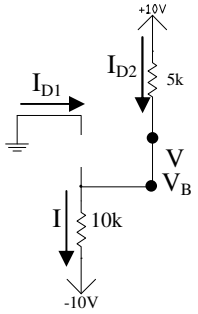
0V + v_{D1} - 3.3V

$v_{D1}=-3.3\text{V}<0 \Rightarrow I_{D1}=0$

D2: $I_{D2}=1.33\text{mA}$

10V + v_{D2} - 3.3V

$I_{D2}>0 \Rightarrow v_{D2}=0$



Think of finding I and V like solving a puzzle…

Method for analyzing diode circuit:

1). Assume each diode is either ON or OFF

2). Find i_d and v_d for each diode to see:

- Is solution consistent with

  OFF: $v_D \leq 0$ (ideal) or $v_D \leq v_{DO}$ (real) $\Rightarrow I_D=0$

  ON: $I_D>0 \Rightarrow v_D=0$(ideal) or $v_D=v_{DO}$ (real)

*Make sure you are looking at voltage across the diode and current through the diode when you are checking for this! NOT the I and V necessarily that you were asked to find.

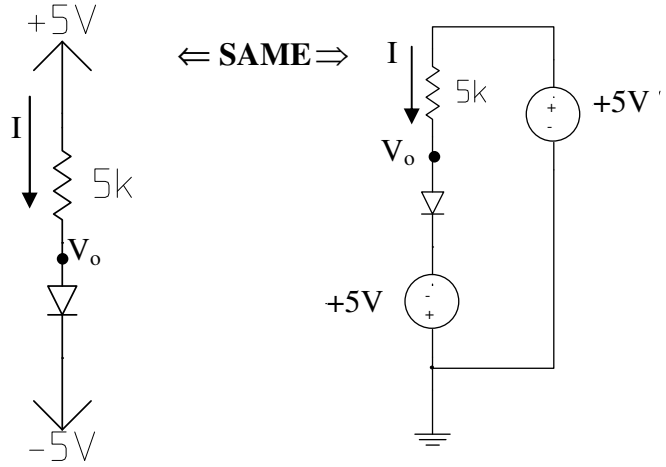
3). If so, assumption was correct (check consistency) – only one solution possible, so STOP

4). Find the requested I and/or V

5). If not, start again with new assumption (NOTE: I and V values are no longer valid, so you have to discard those previous values)

Example 18

Find I and Vo



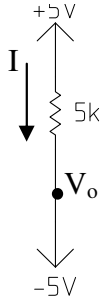
Assume "ON":

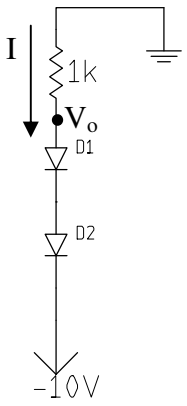
Vo=-5V

$I=\frac{5-(-5)}{5k}=2mA$

check:

$I_D>0 \Rightarrow v_D=0$





Find I and Vo

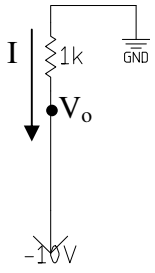
Assume both "ON"

Vo=-10V

$I=\frac{0-(-10)}{1k}=10mA$

check:

$I_D>0 \Rightarrow v_D=0$



Analysis of Diode Circuits

For hand calculations, we have 4 main models to use:

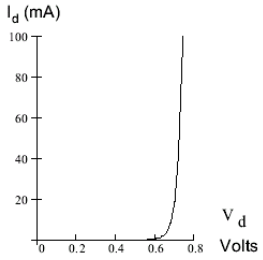
1). Ideal model for diode:
Reverse Bias: OFF/cutoff/open circuit
Forward Bias: ON/conducting/short circuit

2). Use full diode equation: $i_D = I_S(e^{V_D/nV_T} - 1)$

(Reverse Bias: i_D ~= $-I_S$)

Forward Bias: $i_D \approx I_S(e^{V_D/nV_T})$

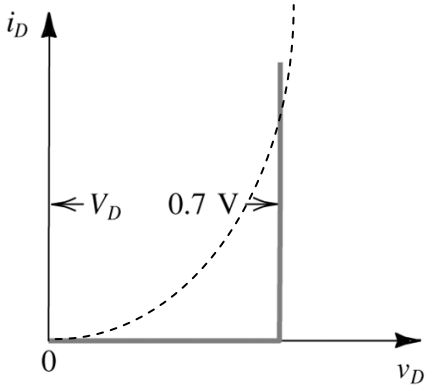
Use an iterative method and solve



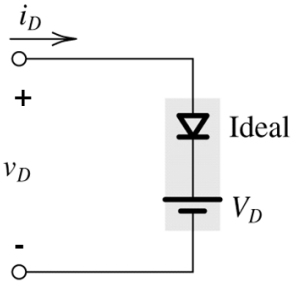
3). ***Constant-voltage-drop model*** for diode (apply for forward bias):

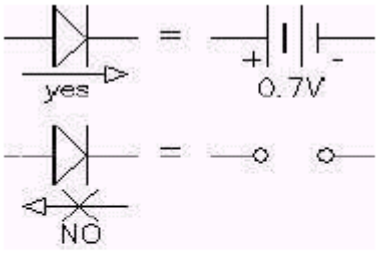
- Replace real diode with an ideal diode and a voltage drop V_D

i-v characteristic

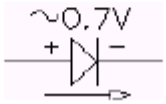


model



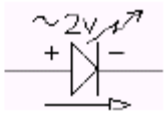


silicon diode



light-emitting diodes (LEDs) are modeled by 2v drop in forward direction:

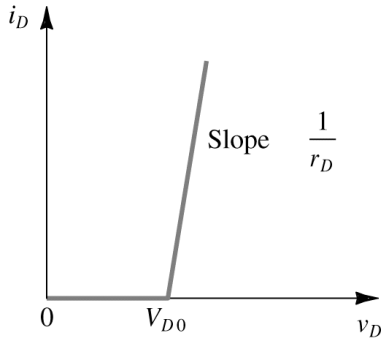
LED



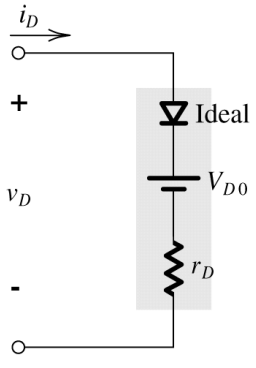
4). Piecewise-linear model for diode (apply for FB):

- Replace real diode with an ideal diode, a voltage drop V_{D0}, and a resistor, r_D

i-v characteristic



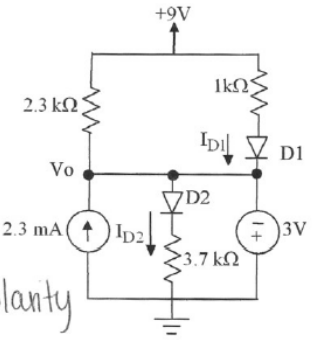
model



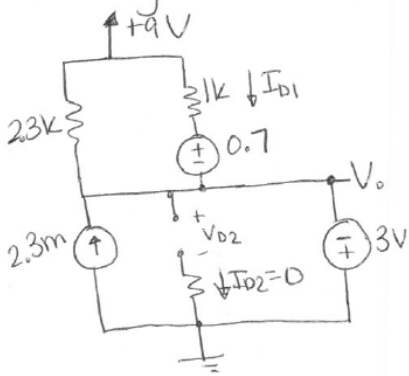
Example 19;

Assume all diodes are identical and have V_{DO}=0.7V, n=1, and V_T=25mV. Use the constant voltage drop method. Verify that your assumption for the diode operation(i.e. on or off) are correct. Find the following making sure you find the correct operation of the diodes.

a) State your assumptions (diode is on/off).
b) The current I_{D1}
c) The current I_{D2}
d) The voltage Vo
e) Your verification to prove your assumptions for the diodes are correct.



a) D1 on, D2 off (D2 will have -3V across it from observation- voltage polarity is wrong direction).



$+9 - I_{D1}(1k) - 0.7 + 3 = 0$

b) $I_{D1} = \frac{11.3}{1k} = \boxed{11.3mA} > 0$

So assumption for D1 ON correct. ✓

c) $\boxed{I_{D2} = 0}$

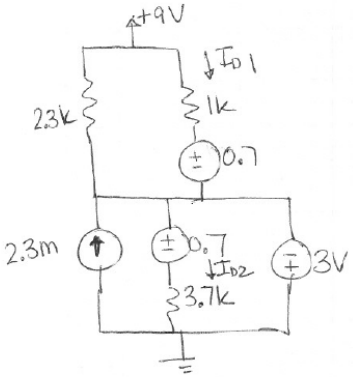
d) $\boxed{V_o = -3V}$

e) $-3V - V_{D2} = 0 \Rightarrow \boxed{V_{D2} = -3V} < 0$

∴ Assumption D2 on correct

$I_{D1} > 0$, D1 ON

D1 and D2 ON ⇒



$+9 - 0.7 + 3 - I_{D1}(1k) = 0$

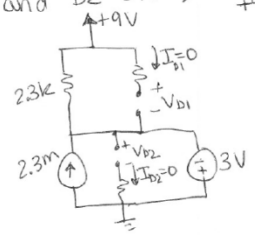
$I_{D1} = \frac{11.3}{1k} = 11.3mA$

$-3V - 0.7 - I_{D2}(3.7k) = 0$

$I_{D2} = \frac{-3.7}{3.7k} = -1mA < 0$ ✗

∴ Wrong Assumption

D1 and D2 off ⇒



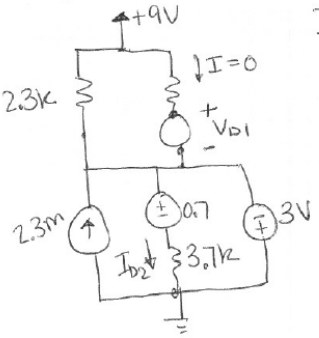
$+9 - V_{D1} + 3V = 0$

$V_{D1} = 12V$ (NOT NEGATIVE)
→ wrong assumption

$-3V - V_{D2} = 0$

$V_{D2} = -3V < 0$ (correct)

D2 ON, D1 off ⇒



$-3 - 0.7 - I_{D2}(3.7k) = 0$

$I_{D2} = \frac{-3.7}{3.7k} = -1mA < 0$ ✗ WRONG Assumption

$+9V - V_{D1} + 3V = 0$

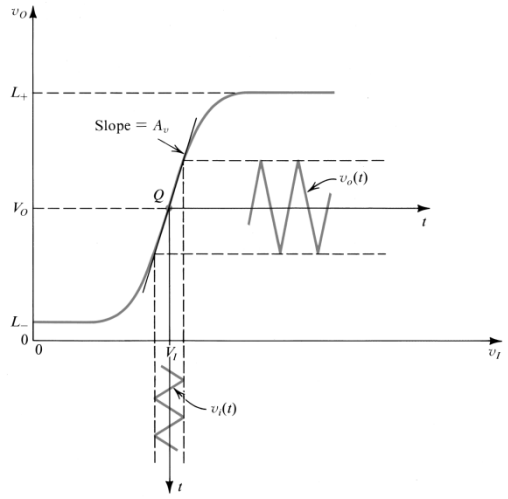
$V_{D1} = +12V$ which is NOT negative ⇒ WRONG ASSUMPTION

Small-Signal Analysis of Diodes

- So far we have looked at ***dc models*** for diodes
- For some applications it is necessary to also use a ***"small-signal" ac*** model
- If we use a small-signal model that linearizes the components, we can apply regular linear circuit analysis!
- We can then separate ac and dc analysis

The technique used to linearize a nonlinear characteristic is called ***biasing***.

Biasing:



- Biasing is achieved by operating the circuit with the nonlinear characteristic in a point near the middle
- From the graph, at dc voltage input V_I the dc voltage output is V_o.
- The point Q is known as the **quiescent point**, the **dc bias point**, or the **operating point**
- By limiting the amplitude of a ac time varying input signal, $v_I(t)$ the operating point is limited to a linear region of the curve.
- Note that this only works when the input signal is kept sufficiently small

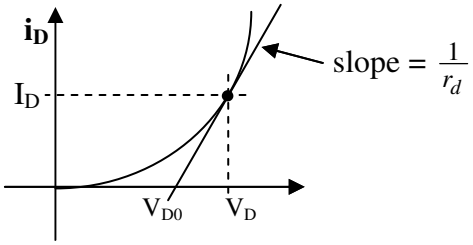
Derivation of the small-signal is done in the book (pg. 160).

The meaning of CAPITALS and lower case letters

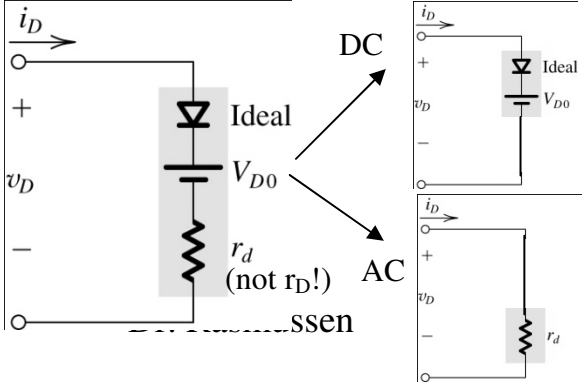
	examples		meaning
CAP_{CAP}	V_D	I_D	DC, Bias quantity
sm_{sm}	v_d	i_d	AC, signal
sm_{CAP}	v_D	i_D	DC and AC together

- Hard to analyze circuit with both signals together
  - Result of derivation: Can separate analysis into DC then AC!
  - $r_d = nV_T/I_D$ = small-signal resistance {result of analysis}

NOTE: This r_d is different than r_D from dc model
This r_d comes into play as the slope of the line tangent to the operating point:



Equivalent circuit model for the diode for small changes around the operating point:



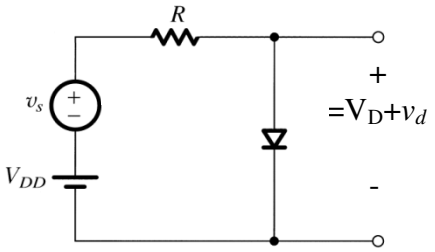
$$v_D = V_{D0} + i_D r_d$$
$$= V_{D0} + (I_D + i_d) r_d$$
$$= (V_{D0} + I_D r_d) + i_d r_d$$
$$= V_D + i_d r_d \ (DC + AC)$$

Procedure:

1). Do dc analysis first (what we have done so far) to find I_D
2). Use dc current value (I_D) to determine small-signal model parameter $r_d = nV_T/I_D$
3). Then do ac analysis to find i_d and v_d (AC values)

Example: Voltage Regulation – given an ac input voltage, povides ≈ constant dc voltage at output

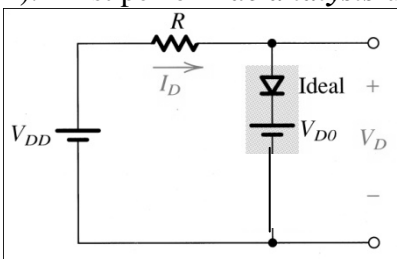
Circuit:



R=5k, v_s=sin(2π60t), V_{DD}=10V
Assume diode has 0.7V drop at 1mA and n=2

Find dc eak-to-peak signal voltage v_d across diode

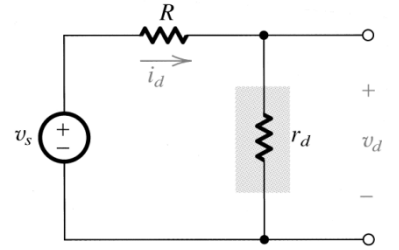
1). First perform ***dc analysis*** using constant voltage drop model- dc circuit model:



$-V_{DD}+I_D(R)+V_{D0}=0$
$I_D=(10-0.7)/5k=1.86mA$
$V_D=0.7V$

2). Calculate small-signal resistance(depends on dc current!): $r_d = \frac{nV_T}{I_D} = \frac{2(25mV)}{1.86m} = 26.8\Omega$

3). Perform ***ac analysis*** using small-signal model small-signal circuit model:



$v_s+i_d(R+r_d)=0 \Rightarrow i_d=v_s/(R+r_d)$

v_d (peak-to-peak)$=i_d(r_d)=\frac{v_s r_d}{(R+r_d)} = \frac{2(26.8)}{(5k+26.8)} = 10.7mVac$

Input: 10Vdc + $2V_{p\text{-}p}$ ac → i.e. ac is 10% of dc
Output 0.7Vdc + $10.7mV_{p\text{-}p}$ ac → ac is ≈ 0.8% of dc

PHYSICS OF DIODE

link can be used to understand more about the PN junction:
.buffalo.edu/applets/education/fab/pn/diodeframe.html

Physical properties of a diode => A diode is made up of what is called a pn-junction.

What is one main characteristic of a metal?Metals: tend to be good conductors because they have "free electrons" that can move easily between atoms; *flow of electrons → current flow*

Insulators: electrons in covalent bonds, so they can't move around; no flow of electrons → no current flow

A pn-junction has two different pieces of silicon(between a metal and insulator)that when put together and applying a forward voltage of approximately > 0.7V, we will have a conducting device that has current flow through it fully in one direction and very minutely in the reverse direction

→ You can change the behavior of silicon by ***doping*** it

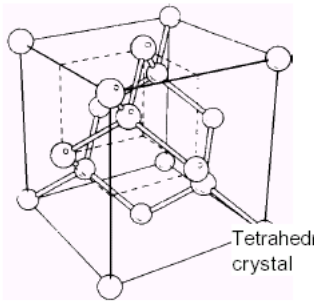
Doping: mix small amount of impurities into the silicon which changes its charge

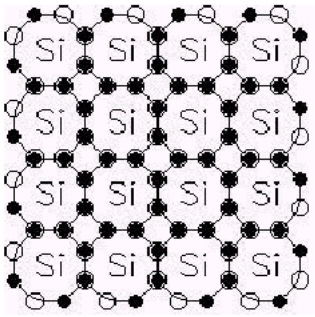
Silicon atoms

Silicon atoms each have 4 valence electrons (electrons in their outermost shell). That leaves 4 spaces in the outer shell of 8. This makes silicon a very reactive chemical, like carbon, which has the same valence configuration.

Silicon crystals

Each atom covalently bonds with four neighboring atoms to form a tetrahedral crystal, which we'll represent in 2D.

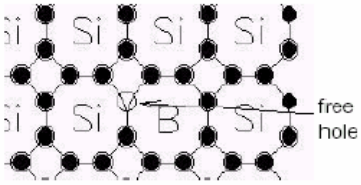




2-dimensional representation

Two types:

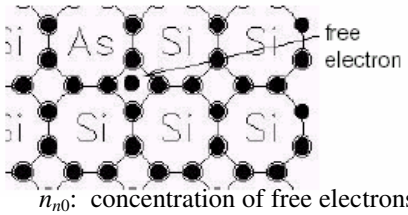
p-type



n_{p0}: concentration of free electrons in p-type
p_{p0}: concentration of holes in p-type
N_A: concentration of acceptor atoms

- p-type silicon ~ **Positive** charge
  - {holes are **majority**}
- $P_{po} \cong N_A \rightarrow n_{po} \cong \frac{n_i^2}{N_A}$
- n_{p0} is a function of temperature, p_{p0} independent of temperature

n-type



n_{n0}: concentration of free electrons in n-type
p_{n0}: concentration of holes in n-type
N_D: concentration of donor atoms

- n-type silicon ~ **Negative** charge
  - {e^- are **majority**}
- $n_{n0} = N_D$ $\qquad p_{n0} \cong \frac{n_i^2}{N_D}$
- p_{n0} is a function of temperature, n_{n0} independent of temperature

- A ***diffusion current*** I_D results in the forwar
- ***Minority carriers*** drift: Thermally generated holes in n material (electrons in p material) diffuse to edge of depletion region → electric field causes them to be swept across to the p side (n side)

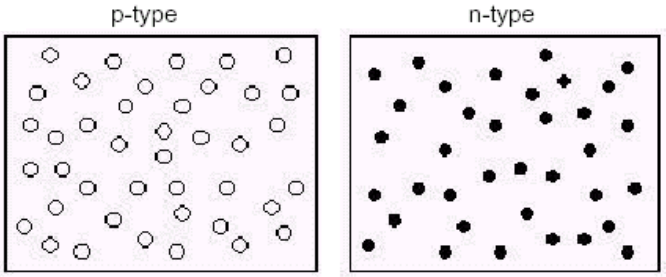
  → ***Drift current*** I_S is due to ***minority carriers*** diffusion (Temperature dependent since minority carriers are thermally generated)

  If no external current/voltage is applied, the above two currents will be equal:
  $I_D = I_S$ (Note: Can say diode current is $i_D = I_D - I_S = 0$)
  The built-in voltage, V_O, keeps this equilibrium.

  There is a **"built-in" voltage** (V_O) across the depletion region – acts as a barrier that diffusing holes or electrons have to overcome → larger it is → harder to overcome → fewer carriers diffuse → smaller I_D

Summary: electrons and holes have high mobility and result in current flow with applied current or voltage

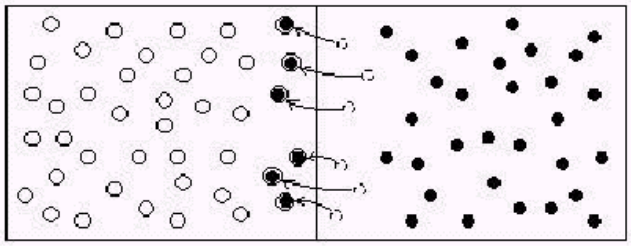
It turns out that the free carriers are the most important things in the semiconductor crystals, so we can simplify the drawings to show only these free carriers.



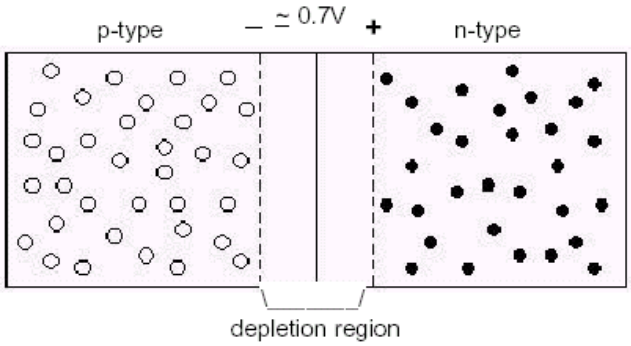
circles represent free holes dots represent free electrons

PN Junction

When a p-type semiconductor is created next to an n-type, some of the free electrons from the n side will cross over and fill some of the free holes on the p side. This makes the p side negatively charged and leaves the n side positively charged. When the voltage across the junction reaches about 0.7 V the electrons find it too difficult to move against the charge and the process stops.



A region near the junction is now depleted of carriers and (surprise) is called the depletion region.

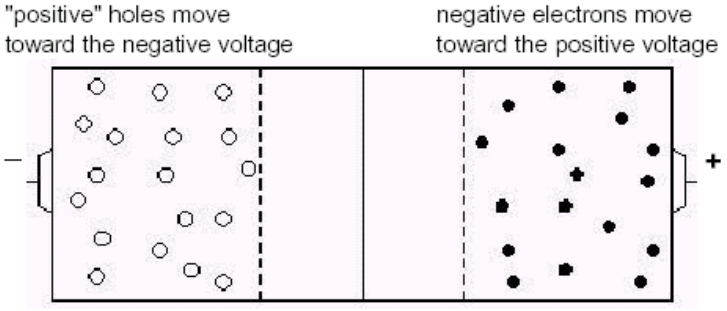


Reverse bias

This pn junction is now a diode. If you place an external voltage across the diode in the reverse bias direction, the depletion region gets bigger and no current flows.

This reverse bias region can be can be used as a heat or light sensor since the only current flow should be due to a few carriers produced by these effects.

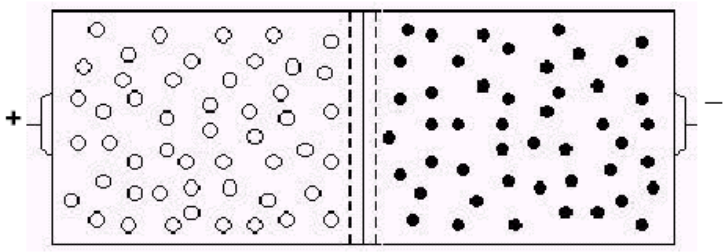
The reverse biased diode can also be used as a voltage variable capacitor since it is essentially an insulator (the depletion region) sandwiched between two conducting regions.



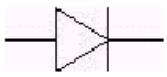
With reverse bias the depletion region gets bigger

Forward bias

If you place an external voltage across the diode in the forward bias direction, the depletion region shrinks until your external voltage reaches about 0.7V. After that the diode conducts freely..



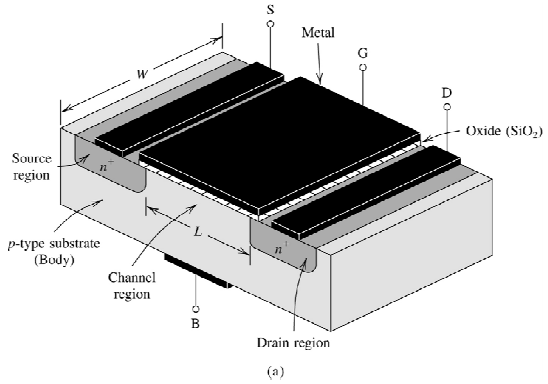
With forward bias the depletion region gets smaller and eventually (at about 0.7V) conducts freely.



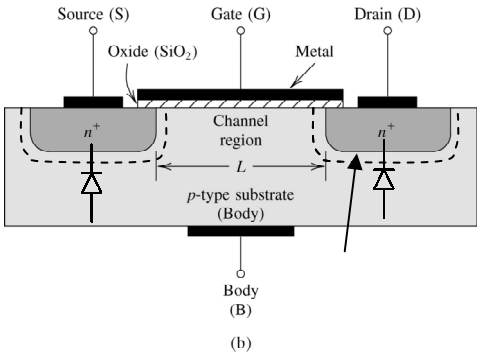
Diode

MOSFET

- This type of device dominates Integrated Circuit (IC) development due to their small size and low power consumption
- These devices have a totally different operating mechanism than BJT but once biased and linearized to allow linear small-signal operation, the same small-signal model for the BJT are applicable with little modifications
- Structure of MOSFET: A 4-terminal device



(a)



(b)

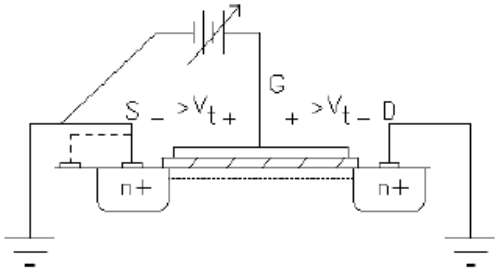
Threshold Voltage

Need some minimum voltage to induce a channel (n) in the p substrate

This minimum voltage is V_t, the threshold voltage

Usually: $1V < V_t < 3V$ but is very variable (like β)

Below this voltage the FET is off



Characteristics:

- 3 regions of operation:
  - cutoff
  - triode: $|V_{DS}| \le |V_{GS}| - |V_t|$, $V_{GS} > V_t$

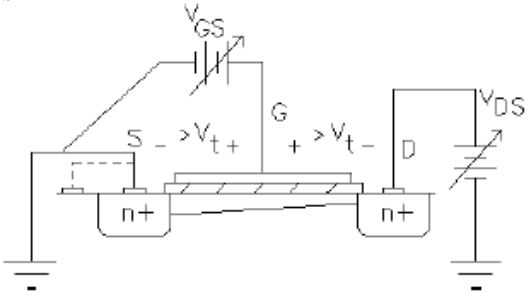
$$i_D = k_n'\left(\frac{W}{L}\right)\left[(V_{GS} - V_t)V_{DS} - \frac{1}{2}V_{DS}^2\right]$$

$$i_D \approx k_n'\left(\frac{W}{L}\right)(V_{GS} - V_t)V_{DS}$$

$$\frac{i_D}{V_{DS}} = \frac{1}{r_{DS}} \approx k_n'\left(\frac{W}{L}\right)(V_{GS} - V_t)$$

$$r_{DS} \approx \frac{1}{k_n'\left(\frac{W}{L}\right)(V_{GS} - V_t)}$$

if V_{DS} small ~200mV



  - saturation: $|V_{DS}| > |V_{GS}| - |V_t|$, $V_{GS} > V_t$

$$i_D = \frac{1}{2}k_n'\left(\frac{W}{L}\right)(V_{GS} - V_t)^2$$

k'_n = process transconductance parameter = 20 to 100 μA/V²

k'_p = 8 to 40 μA/V²

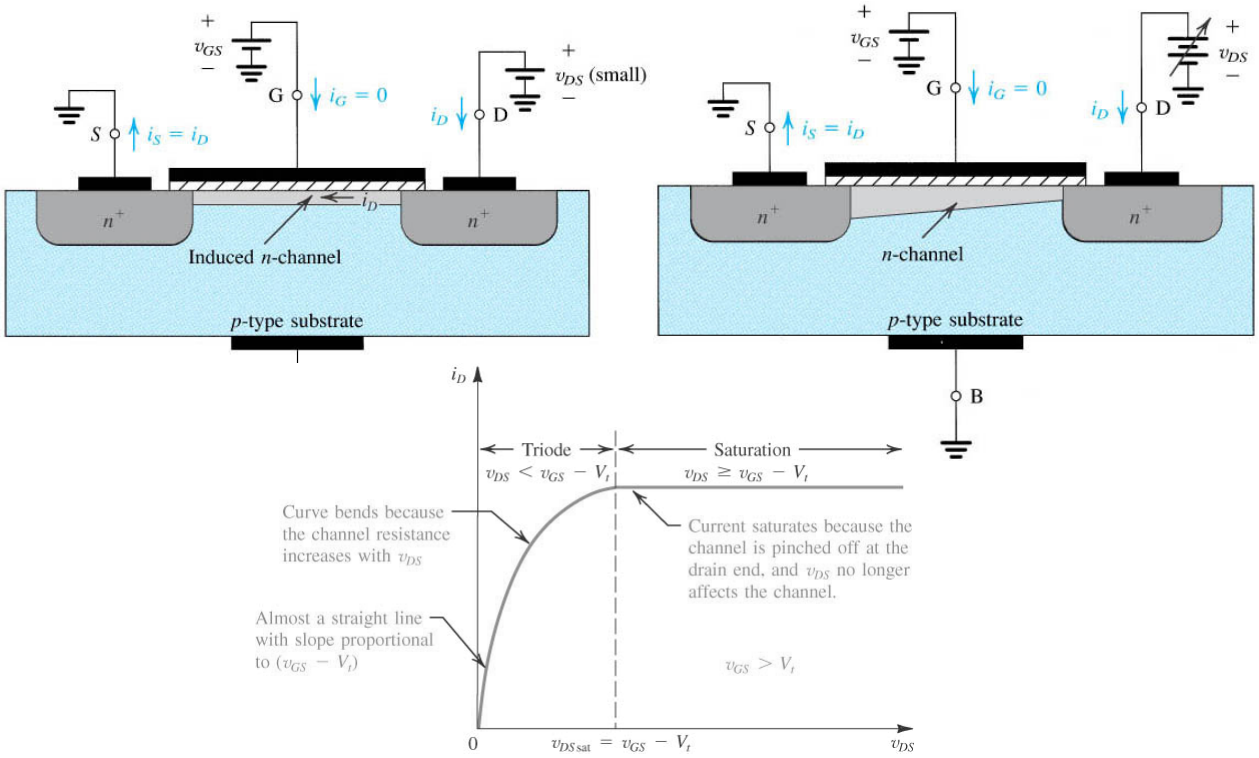
W = channel width

L = channel length

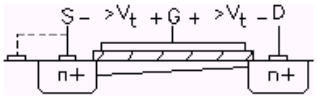
$K = k'_n \cdot \frac{W}{L}$ = gain factor (combined in books that are less interested in IC design)

$k'_n = \mu_n \cdot C_{ox}$ μ_n = electron mobility = $580 \cdot \frac{cm^2}{V \cdot s}$ $\mu_p := 230 \cdot \frac{cm^2}{V \cdot s} \simeq 40\% \mu_n$

$C_{ox} = \frac{\text{oxide capacitance}}{\text{unit area}}$ $= \varepsilon_{ox}/t_{ox}$ = permittivity / thickness = capacitance / (unit area)



Characteristic Curves



triode region

(a.k.a., ohmic or linear)

$v_{DS} < v_{GS} - V_t$

$v_{GD} > V_t$

saturation region

(a.k.a., constant current or active)

$v_{DS} = v_{GS} - V_t$

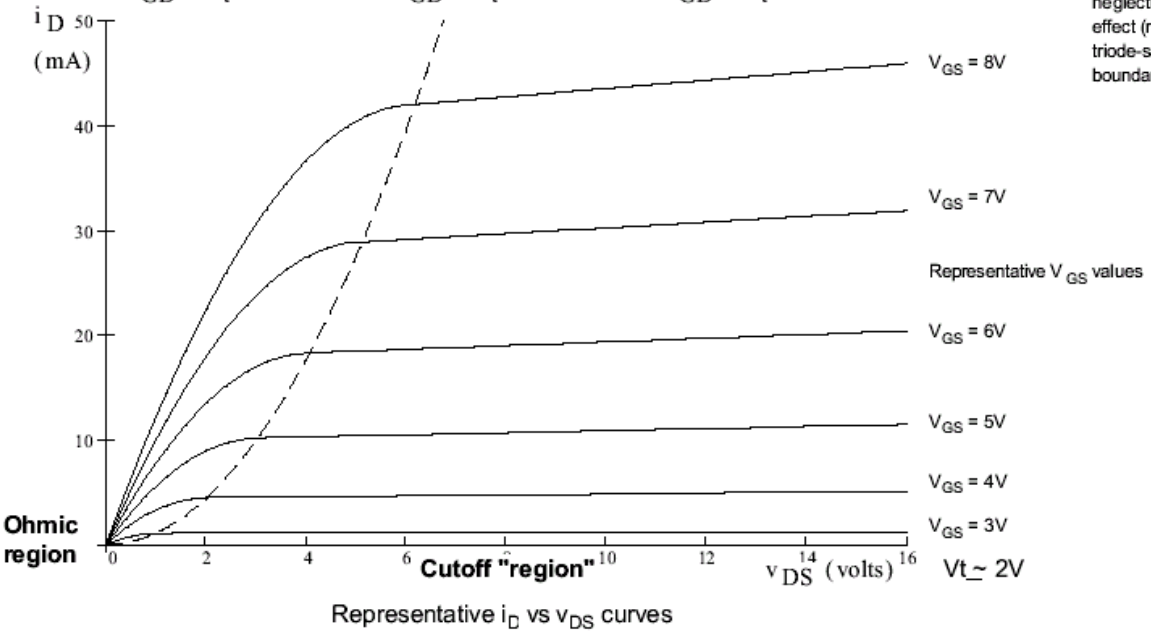
$v_{GD} = V_t$

$v_{DS} > v_{GS} - V_t$

$v_{GD} < V_t$

$$i_D \simeq \frac{1}{2} \cdot k'_n \cdot \frac{W}{L} \cdot (v_{GS} - V_t)^2$$

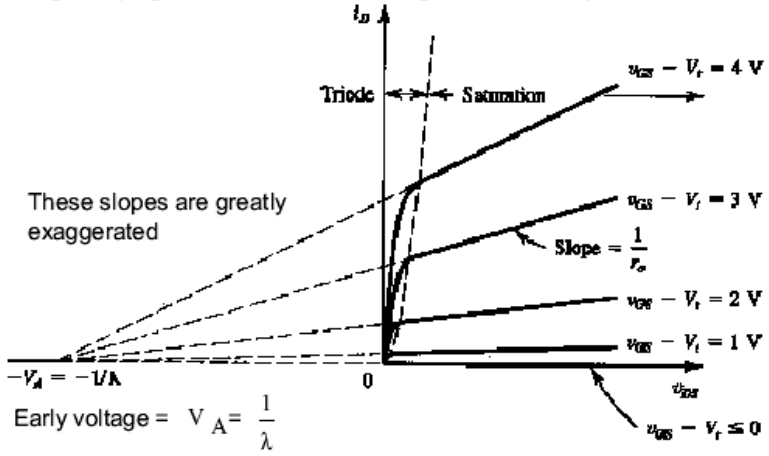
neglecting Early effect (r_o), or near triode-saturation boundary

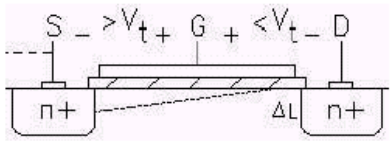


Representative i_D vs v_{DS} curves

Early effect, channel length modulation (r_o)

However, the pinched-off spot does get bigger as V_{DS} increases, leading to a shortening of the rest of the channel, and correspondingly more current. This leads to "channel length modulation" which is just like base width modulation in the BJT. It also leads to an Early voltage, sloping lines in the saturation region, and an output resistance.





including Early effect (r_o), due to channel length modulation $\lambda = \frac{1}{V_A}$

$$i_D = \frac{1}{2}\cdot k'_n \cdot \frac{W}{L}\cdot (v_{GS} - V_t)^2 \cdot (1 + \lambda \cdot v_{DS})$$

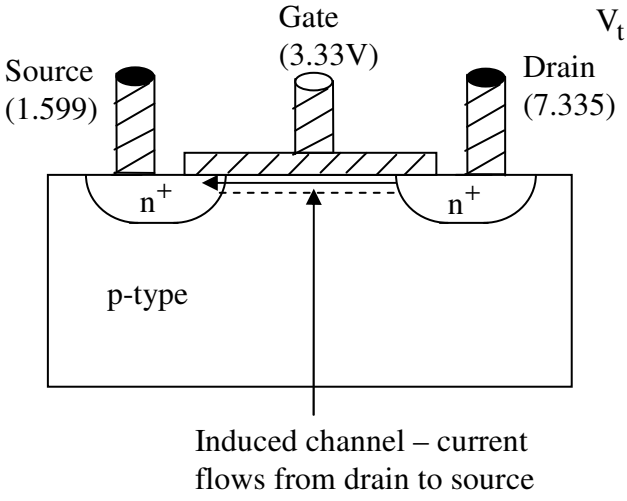
IMPORTANT EQUATION

$$r_o = \frac{\Delta v_{DS}}{\Delta i_D} = \frac{1}{\lambda\left[\frac{1}{2}\cdot k'_n \cdot \frac{W}{L}\cdot (v_{GS} - V_t)^2\right]} \simeq \frac{1}{\lambda \cdot I_D} = \frac{V_A}{I_D} = r_o$$

IMPORTANT EQUATION

Example

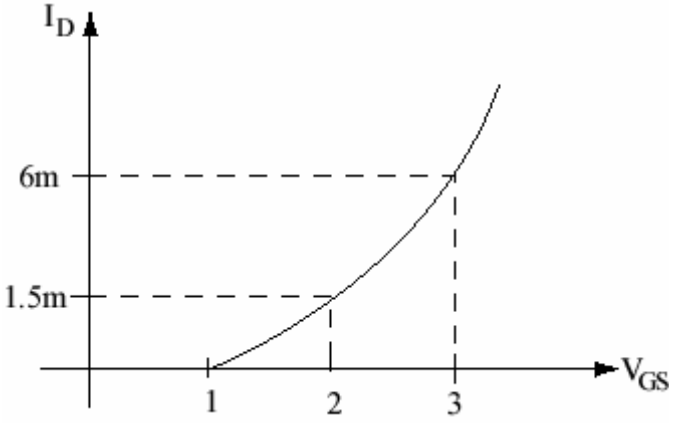
- **Cross-Section**



$V_t = 1V, \quad K'_n\left(\frac{W}{L}\right) = \frac{2mA}{V^2}, \quad I_D = \frac{1}{2}(3m)(V_{GS} - V_t)^2$

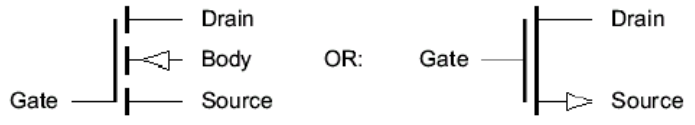
$V_S = 2: \quad I_D = 1.5m$

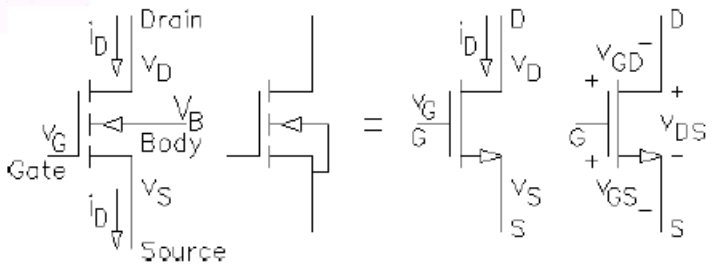
$V_{GS} = 3: \quad I_D = 6m$



Symbols:

n-channel enhancement:





p-Channel MOSFETs

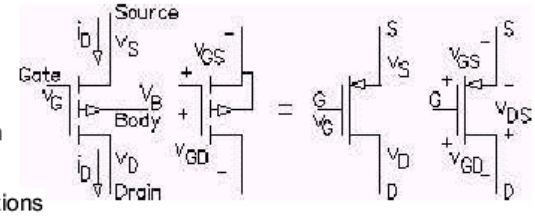
Use the same equations as for the n-channel, but:

Swap < for > and > for < in all the voltage tests.

Swap k'_p for k'_n in all equations

V_t will be negative

i_D comes out positive because the v_{DS} used in the equations is negative



Always shown in your book with the source on top, but that is not a requirement of the part symbol.

OR, just mirror the circuit and use an n-channel for purposes of analysis and then interpret the results.

The mobility of holes is only about 40% of the mobility of electrons.

So: $\mathbf{k'_p = \mu_p C_{ox} \sim 40\% k'_n}$

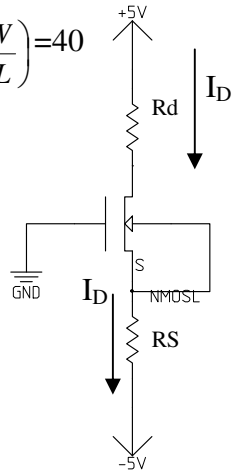
p-channel parts have to be $2^1/_2$ times as wide as an equal n-channel part. That means more $

Procedure for DC analysis of MOSFET:

1. **Assume Saturation mode**
2. **Put I_G=0 and I_D=I_S**
3. **Use** $I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS} - V_t)^2$
4. **Calculate voltages and currents**
5. **Check Saturation conditions =>** $|V_{DS}| > |V_{GS}| - |V_t|$, $V_{GS} > V_t$

Example 19: Let I_D=0.4mA, V_D=+1V

Given: V_t=2V, $\mu_n C_{ox} = k_n'$ =20μA/V2, L=10μm and W=400μm $\left(\frac{W}{L}\right)$=40



Assume **SATURATION**: $I_D \propto V_{GS}$ ($\lambda = 0$)

$$I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS} - V_t)^2$$

$$0.4x10^{-3} = \left(\frac{1}{2}\right)20x10^{-6}(40)(V_{GS} - 2)^2$$

$$0.4x10^{-3} = 400x10^{-6}\left({V_{GS}}^2 - 4V_{GS} + 4\right)$$

Quadratic Solution: ax^2+bx+c => $x = \frac{-b \pm \sqrt{b^2 - 4ac}}{2a}$ (2 solutions)

Therefore, $V_{GS} = \frac{4 \pm \sqrt{16 - 4(1)(3)}}{2(1)} = \frac{4 \pm 2}{2} = 1$ or 3V

Since V_t=2V then V_{GS}=1V does not have the transistor on so $V_{GS}=V_G - V_S$ =3V and so V_S=-3V

$$R_S = \frac{V_S - V_{SS}}{I_D} = \frac{-3-(-5)}{0.4} = 5k\Omega$$

$$R_D = \frac{V_{DD} - V_D}{I_D} = \frac{5-1}{0.4} = 10k\Omega$$

Example 20:

Solve the circuits below to find V_G, V_D, and V_S. Find the currents in all branches. Assume $\lambda=0$ and $|V_t|=1$, $k_n'(W/L)=100\mu A/V^2$.

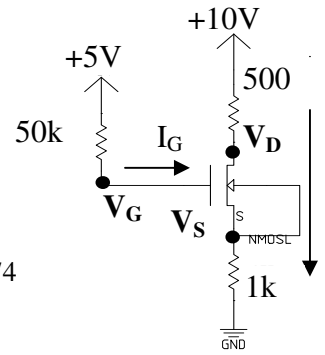
$I_G=0$ $V_G=+5V$ $V_S=I_D(1k)$ $V_D=10-I_D(500)$

$$I_D=\frac{1}{2}k_n'\left(\frac{W}{L}\right)(V_{GS}-V_t)^2(1+\lambda V_{DS})$$

Assume Sat: $$I_D=\frac{1}{2}(100x10^{-6})(5-I_D(1k)-1)^2(1+0(V_{DS}))$$

$$0=8x10^{-4}-1.4I_D+50I_D^2$$

$$I_D=\frac{1.4\pm\sqrt{(-1.4)^2-4(50)(8x10^{-4})}}{2(50)}=0.584m,0.0274$$



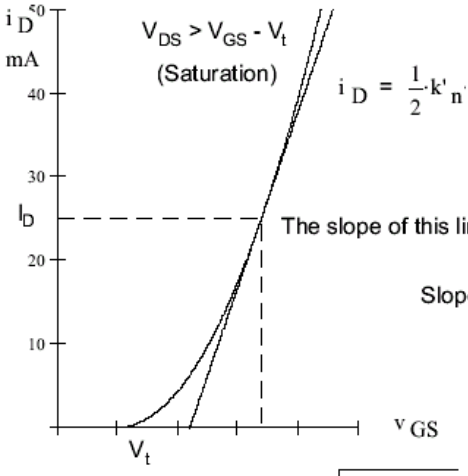
I_D=0.0274:

Vs=27.4V => Vgs<V_t (OFF!)

I_D=0.584m:

Vs=.584V **V_D=9.71V** **V_{DS}=9.12>3.416=(Vgs-V_t) (SAT.)**

Transconductance



$$\text{Slope} = \frac{d}{dv_{GS}}i_D = \frac{d}{dv_{GS}}\left[\frac{1}{2}\cdot k'_n\cdot\frac{W}{L}\cdot(v_{GS}-V_t)^2\right]$$

$$= \left[k'_n\cdot\frac{W}{L}\cdot(V_{GS}-V_t)\right]\cdot 1 = g_m = \frac{i_d}{v_{gs}}$$

small signal values

$$g_m = k'_n\cdot\frac{W}{L}\cdot(V_{GS}-V_t) = \sqrt{k'_n\cdot\frac{W}{L}\cdot 2\cdot I_D}$$

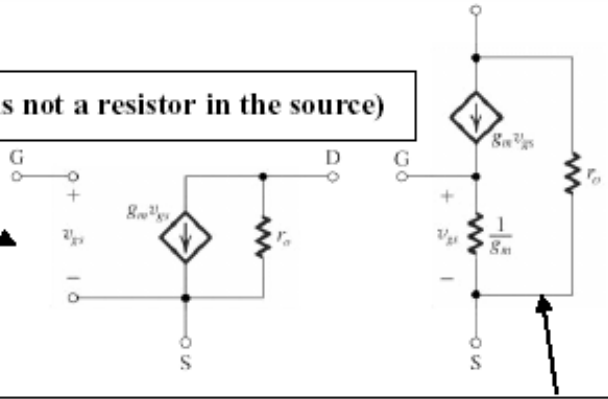
$$= \sqrt{\frac{4\cdot I_{DSS}\cdot I_D}{V_t^2}}$$ Depletion-type parts

Also called "transfer admittance, y_f"

Use $\frac{1}{g_m}$ in gain equations like r_e for BJT's

Small-signal model:

hybrid-π (use when there is not a resistor in the source)



$$r_o = \frac{V_A}{I_C} \approx \frac{1}{\lambda I_C}$$

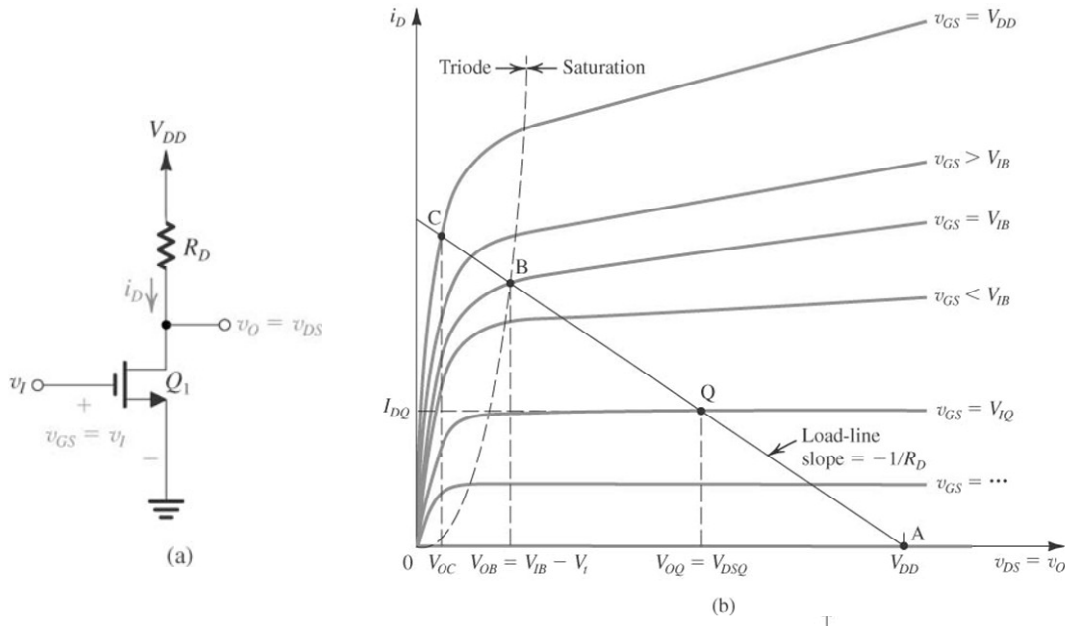
ignore if large

model-T (use when there is a resistor in the source - makes analysis a little easier)

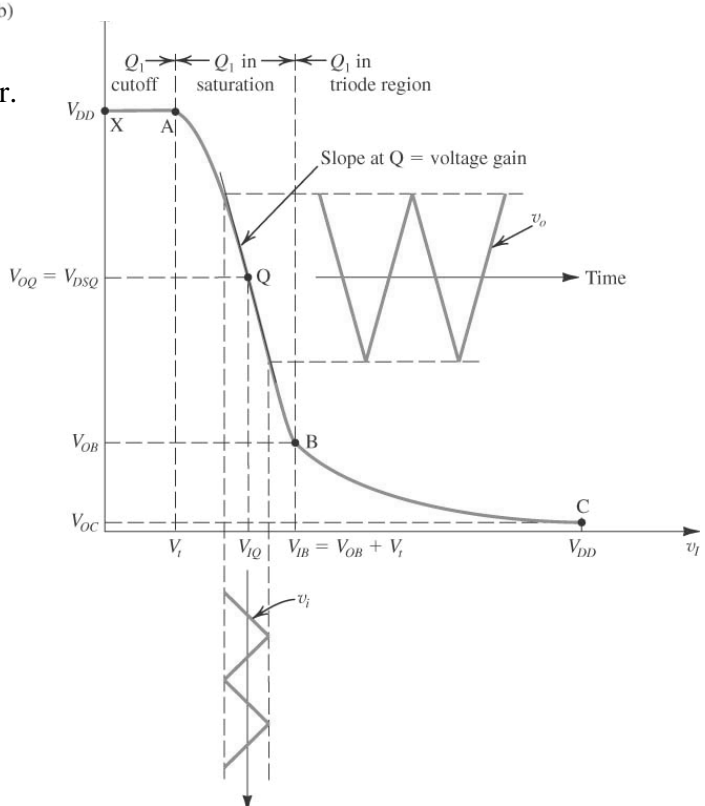
AS POINT

and AC values

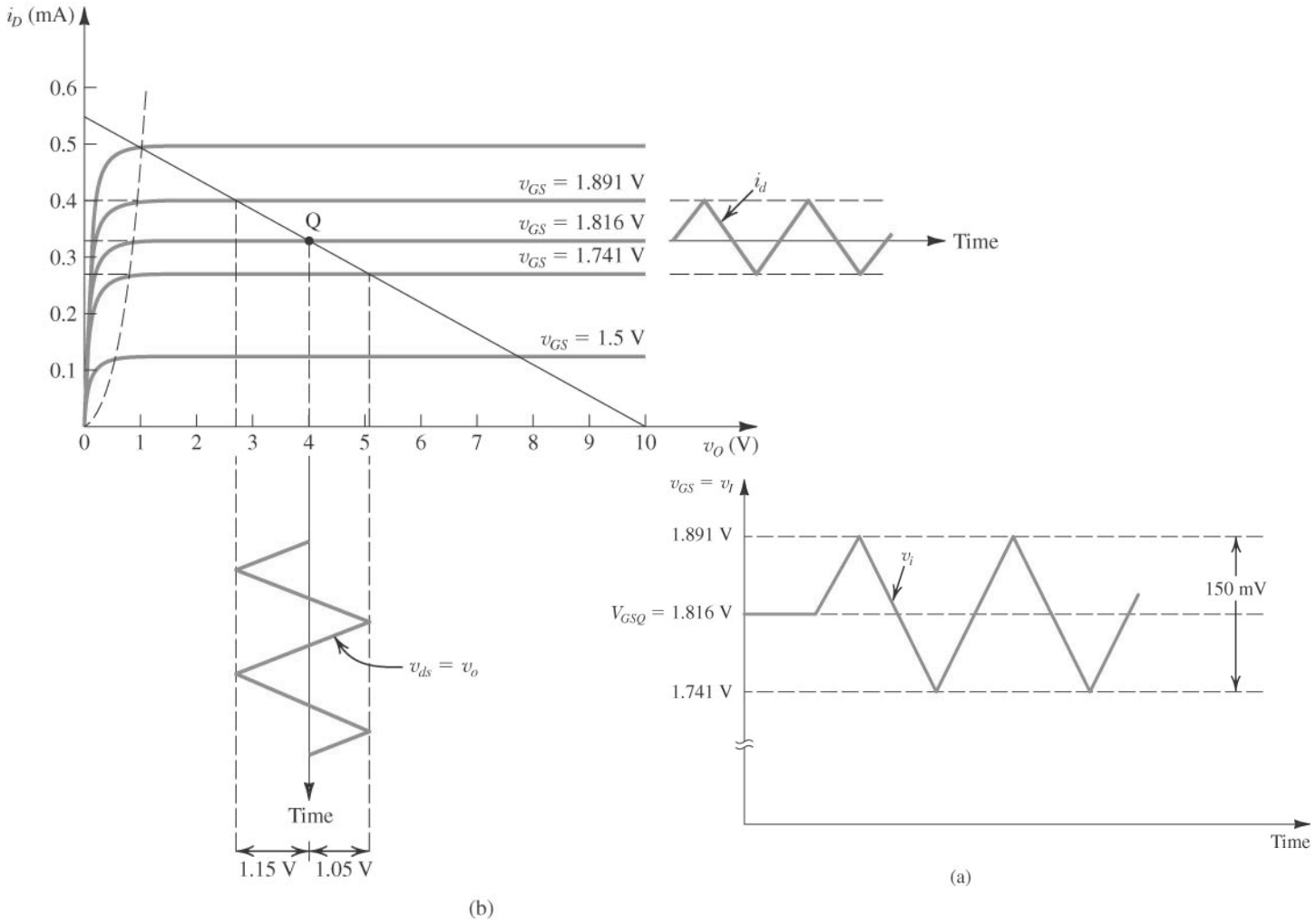
Example 20 (4.8 from book)



k'(W/L)=1mA/V^2, V_t=1V, R_D=18kohm, V_{DD}=10V
Find a good Q-point (bias point) to operate the amplifier.



Dr. Rasmussen

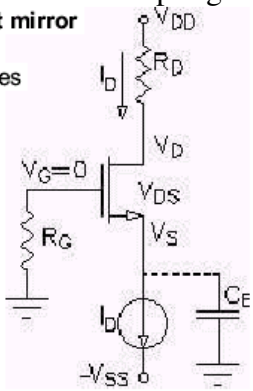

i_D (mA)
0.6
0.5
0.4
0.3
0.2
0.1
v_{GS} = 1.891 V
v_{GS} = 1.816 V
v_{GS} = 1.741 V
v_{GS} = 1.5 V
Q
0 1 2 3 4 5 6 7 8 9 10
v_O (V)
i_d
Time
$v_{ds} = v_o$
Time
1.15 V
1.05 V
(b)
$v_{GS} = v_I$
1.891 V
V_{GSQ} = 1.816 V
1.741 V
v_i
150 mV
Time
(a)

Biasing of MOSFET:

- Biasing is a key step in transistor design. It puts the transistor configuration at a good point in the saturation region that ensures that I_D, V_{OV}, and V_{DS} are predictable and stable and do not vary by a large amount when the transistor is replaced by another of the same type.
- R_G can be made very large: high R_{in}
- We need R_S to stabilize I_D from variations in V_t
- For IC(integrated circuit) design, we use active biasing or a constant current source.
  - Minimize number or R's and caps on an IC due to their large area requirement
    - Use active load for R
    - Use direct coupling for C

Current source bias from current mirror

Most common bias in ICs involves a current source

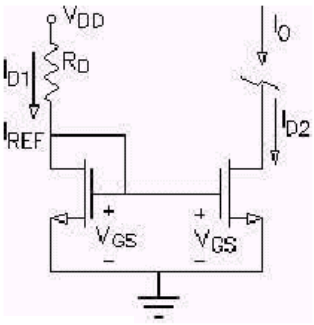


Note this particular arrangement doesn't have voltage gain unless the current source is bypassed, a rare thing in ICs since capacitors are so expensive to make in silicon.

Usually the current source is in a different position.

Current mirrors

$$I_{D1} = \frac{1}{2}\cdot k'_n \cdot \frac{W_1}{L_1}\cdot (V_{GS} - V_t)^2$$



$$I_{D2} = \frac{1}{2}\cdot k'_n \cdot \frac{W_2}{L_2}\cdot (V_{GS} - V_t)^2$$

The same VGS can be used to turn on many current sources, each with its own W/L ratio.

Usually k'_n and V_t are the same for both MOSFETs because they are in the same IC and were made by same processing, but you can still adjust the I_O current to any value you want by adjusting the W/L ratios.

$$\frac{I_O}{I_{REF}} = \frac{W_2}{L_2}\cdot\frac{L_1}{W_1}$$

Example 21

I_{REF}=100μA, Q_1&Q_2 same: (W/L)=(100μm/10μm), V_t=1V, k_n'=20μA/V^2, V_A=10L

I_o=100 μA

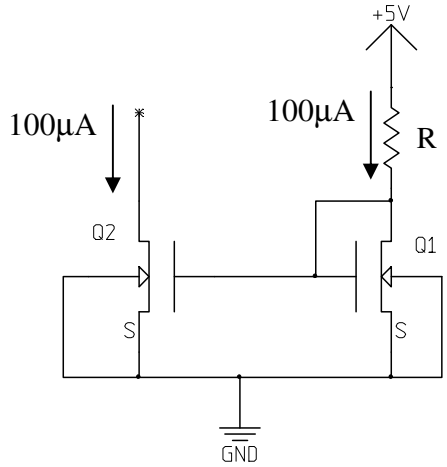
$$I_{D1} = I_{REF} = 100\mu = \frac{1}{2}20\mu(10)(V_{GS}-1)^2$$

$$100\mu = 100\mu(V_{GS}-1)^2 \Rightarrow 1 = V_{GS}{}^2 - 2V_{GS} + 1$$

$$V_{GS} = 2 \Rightarrow V_{o\min} = V_{GS} - V_t = 2 - 1 = 1V$$

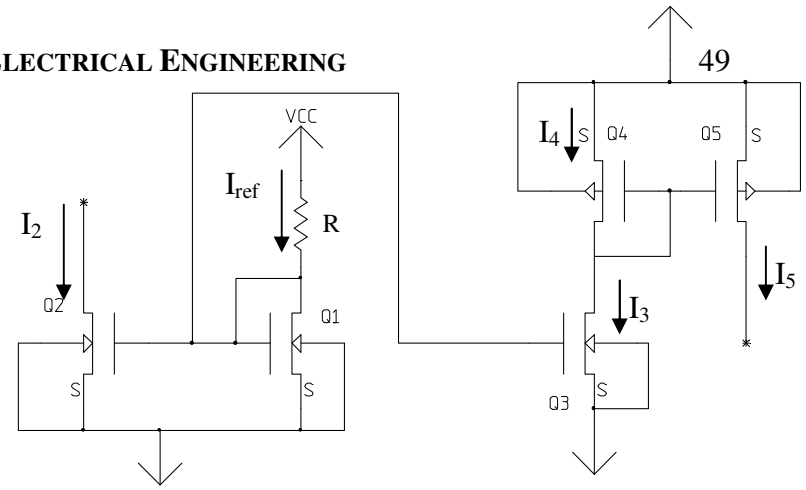
$$V_R = 5 - 2 = 3 \Rightarrow R = \frac{3}{100\mu} = 30k\Omega$$

$$V_A = 10L = 10(10) = 100V \Rightarrow r_o = \frac{V_A}{I_o} = \frac{100}{100\mu} = 1M\Omega$$



Example 22

Vdd=Vss=5V, V_{tn}=1V. V_{tp}=-1V, L=10μm, k_n'=20μA/V^2, k_p'=8μA/V^2, and λ=0. For I_{ref}=10μA, find all widths so that I_2=50μA, I_3=2.5μA, and I_5=50μA. Also let V_{D2} go down to within 0.5V of Vss and V_{D5} go up to within 0.5V of Vdd.



Want all transistors to operate in **SAT**
From above:

$$\frac{I_2}{I_{REF}}=\frac{(W/L)_2}{(W/L)_1} \qquad \frac{I_3}{I_{REF}}=\frac{(W/L)_3}{(W/L)_1}$$

$$\frac{I_5}{I_3}=\frac{(W/L)_5}{(W/L)_3} \qquad I_3=I_4$$

The threshold between saturation and linear region is: $V_{DS}=(V_{GS}-V_t)$
For Q_2: $V_{DS2}=V_{D2}-V_{S2}=0.5$
$V_{GS2}=V_{DS2}+V_{tn}=1.5$

$$I_2=50\mu A=\frac{1}{2}k_n'\left(\frac{W}{L}\right)_2\left(V_{GS1}-V_{tn}\right)^2=\frac{1}{2}20\mu\left(\frac{W}{L}\right)_2(1.5-1)^2$$

W_2=200μA

For Q_5: $V_{DS5}=V_{D5}-V_{S5}=-0.5$
$V_{GS5}=V_{DS5}+V_{tp}=-1.5$

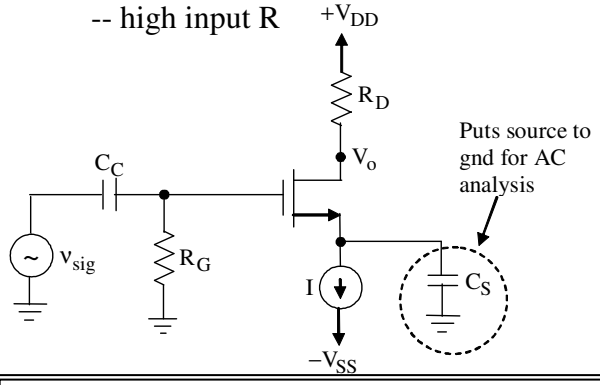
$$I_5=50\mu A=\frac{1}{2}k_p'\left(\frac{W}{L}\right)_5\left(V_{GS5}-V_{tp}\right)^2=\frac{1}{2}8\mu\left(\frac{W}{L}\right)_5(-1.5+1)^2$$

W_5=500μA

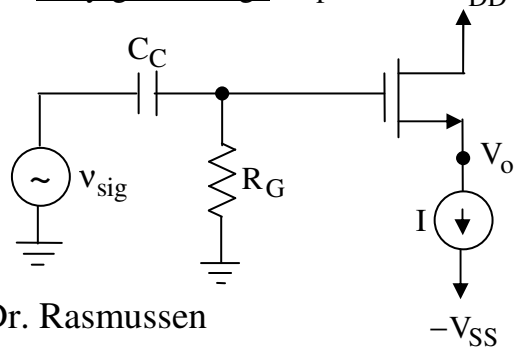
$\frac{I_2}{I_{REF}}=\frac{(W/L)_2}{(W/L)_1}$ and $\frac{I_5}{I_3}=\frac{(W/L)_5}{(W/L)_3}\Rightarrow$ **W_1=40μA** and **W_3=10μA**

MOSFET Configurations

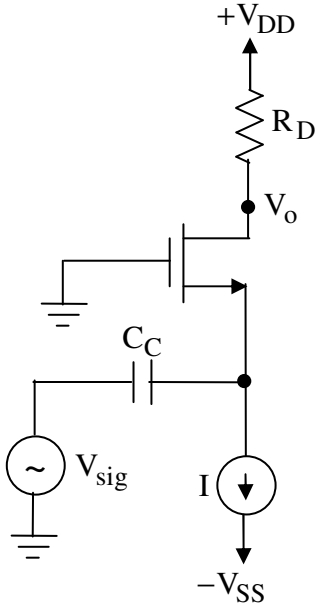
- **Common Source (CS)**
  -- best for high gain (most common)
  -- high input R



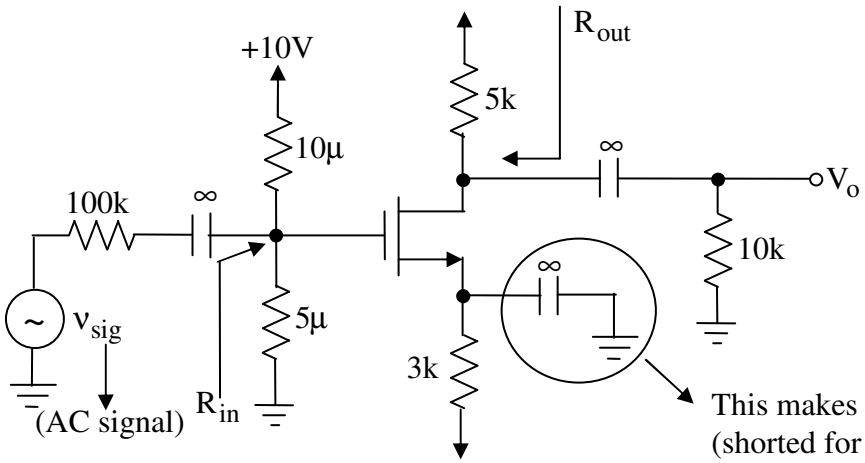
- **Common-Drain (CD)**
  -- used for <u>unity-gain voltage</u> amplifier



- **Common Gate (CG)**
  -- low input R (bad for voltage gain, good to not attenuate current signal)
  -- used for <u>unity-gain current</u> amplifier



Example 22:



CS Amplifier

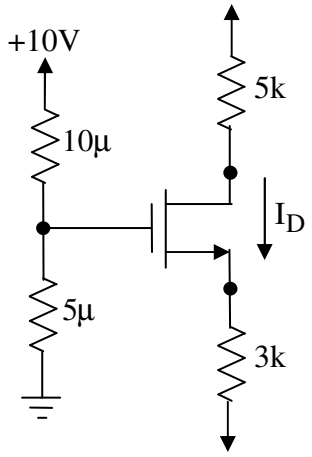
$V_t = 1$

$\lambda = 0$

$K_n'\left(\frac{W}{L}\right) = \frac{2\text{mA}}{V^2}$

Capacitors frequency dependence => $\frac{1}{Cj\omega}$

DC Analysis $\Rightarrow$ Open Caps and Find I_D {ω=0 for DC signal so $\frac{1}{0} = \infty$. It looks like a short}



$$V_G = \frac{10(5\mu)}{15\mu} = 3.38\text{V}$$

$$I_D = \frac{1}{2}(2\text{m})(3.33 - I_D(3\text{k}) - 1)^2$$

$$I_D = (1\text{k}) = (2.33 - I_D(3\text{k}))^2 = 5.44 + I_D^2(3\text{k})^2 - 13980\, I_D$$

$$I_D = +\frac{14980 \pm \sqrt{(14980)^2 - 4(5.44)(3\text{k})^2}}{2(3\text{k})^2} = +\frac{14980 \pm 5378}{18\mu}$$

$I_D = 1.1\text{m}$, $\boxed{+533\mu}$

$I_2 = 1.1\text{m} \Rightarrow V_S = 3.3\text{V}$

$\therefore V_{SS} = 0.03\text{V} < V_t$ NO

$I_D = 533\mu \Rightarrow V_S = 1.599,\ V_S = 1.731 > V_t$

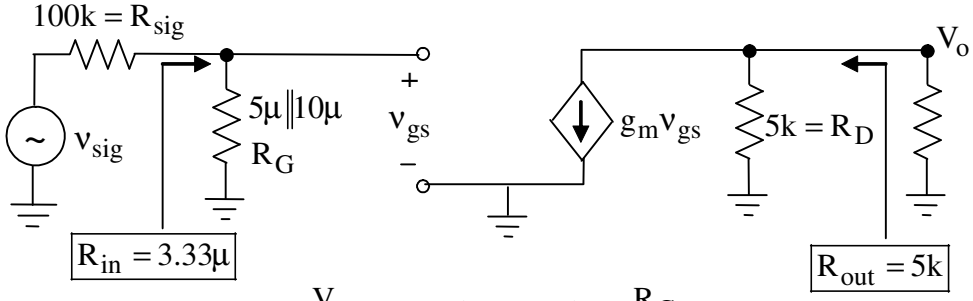
$\therefore$ ON

$V_D = 10 - 5\text{k}(533\mu) = 7.335$

$\therefore V_D > V_G - V_t$ (SATV)

AC Analysis $\Rightarrow$ Short Caps {C=large so $\frac{1}{\infty} \to 0$}

$$g_m = \sqrt{2K_n'\left(\frac{W}{L}\right)I_D} = 1.5\text{m} = \sqrt{2*2e-3*533e-6}$$



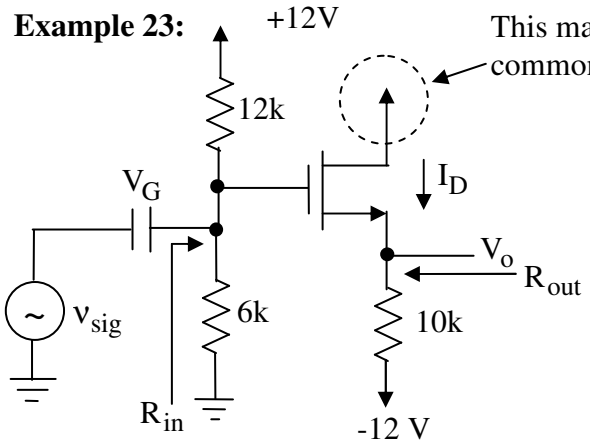
$$V_o = -g_m v_{gs}(5\text{k} \| 10\text{k})$$

$$v_{gs} = \frac{v_{sig}(3.33\mu}{3.33\mu + 100\text{k}}$$

$$\frac{v_o}{v_{sig}} \cong \boxed{-4.85\frac{V}{V}}$$

$$\frac{V_o}{V_{sig}} = -g_m(R_D \| R_L)\frac{R_G}{R_G + R_{sig}}$$

Example 23:



This makes this amplifier a common-drain (CD)

DC Analysis ⇒

$$V_t = 1V, \quad K_n'\left(\frac{W}{L}\right) = 6m, \quad \lambda = 0$$

$$V_o = I_D(10k) - 12$$

$$V_G = \frac{+12(6k)}{12k + bk} = 4V$$

$$I_D = \frac{1}{2}(6m)\left(4 - I_D(10k) + 12 - 1\right)^2$$

$I_D = \boxed{1.4m}$, $\quad 1.6m \Rightarrow I_D = 1.6m$

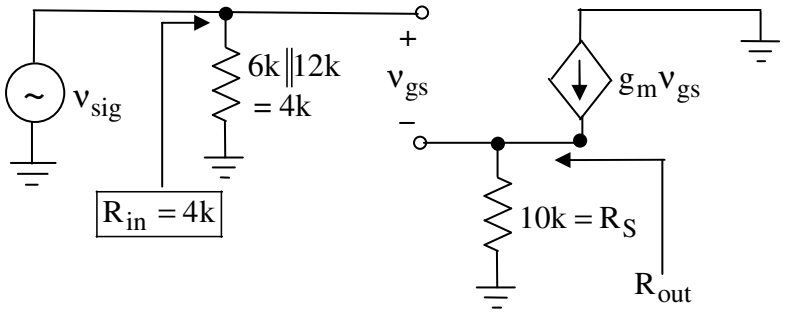
$V_S = 2V$

$V_{GS} = 2V > V_t$

$V_D = +12V \quad \left(\underline{\underline{SAT}} \Rightarrow V_{DS} \geq V_{GS} - V_t\right)$

$V_S = 4 \Rightarrow V_{GS} = 0V < V_t \quad \underline{\underline{NO}}$

AC Analysis ⇒

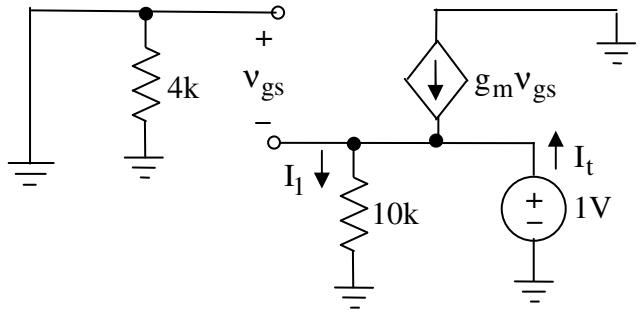


$$V_o = g_m v_{gs}(10k)$$

$$v_{gs} = v_{sig} - g_m v_{gs}(10k)$$

$$g_m = \sqrt{2(6m)1.4m} = 4.1m$$

$$\frac{V_o}{v_{sig}} = \frac{41}{1 + g_m(10k)} = \boxed{0.98\frac{V}{V}}$$

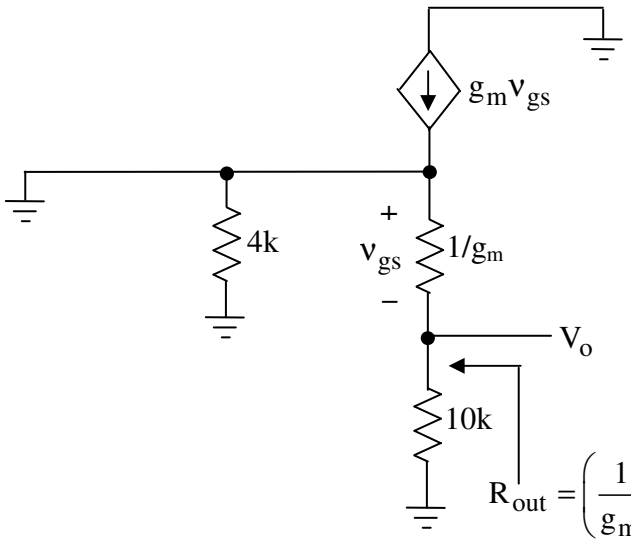


$$R_{out} = \frac{1V}{I_t} \qquad V_{gs} = -1V$$

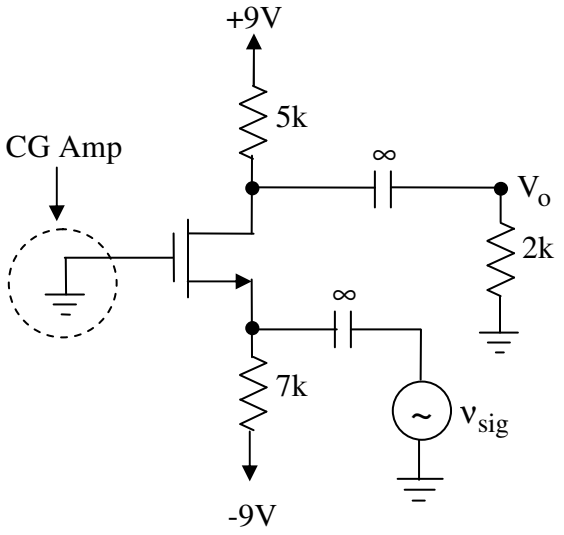
$$I_t + g_m v_{gs} - I_1 = 0 \Rightarrow I_t = g_m + \frac{1}{10k}$$

$$R_{out} = \frac{1V}{g_m + \frac{1}{10k}} = \frac{1}{g_m} \| 10k = \boxed{238\Omega}$$

Note: (Model T)

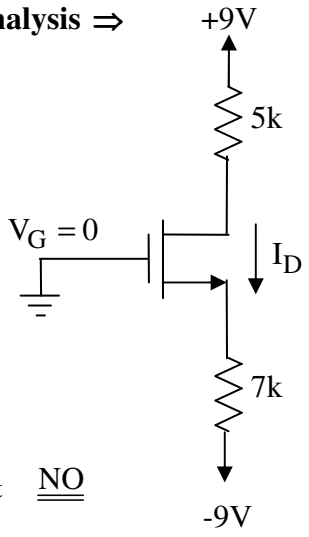


Example 24:



$$V_t = 1V, \quad K_n'\left(\frac{W}{L}\right) = \frac{2mA}{V^2}, \quad \lambda = 0$$

DC Analysis ⇒



$$I_D = \frac{1}{2}(2m)\left(0 - I_D(7k) + 9 - 1\right)^2$$

$$I_D = \boxed{1m}, \quad 1.3m \Rightarrow I_D = 1.3m, \quad V_s = .1, \quad V_S = -0.1 < V_t \quad \underline{\underline{NO}}$$

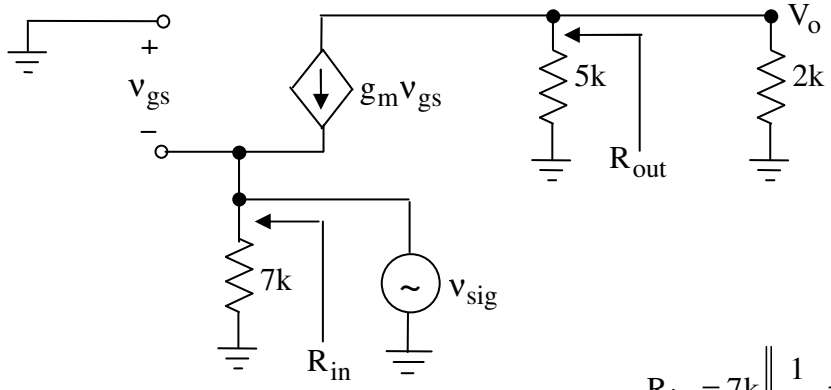
$$V_S = -2$$

$$V_{GS} = +2V > V_t \quad (ON)$$

$$V_D = 9 - 5 = 4V \quad (SAT)$$

AC Analysis:

$$g_m = \sqrt{2(2m)1m} = 2m, \quad V_o = -g_m \nu_{gs}(5k \| 2k), \quad \nu_{gs} = -V_{sig}$$

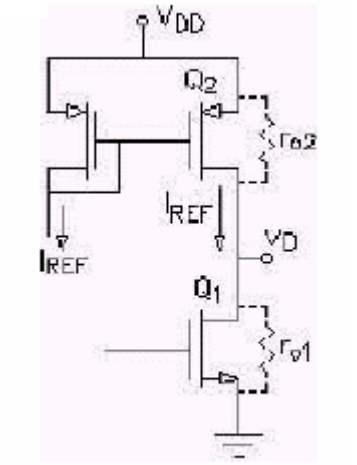


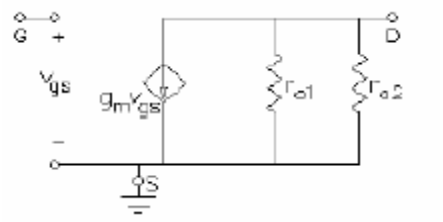
$$\boxed{\frac{V_o}{\nu_{sig}} = 2.9\frac{V}{V}}$$

$$R_{in} = 7k \left\| \frac{1}{g_m} \right. = \boxed{467\Omega}$$

$$R_{out} = \boxed{5k}$$

Common Source biased with current mirror:

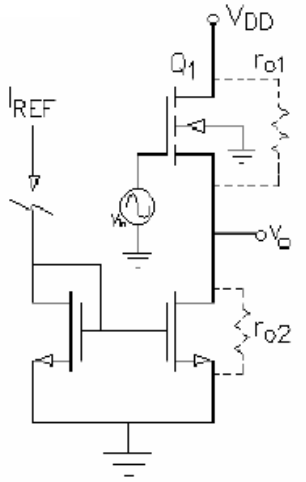


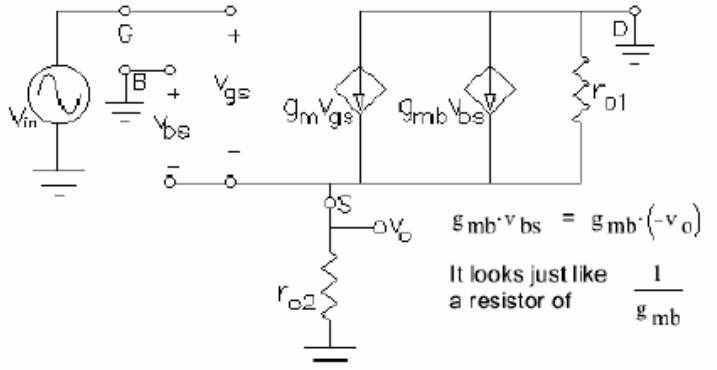


$r_{o1} \| r_{o2}$

0

Common drain (source follower) biased with current mirror:



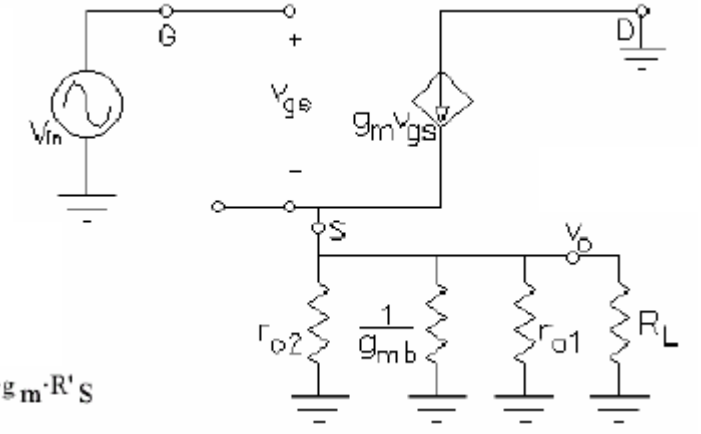


$g_{mb} \cdot v_{bs} = g_{mb} \cdot (-v_o)$

It looks just like a resistor of $\frac{1}{g_{mb}}$

$$R'_S = \frac{1}{\left(g_{mb} + \frac{1}{r_{o2}} + \frac{1}{r_{o1}} + \frac{1}{R_L}\right)}$$

$$v_o = v_{gs} \cdot g_m \cdot R'_S$$



$$= \left(v_{in} - v_o\right) \cdot g_m \cdot R'_S = v_{in} \cdot g_m \cdot R'_S - v_o \cdot g_m \cdot R'_S$$

$$\frac{v_o}{v_{in}} = \frac{g_m \cdot R'_S}{1 + g_m \cdot R'_S} = \frac{g_m}{\frac{1}{R'_S} + g_m} = \frac{g_m}{g_m + \left(g_{mb} + \frac{1}{r_{o2}} + \frac{1}{r_{o1}} + \frac{1}{R_L}\right)} = \frac{g_m}{g_m + \chi \cdot g_m + \frac{1}{r_{o2}} + \frac{1}{r_{o1}} + \frac{1}{R_L}}$$

$$R_o = \frac{1}{\left(g_m + g_{mb} + \frac{1}{r_{o2}} + \frac{1}{r_{o1}}\right)}$$

often neglected /____/

Example 28

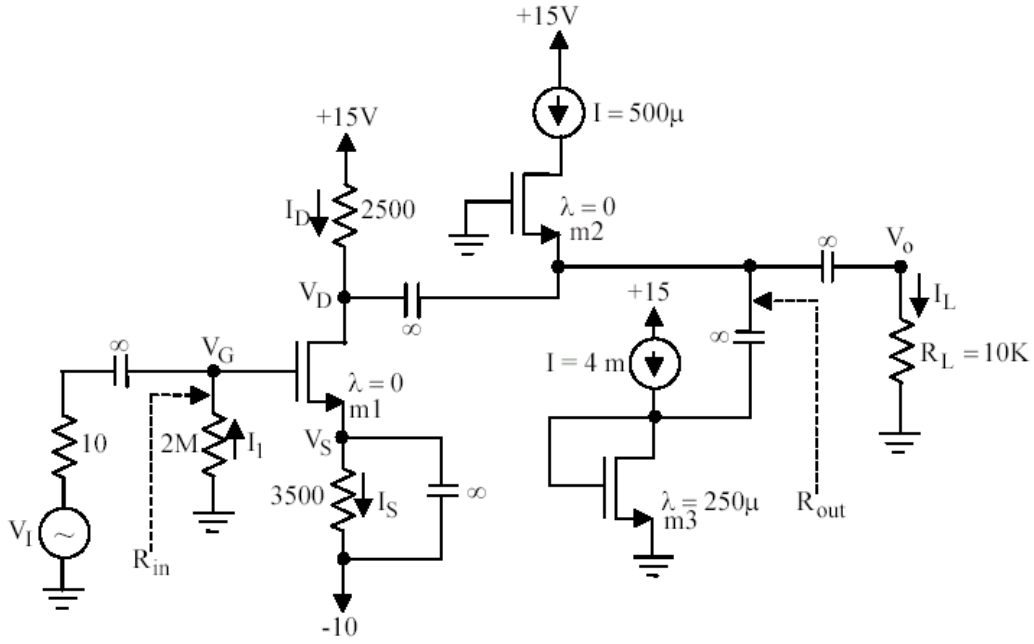
V_t=2V

k_n'(W/L)=4mA/V^2

Find I_1, I_D, I_S, I_L

Find V_G, V_S, V_o

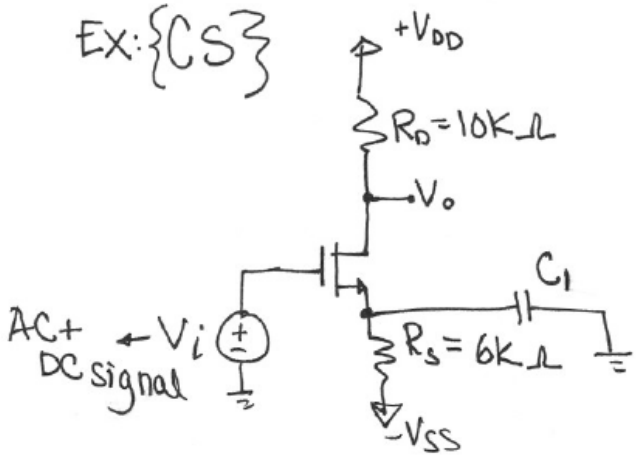
Find R_{in}, , $A_v=\frac{V_o}{V_I}$



Frequency Response:

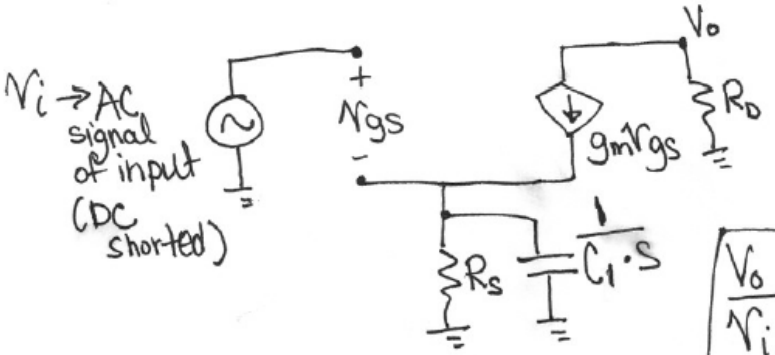
- The low frequency is typically determined by the coupling capacitors.
  - These are controlled by the designer

Ex: {CS}



- given $g_m = 1mA/V$
  $I_D = 1m$

- Leave capacitors in the AC model to determine overall transfer function ⇒



$$V_o = -g_m v_{gs} \cdot R_D$$

$$v_{gs} = v_i - g_m v_{gs}\left(R_s \| \frac{1}{C_1 s}\right)$$

$$v_{gs} = \frac{v_i}{1 + g_m\left(R_s \| \frac{1}{C_1 s}\right)}$$

$$\boxed{\frac{V_o}{v_i} = \frac{-g_m R_D (R_s C_1 s + 1)}{(1 + g_m R_s)\left[\left(\frac{R_s C_1 s}{1 + g_m R_s}\right) + 1\right]}}$$

$$\frac{V_o}{V_i} = \frac{-g_m R_D}{(1+g_m R_S)} \cdot \frac{(R_S C_1 s + 1)}{\left[\left(\frac{R_S C_1 s}{1+g_m R_S}\right)+1\right]}$$

magnitude plot ⇒ · One zero @ $(R_S C_1 s + 1) = 0$

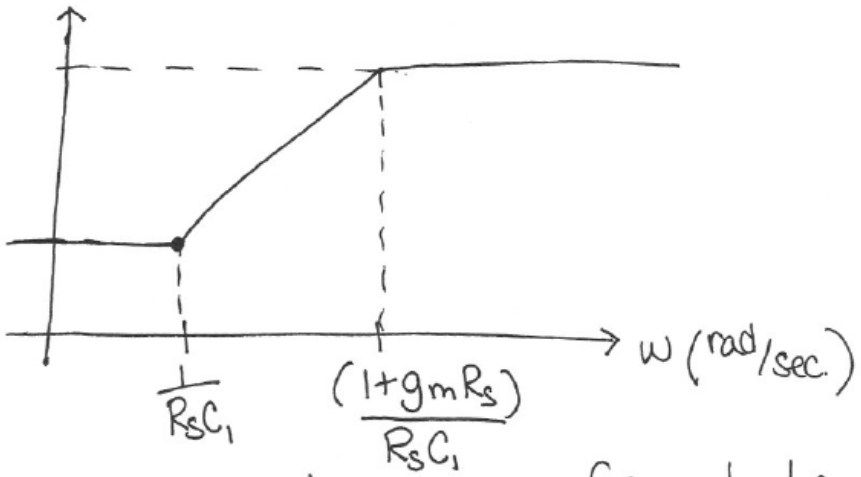
$$\therefore s = \frac{1}{R_S C_1}$$

· One pole at $\left(\frac{R_S C_1 s}{1+g_m R_S} + 1\right) = 0$

$$s = \frac{(1+g_m R_S)}{R_S C_1}$$

∴ The pole will be larger than the zero

· Recall that a zero contributes +20dB/dec and a pole -20dB/dec.

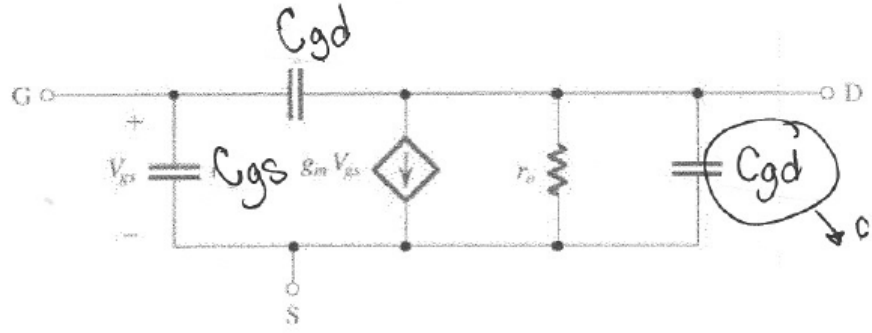


· Suppose you want the low freq. to be 10Hz

$$\therefore 10\,Hz = \frac{(1+g_m R_S)}{2\pi (R_S C_1)} \Rightarrow C_1 \cong 18.6\mu F$$

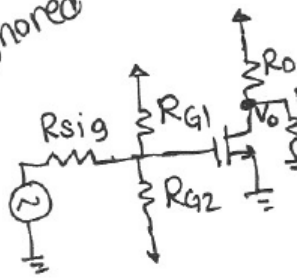
(when $g_m = 1m$, $R_S = 6k$)

High Frequency: · Controlled by parasitic capacitance

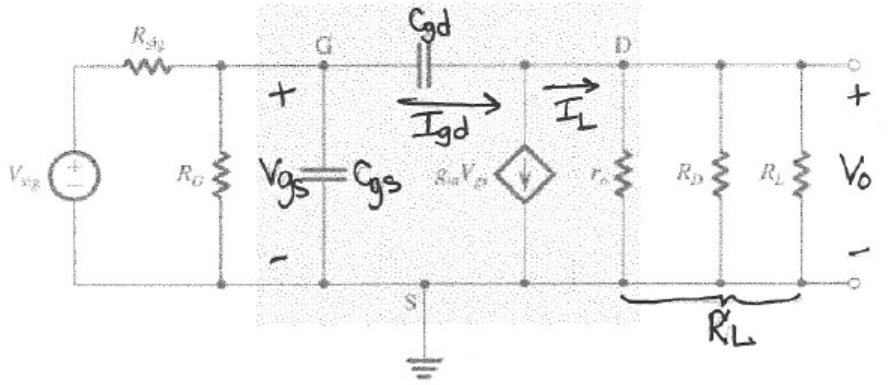


(b)

can be typically ignored



$R_G = R_{G1} \| R_{G2}$



(a)

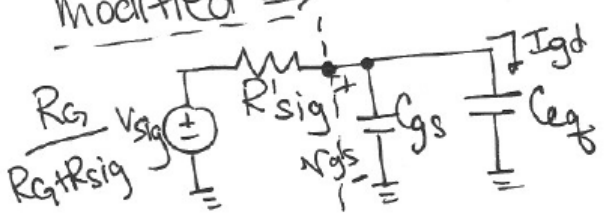
$I_L = g_m v_{gs} - I_{gd}$ (at frequencies $\sim f_H$ assume $I_{gd} \ll g_m v_{gs}$)

$\therefore V_o \approx -g_m R'_L v_{gs}$

$$I_{gd} = \frac{V_G - V_o}{\frac{1}{C_{gd} \cdot s}} = C_{gd} \cdot s \left(v_{gs} - (-g_m R'_L v_{gs})\right)$$

$$I_{gd} = C_{gd} \cdot s \left(1 + g_m R'_L\right) v_{gs}$$

· Since I_{gd} does not influence the output, it can be modified ⇒



Thevenin equivalent

where $R'_{sig} = R_{sig} \| R_G$

· From new circuit,

$$I_{gd} = \frac{V_{gs}}{\frac{1}{C_{eq}\cdot s}} = C_{eq}\cdot s\cdot V_{gs}$$

· Setting old I_{gd} = new I_{gd}

$$C_{eq}\cdot s\cdot V_{gs} = C_{gd}\cdot s\cdot(1+g_m R'_L)V_{gs}$$

$$\therefore C_{eq} = C_{gd}(1+g_m R'_L)$$

$$V_{gs} = \frac{V_{sig}(R_G)}{R_G + R'_{sig}}\cdot\frac{\left(\frac{1}{C_{gs}\cdot s} \parallel \frac{1}{C_{eq}\cdot s}\right)}{\left(\frac{1}{C_{gs}\cdot s} \parallel \frac{1}{C_{eq}\cdot s}\right) + R'_{sig}}$$

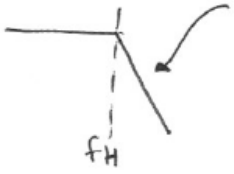
$$\frac{1}{C_{gs}\cdot s} \parallel \frac{1}{C_{eq}\cdot s} = \frac{1}{s(C_{eq}+C_{gs})}$$

$$\therefore V_{gs} = \frac{V_{sig}R_G}{(R_G+R'_{sig})}\cdot\frac{\frac{1}{s(C_{eq}+C_{gs})}}{\frac{1}{s(C_{eq}+C_{gs})} + R'_{sig}} = \frac{V_{sig}\cdot R_G}{(R_G+R'_{sig})\left(1+R'_{sig}(s(C_{eq}+C_{gs}))\right)}$$

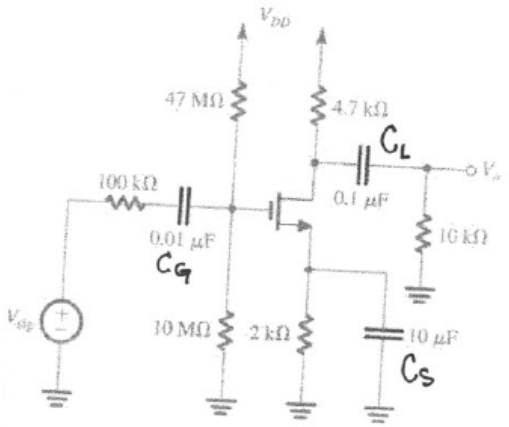
$$V_{gs} = \frac{V_{sig}\cdot R_G}{(R_G+R'_{sig})(1+sR'_{sig}(C_{eq}+C_{gs}))}$$

Recall → $V_o \cong -g_m R'_L V_{gs} \Rightarrow \frac{V_o}{V_{sig}} = \frac{-g_m R'_L R_G}{(R_G+R'_{sig})(1+sR'_{sig}(C_{eq}+C_{gs}))}$

· with only 1 pole ⇒ (recall -20dB/dec) $\therefore \omega_H = \frac{1}{R'_{sig}(C_{eq}+C_{gs})}$



Example:

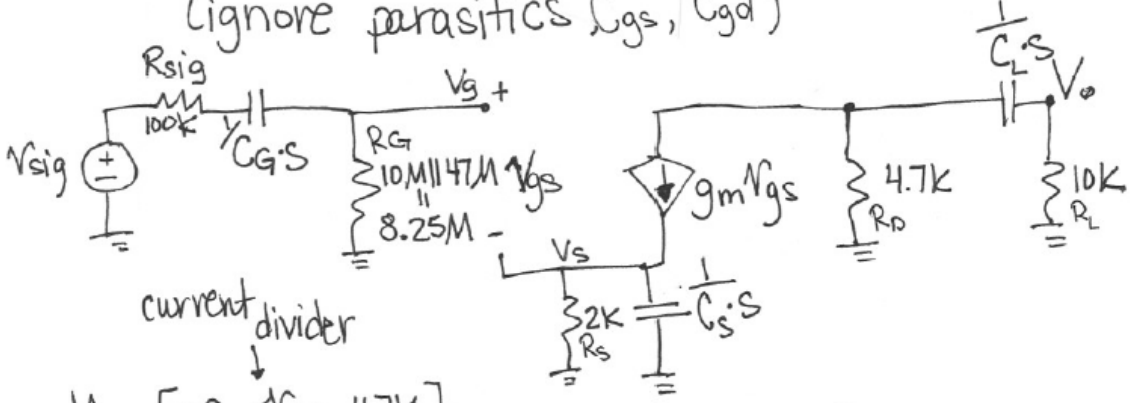


$g_m = 1mA/V$

$C_{gs} = 1pF$

$C_{gd} = 0.2pF$

- Let us analyze low Freq. 1st ⇒ C_G, C_s, and C_L contribute to low response (ignore parasitics C_{gs}, C_{gd})



current divider ↓

$$V_o = \left[\frac{-g_m V_{gs} \cdot 4.7K}{4.7K + \frac{1}{C_L S} + 10K}\right] \cdot 10K = \frac{-g_m 4.7K(10K) V_{gs} \cdot C_L S}{((14.7K)C_L S + 1)} =$$

$$V_{gs} = \frac{V_{sig}(8.25M)}{8.25M + 100K + \frac{1}{C_G \cdot S}} - g_m V_{gs}(2K \| \frac{1}{C_S \cdot S})$$

$$V_{gs} = \frac{V_{sig}(8.25M)C_G \cdot S}{(8.35M C_G \cdot S + 1)} \quad \frac{1}{1 + g_m(2K \| \frac{1}{C_S \cdot S})}$$

$$V_{gs} = \frac{V_{sig}\,(8.25M)\,C_G \cdot s\,(2K \cdot C_S \cdot s + 1)}{(8.35M \cdot C_G \cdot s + 1)(1 + g_m 2K)\left(\frac{2K \cdot C_S \cdot s}{1 + g_m 2K} + 1\right)}$$

$$\frac{V_o}{V_{sig}} = \frac{-4.7m\,(0.0825)(0.02s+1)\cdot s^2}{(1.47m \cdot s+1)(0.0835 \cdot s+1)(3)(6.67m \cdot s+1)}$$

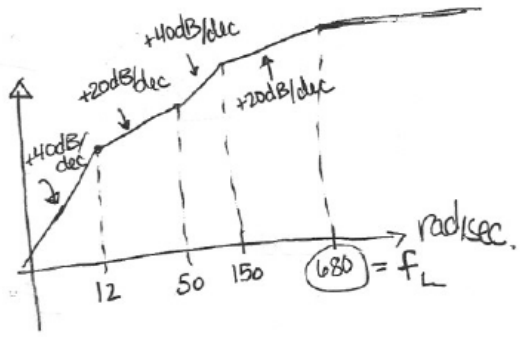
poles at $w \cong 680.3$ rad/sec $\rightarrow \frac{1}{(R_D+R_L)C_L}$

$w \cong 12$ rad/sec $\rightarrow \frac{1}{(R_G+R_{sig}) \cdot C_G}$

$w \cong 150$ rad/sec $\rightarrow \frac{1}{(\frac{1}{g_m} \| R_S) \cdot C_S}$

zero at $w \cong 50$ rad/sec

This circuit will start to work properly at $f_L = 108$ Hz



High frequency $\Rightarrow$ (Recall derivation)

$$w_H = \frac{1}{R'_{sig}(C_{eq} + C_{gs})}$$ where $R'_{sig} = 100K \| 18.25M$

$R'_{sig} = 98.802K$

$C_{eq} \Rightarrow$ (Short all external caps and only look at C_{gs} and C_{gd})

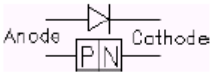
$\therefore C_{eq} = C_{gd}(1 + g_m(4.7K \| 10K)) = 0.84pF$

$\therefore w_H = \frac{1}{98.802K(0.84p + 1p)} = 5.5M$ rad/sec

$f_H \cong \underline{876\ Hz}$

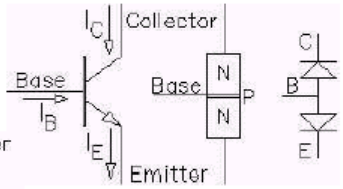
Introduction to Bipolar Junction Transistors (BJTs)

A transistor has three terminals-- the base, the collector, and the emitter. The current flow from the collector to the emitter (through the transistor) is controlled by the current flow from the base to the emitter. A small base current can control a much larger collector current.

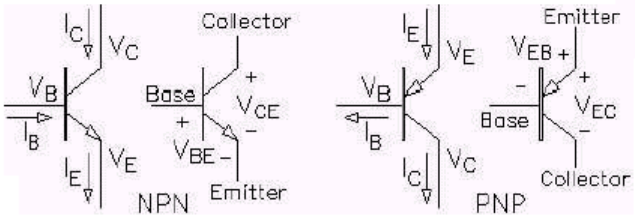


Bipolar junction transistors (BJTs) consist of three layers of doped silicon. The NPN transistor has a thin layer of P-doped silicon sandwiched between two layers of N-doped silicon. Each P-N junction can act like a diode. In fact, this is a fairly good way to check a transistor with an ohmmeter (set to the diode setting).

The base-emitter junction always acts like a diode, but because the base is very thin, it makes the other junction act like a controlled valve (details to come later).



Symbols and conventions



PNP: Replace v_{BE} with v_{EB} and v_{CE} with v_{EC} in equations below

Very High Level Overview of how a transistor works:

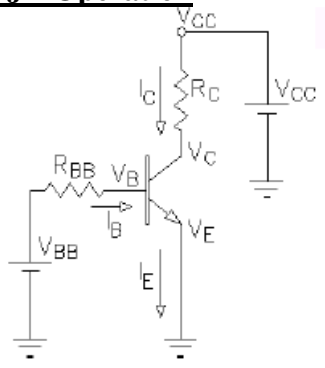
- A small amount of base current controls a large emitter (collector) current

Analogy:

- Think of the transistor as an "electronic" tap able to control a large flow of electrons *(from collector to emitter)* with only a small variation in the "handle" *(base)*
- Water Tap Analogy: (water spigot)

  → Large amounts of H_2O controlled by very small movement of the tap

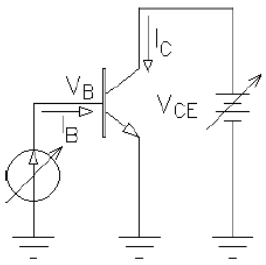
BJT Operation

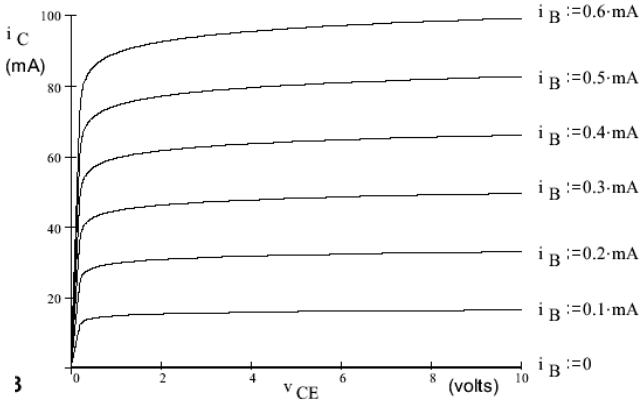


Modes or regions of operation (v_{BE} and v_{CE} are approximate)

Cutoff (off)	Active (partially on)	Saturation (fully on)
$v_{BE} < 0.7 \cdot V$	$v_{BE} \sim 0.7 \cdot V$	$v_{BE} \sim 0.7 \cdot V$
$i_B = 0$	$i_B > 0$	$i_B > 0$
$i_C = 0$	$v_{CE} \geq 0.7 \cdot V$	$v_{CE} = 0.2$ to $0.7 \cdot V$
	$i_C = \beta \cdot i_B = \alpha \cdot i_E$ controlled by the transistor	$i_C < \beta \cdot i_B$ limited by something outside of the transistor

Typical transistor curves





Summary of BJT Current-Voltage Relationships in the Active Mode:

$i_c = I_S e^{v_{BE}/V_T}$ (n=1 always for BJT) {Ebers-Moll equation}

$i_B = \frac{i_C}{\beta} = \left(\frac{I_S}{\beta}\right) e^{v_{BE}/V_T}$

$i_E = \frac{i_C}{\alpha} = \left(\frac{I_S}{\alpha}\right) e^{v_{BE}/V_T}$

Note: For the *pnp* transistor, replace v_{BE} with v_{EB}

$I_C = \alpha I_E = \beta I_B$ $I_E = (\beta+1) I_B$ $\beta = \frac{\alpha}{1-\alpha}$ $\alpha = \frac{\beta}{\beta+1}$

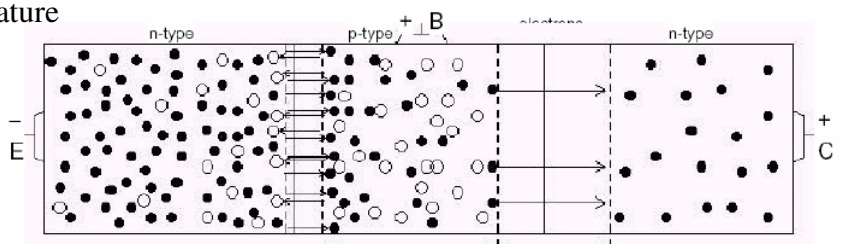
V_T=thermal voltage $\cong$ ~25mV at room temperature

Temperature dependencies

$v_{BE} = 0.7 \cdot V$ (decreases about 2.1 mV / °C)

at constant I_C: $\Delta V_{BE} = \frac{-2.1 \cdot mV}{degC}$

at constant V_{BE}: I_C increases by 8% per °C (10x per 30°C)



Method for solving DC voltages and currents of a BJT circuit:

1). Start by assuming transistor is in active mode
Either use given values for base-emitter voltage, or use
$V_{BE} = 0.7V$ (npn)
$V_{EB} = 0.7V$ (pnp)

2). Solve for the BJT node voltages and currents
- Voltages: sometimes can read off directly, otherwise use loop equation
- Once you have one current, you can get the other two from the active mode equations

3). Check to see if the solution is consistent!
$V_C \geq V_B > V_E$ npn active more explicitly: $V_{CB} \geq 0$, $V_{BE} \geq 0.7V$
$V_E > V_B \geq V_C$ pnp active more explicitly: $V_{CB} \geq 0$, $V_{EB} \geq 0.7V$

4). If the solution is consistent, stop → you are done
If not, the transistor is either in saturation or cutoff
→ go to 2)., however active mode equations **do not** apply!
→ Now use: saturation: $v_{BE} \approx 0.7V$ and $v_{CE} \approx 0.2V$ for npn
($v_{EB} \approx 0.7V$ and $v_{EC} \approx 0.2V$ for pnp)
cutoff: set all currents to approximately 0: $i_C = 0$ $i_E = 0$ $i_B = 0$

NPN ACTIVE AND ON when:

$v_{BE} \geq V_{BEon}$ ($V_{BEon} \cong 0.5V$)

$V_C \geq V_B > V_E$ and V_{CE}>0.2V

PNP ACTIVE AND ON when:

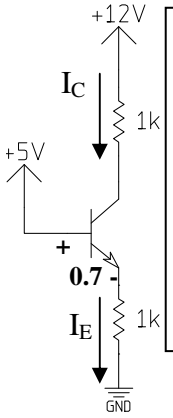
$v_{EB} \geq V_{EBon}$

$V_E > V_B \geq V_C$ and V_{EC}>0.2V

Example 29:

Find V_E and I_c for each circuit. Assume that $|V_{BE}| = 0.7V$ and $\beta = 40$. Both transistors are being operated in the active mode.

(a) NPN



$V_E = 5 - 0.7 = \boxed{4.3V}$

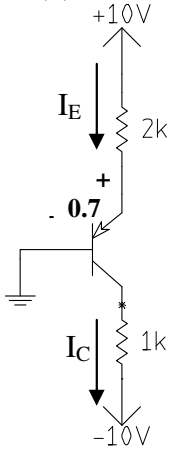
$I_E = \frac{V_E}{R_E} = \frac{4.3}{1k} = 4.3mA$

$I_c = \frac{\beta}{\beta+1} I_E = \frac{40}{41}(4.3mA) = \boxed{4.2mA}$

Check:

$V_C = 7.8V \geq V_B = 5V > V_E = 4.3V$

(b) PNP



$V_E = \boxed{0.7V}$

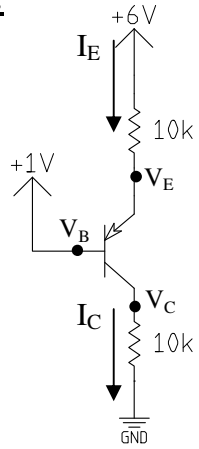
$I_E = \frac{10 - 0.7}{2k} \approx 4.7mA$

$I_c = \frac{\beta}{\beta+1} I_E = \boxed{4.5mA}$

Check:

$V_E = 0.7V > V_B = 0 \geq V_C = -5.5V$

Example 30:



Given: $|V_{BE}| = 0.7V$

Find: I_C, V_C, and V_E

Recall: For active mode pnp, should have

$V_E > V_B > V_C$

(All dc, so use caps)

1). Assume active mode

2). Solve:

$V_E = V_B + 0.7V = 1.7V (V_B = 1V)$

$I_E = \frac{6 - V_E}{10k} = \frac{6 - 1.7}{10k} = 0.43mA$

$I_c = \alpha I_E = \frac{\beta}{\beta+1} I_E \approx 0.43mA$

$V_C = 10k(I_c) = 4.3V$

3). Check: $V_C = 4.3 > V_B = 1V$ → can not be active

4). Start over with assumption that transistor is cutoff:

To see if cutoff, set all currents to 0 or in other words take transistor out of circuit and should get $V_B > V_E$ and $V_B > V_C$

$V_E = 6V$, $V_B = 1V$ → $V_E > V_B$ → Can not be cutoff (pnp!!)

Transistor must be saturated:

To see if saturation, set $V_{EB} = 0.7V$ and $V_{EC} = 0.2V$

And should get $V_C > V_B$ for FB CBJ

Need to recalculate values (i.e. ones from active mode assumption are not valid)

Active mode equations do not apply → need to just use V=IR, KVL,KCL

Saturation analysis=>

$V_E = V_B + 0.7 = 1.7$

$I_E = 0.43mA$

$V_C = 1.7 - 0.2 = 1.5V$

$I_C = \frac{1.5}{10k} = 0.15mA$

$V_{CB} = 0.7 - 0.2 = 0.5V$

$V_C > V_B$ → It is saturated!

Example 31

$\beta = 100$

$V_{BB} = I_B R_{BB} + V_{BE} + I_E R_E$

$I_B = \dfrac{I_E}{\beta + 1}$

$I_E = \dfrac{V_{BB} - V_{BE}}{R_E + \left[R_{BB} \big/ (\beta + 1) \right]} = \dfrac{5 - 0.7}{3k + \left(33.3k \big/ 101 \right)} = 1.29mA$

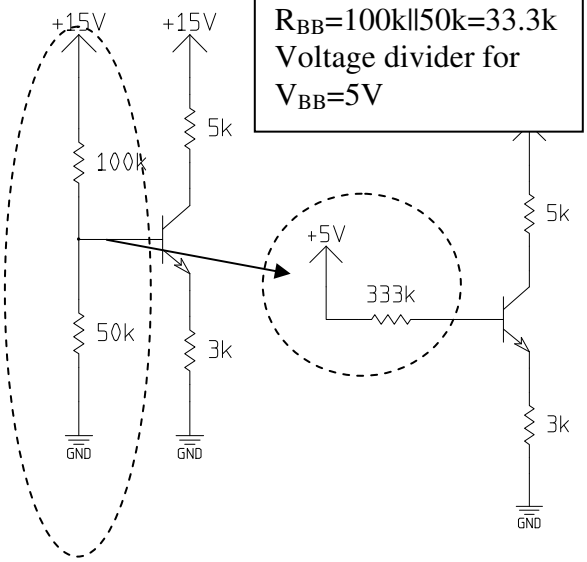
$V_E = I_E R_E = (1.29mA)(3k) = 3.87V$

$I_B = \dfrac{1.29mA}{101} = 12.8mA$

$V_B = V_{BE} + V_E = 0.7 + 3.87 = 4.57V$

$I_C = \alpha I_E = 0.99(1.29m) = 1.28mA$

$V_C = 15V - I_C R_C = 15V - (1.28m)(5k) = 8.6V$



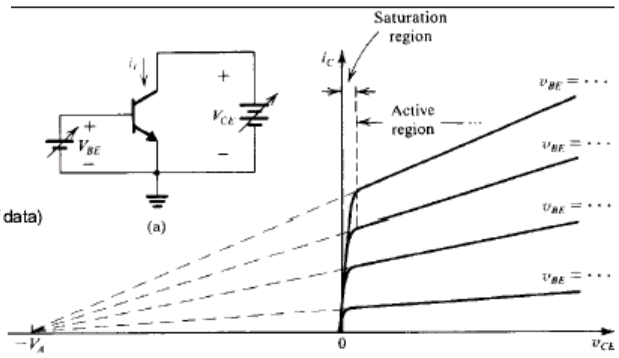
Thevenin:
R_{BB}=100k||50k=33.3k
Voltage divider for
V_{BB}=5V

Early Voltage and output resistance

β depends on the effective base width, W which depends on V_{CB}. This leads to the Early effect, which is expressed as an output resistance.

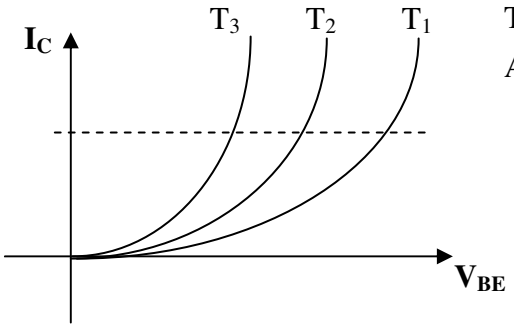
output resistance = $r_o = \dfrac{V_A}{I_C}$ Early voltage.

(guess V_A ~ 100 V in absence of data)



Temperature Effects:

NPN Transistor Characteristic



$T_3 > T_2 > T_1$

As $T \uparrow, I \uparrow$ for fixed V_{BE}

Thermal runaway: $T \uparrow \rightarrow I_C \uparrow \rightarrow P_D \uparrow \rightarrow T \uparrow \rightarrow I_C \uparrow \rightarrow P_D \uparrow \rightarrow \cdots$

Bipolar Junction Transistor (BJT) bias in the active region

Bias: Want a stable I_C for any transistor at any temperature

To work as an linear amplifier, a transistor must operate in the active region. To work in the active region i_B and i_C must be positive for all values of the AC signals -- they must be *biased* to some positive DC value. The AC signals will swing above and below these DC values. Furthermore, the transistor must not saturate, or it will lose control of i_C.

Bias should not depend too much on the value of β

β can vary widely from transistor to transistor of the same part number. No one wants to individually test transistors to find ones that will work in your circuit.

Bias should not depend too much on the value of V_{BE}

The relationship between V_{BE} and I_C is far too dependent on temperature and, like β, varies from transistor to transistor.

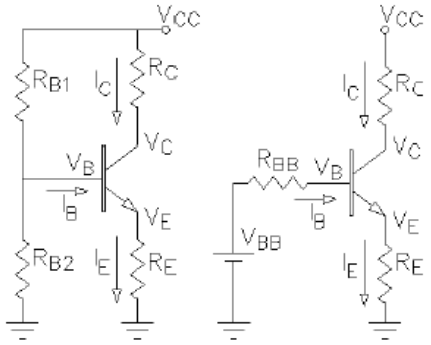
Stable bias set by a stable V_B and an R_E

As we saw last time if we set V_B with a battery (V_{BB}) then I_C is very stable. Instead of I_B controlling I_C through the unpredictable β, a stable V_B sets V_E (V_B - 0.7V) and R_E sets I_E and hence I_C. I_B then takes care of itself, and adjusts to compensate for different βs and temperatures. Unfortunately it's pretty impractical. You don't want two power supplies and besides, you can't get a signal to the base. Still, most schemes to achieve stable bias work by setting a stable voltage at the base for any reasonable I_B,

Voltage-divider bias

To make the left circuit look like the right one:

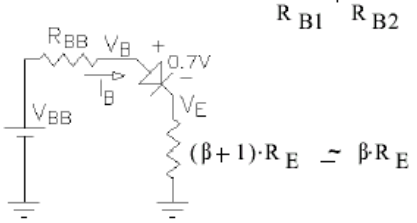
$$V_{BB} = V_{CC}\cdot\frac{R_{B2}}{R_{B1}+R_{B2}} \qquad R_{BB} = \frac{1}{\frac{1}{R_{B1}}+\frac{1}{R_{B2}}}$$



Use Thevenin's analysis

Both circuits:

$$I_B = \frac{V_{BB}-0.7\cdot V}{R_{BB}+(\beta+1)\cdot R_E} \qquad I_C = \beta\cdot I_B \simeq I_E$$



Note: Often in quick-and-dirty analysis you can neglect the base current, I_B. In that case:

$$V_B = V_{BB} \qquad V_E = V_B - 0.7\cdot V \qquad I_E = \frac{V_E}{R_E} \simeq I_C$$

This assumption is OK if: $R_{BB} < \beta\cdot R_E$

Quick check: $R_{B1} < 10\cdot R_E$ OR $R_{B2} < 10\cdot R_E$ Should result in <10% error if $\beta \geq 100$

$$V_C = V_{CC} - I_C\cdot R_C \qquad V_E = I_E\cdot R_E$$

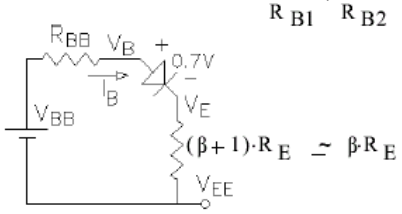
$$V_{CE} = V_C - V_E$$

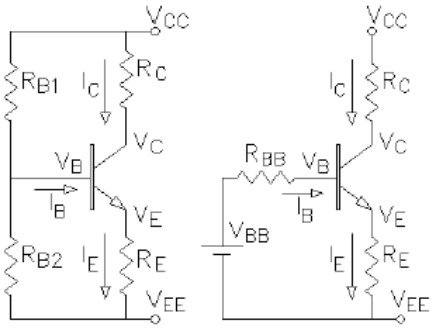
Always check that $V_{CE} > 0.2$ V to see if the ciruit was really in the active region.

What if V_{EE} is not ground ?

$$V_{BB} = (V_{CC}-V_{EE})\cdot\frac{R_{B2}}{R_{B1}+R_{B2}} + V_{EE} \qquad R_{BB} = \frac{1}{\frac{1}{R_{B1}}+\frac{1}{R_{B2}}}$$

$$I_B = \frac{V_{BB}-0.7\cdot V - V_{EE}}{R_{BB}+(\beta+1)\cdot R_E} \qquad I_C = \beta\cdot I_B \simeq I_E$$





If you can neglect the base current, I_B. In that case: $V_B = V_{BB}$ $V_E = V_B - 0.7\cdot V$ $I_E = \frac{V_E - V_{EE}}{R_E} \simeq I_C$

$V_C = V_{CC} - I_C\cdot R_C$ $V_E = I_E\cdot R_E + V_{EE}$ $V_{CE} = V_C - V_E$ Always check that $V_{CE} > 0.2$ V to see if the ciruit was really in the active region.

The equations above and on the last page are for the circuits shown, adapt them as necessary to fit your actual circuit.

BJT Bias Design

Decisions that you make for the bias will effect many other qualities of the circuit, so you should know some of your wants and expectations up front. See the tradeoffs below. Design is often an iterative process. Try something, see if it works, modify, try again. The parameters below are listed in good order for design, i.e. you usually start by selecting I_C.

select	Tradeoffs: lower value	higher value
I_C	less power form supply less power dissipated in transistor higher input impedance	larger available output voltage swing more output power available lower output impedance

Don't want β variations to affect I_C, so make sure that I_B is the one to vary when β changes: Usually make $\beta R_E > R_{BB}$.

Temperature effects on I_C: $\frac{\Delta V_{BE}}{\Delta T} = -2.1 \cdot \frac{mV}{degC}$ (constant I_C) and: For every 60 mV increase in V_{BE}, I_C will increase by factor of 10

If V_{BE} is held constant, I_C will increase by factor of 10 for every 30 °C increase in temperature.

Try to swamp the V_{BE} changes with a much bigger voltage across R_E. For a temperature range of

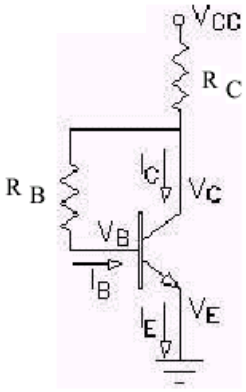
Ex: 0 to 40 degC, V_{BE} changes 84 mV. $24 \cdot 84 \cdot mV = 2 \cdot V$ $V_E = 2 \cdot V$ swamps ΔV_{BE} pretty well (24x).

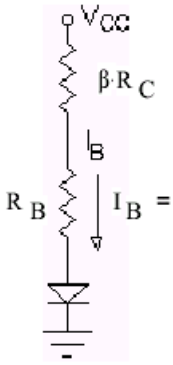
select	Tradeoffs: lower value	higher value
V_E	(CE & CB amps) larger available output voltage swing (CC amp) Bias for output swing requirements	Better β and thermal stability (CC & CB, CE if unbypassed) higher input impedance

calculate $R_E = \frac{V_E}{I_C}$ $V_B = V_E + 0.7 \cdot V$ This will dictate ratio of $\frac{R_{B2}}{R_{B1}} = \frac{V_{BB} - V_{EE}}{V_{CC} - V_{BB}}$

select	Tradeoffs: lower value	higher value
R_{B1} & R_{B2}	Better β stability	(CE & CC) higher input impedance less power form supply

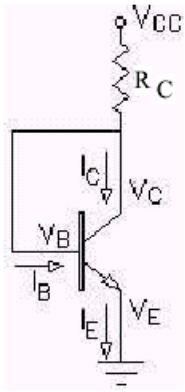
A couple of other bias schemes





$I_B = \frac{V_{CC} - 0.7 \cdot V}{R_B + \beta \cdot R_C}$

The bigger R_C is with respect to R_B, the more stable I_C is



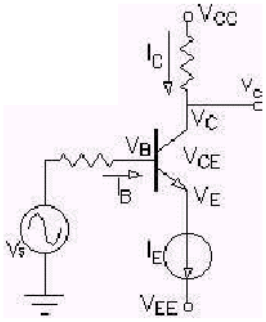
Taken to extremes, IC is now very stable at:

$I_C = \frac{V_{CC} - 0.7 \cdot V}{R_C}$

Seems like a useless circuit, but...

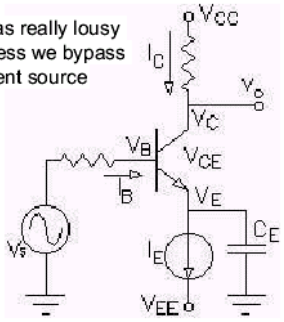
Current source bias: We could make the bias current very stable if we had a current source

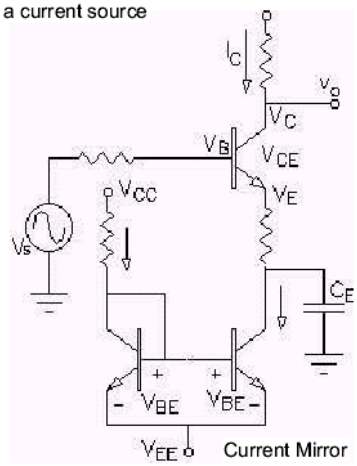
If we can make current sources (drains), then...



For a perfect current source, $R_E = \infty$

which has really lousy gain unless we bypass the current source





Current mirrors A way to make a current source (drain)

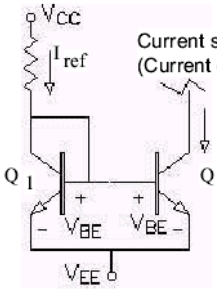
$$I_{C1} = \frac{V_{CC} - V_{EE} - 0.7\cdot V}{R_C} = I_{ref}$$

Recall that v_{BE} is really not exactly 0.7V, from Ebers-Moll eq.: $I_C = I_S \cdot e^{\frac{v_{BE}}{V_T}}$

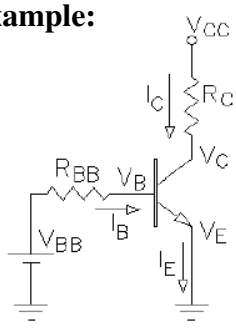
Because $V_{BE1} = V_{BE2}$, $I_{C1} = I_{C2}$

We can get a current source (usually called a current drain in this type of configuration). I could make a positive source if I used PNP transistors.

But, the transistors must be identical, and at the same temperature, like in an IC.



Example:



Say: $V_{CC} := 7\cdot V$

As long as $V_{CC} < 0.2V$, this simple circuit is always in the active region.

R_c is very common in transistor circuits. If the collector current is fluctuating according to some signal, those fluctuations will cause voltage fluctuations across R_c which could be the output signal voltage of the circuit.

What if we want $I_C := 10\cdot mA$ and $V_C := 3\cdot V$ then $R_C := \frac{V_{CC} - V_C}{I_C}$ $R_C = 400\cdot\Omega$

Let's assume that $\beta := 200$ $I_B := \frac{I_C}{\beta}$ $I_B = 0.05\cdot mA$

Say $V_{BB} := 2.5\cdot V$ then $R_{BB} := \frac{V_{BB} - 0.7\cdot V}{I_B}$ $R_{BB} = 36\cdot k\Omega$

All looks hunky-dory, right?

What if $\beta := 100$? $I_B = \frac{V_{BB} - 0.7\cdot V}{R_{BB}} = 0.05\cdot mA$ no change here, looks good so far.

$I_C := \beta\cdot I_B$ $I_C = 5\cdot mA$ Yuk, that changed by half.

$V_C := V_{CC} - I_C\cdot R_C$ $V_C = 5\cdot V$ At least V_C only changed by 2V. Still, that may be too much.

At least we're still in the active region ($V_{CE} > 0.2V$).

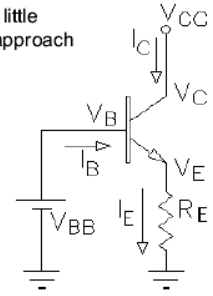
What if $\beta := 400$? $I_B = \frac{V_{BB} - 0.7\cdot V}{R_{BB}} = 0.05\cdot mA$ again, no change here.

$I_C := \beta\cdot I_B$ $I_C = 20\cdot mA$ Oh oh, that doubled.

$V_C := V_{CC} - I_C\cdot R_C$ $V_C = -1\cdot V$ Oops, that can't be good. In fact, we have to assume that we're out of the active region -- way bad...

Must recalculate I_C and V_C. $V_C := 0.2\cdot V$ (Saturation) $I_C := \frac{V_{CC} - 0.2\cdot V}{R_C}$ $I_C = 17\cdot mA$

Let's try a little different approach



Again, let's design for $I_C := 10\cdot mA$

$V_E := V_{BB} - 0.7\cdot V$ It is common here to assume: $I_E := I_C$

$R_E := \frac{V_E}{I_E}$ $R_E = 180\cdot\Omega$ $I_E = 10\cdot mA$

but actually, $I_C = \alpha\cdot I_E = \frac{\beta}{\beta+1}\cdot I_E$

If $\beta := 100$ $\alpha := \frac{\beta}{\beta+1}$ $I_C = \alpha I_E = 9.901\cdot mA$ $I_B = \frac{I_C}{\beta} = 0.1\cdot mA$

If $\beta := 400$ $I_C = \frac{\beta}{\beta+1}\cdot I_E = 9.975\cdot mA$ $I_B = \frac{I_C}{\beta} = 0.025\cdot mA$

Now that's more like it, now I_B changes instead of I_C.

BJT basic amplifier:

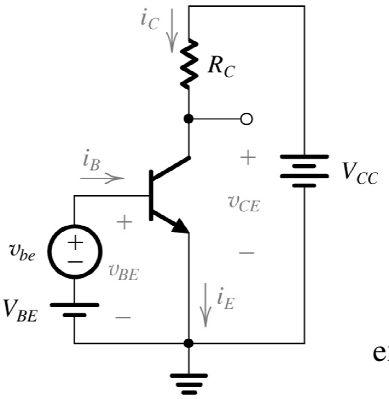
DC:

$$I_C = I_s e^{V_{BE}/V_T}$$

$$I_E = \frac{I_C}{\alpha}$$

$$I_B = \frac{I_C}{\beta}$$

$$V_C = V_{CE} = V_{CC} - I_C R_C$$



DC and AC)

$$\underbrace{I_s e^{V_{BE}/V_T}}_{I_c} e^{v_{be}/V_T}$$

$$= I_c + \frac{I_c}{V_T} v_{be}$$

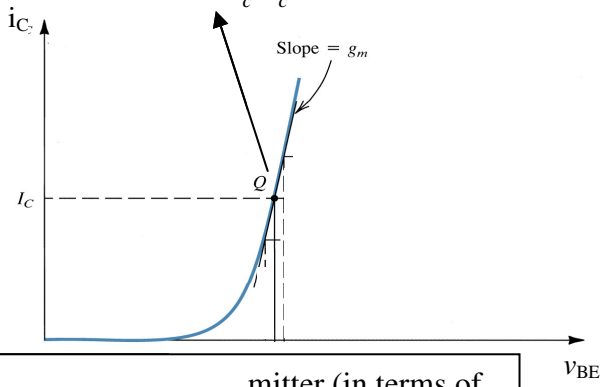
expand by $e^x \approx 1 + x$ for x<<1 ($V_{be} << V_T$)

Look at signal component only: (a)

$$i_c = \frac{I_c}{V_T} v_{be}$$

$$g_m = \frac{I_c}{V_T}$$

$$g_m = \left.\frac{\partial i_c}{\partial v_{BE}}\right|_{i_c = I_c}$$



Transconductance

Dynamic forward resistance of BE junction

Input Resistance:

ıse (in

$\frac{c}{T} v_{be}$

ntities

mitter (in terms of

ge($\alpha \approx 1$): good

imation is $r_e \approx \frac{1}{g_m}$

$$= (\beta + 1) r_e$$

Summary of ac parameters:

$$g_m = \frac{I_c}{V_T} \qquad r_\pi = \frac{V_T}{I_B} = \frac{\beta}{g_m}$$

$$r_o \cong \frac{V_A}{I_c} \qquad r_e = \frac{V_T}{I_E}$$

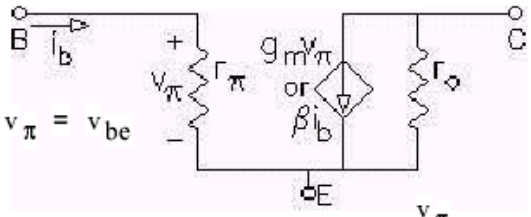
$$i_c = g_m v_{be}$$

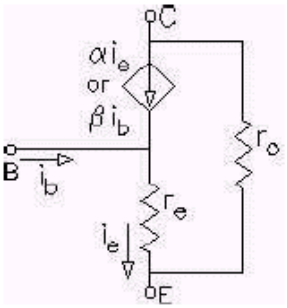
$$\frac{v_c}{v_{be}} = -g_m R_c$$

Small-signal equivalent circuit models

Same concept as that of the MOSFET.

ead of r_π





$$r_\pi = (\beta+1)\cdot r_e \qquad i_b = \frac{v_\pi}{r_\pi}$$

$$\beta \cdot i_b = \beta \cdot \frac{v_\pi}{r_\pi} = \beta \cdot \frac{v_\pi}{(\beta+1)\cdot r_e}$$

$$g_m = \frac{\beta}{(\beta+1)\cdot r_e} = \frac{\alpha}{r_e} \simeq \frac{1}{r_e} = \text{transconductance}$$

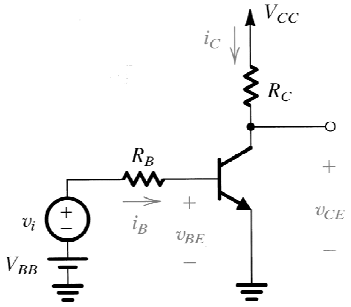
brid-π:

Method for analyzing transistor amplifier circuits:

1). Determine dc operating point, specifically I_C
   (Set ac sources to 0!!)
   Note: Use method for analyzing BJT circuits at DC
2). Calculate small-signal parameters: g_m , r_π, and/or r_e
3). Set dc sources to 0
4). Replace the transistor with one of the equivalent small-signal models
5). Analyze the circuit as usual → linear circuit analysis

Example

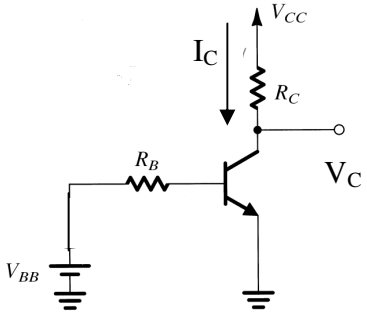
Circuit:
β =100, V_{BB}=3V, R_C=3k
R_B=100k, V_{CC}=10V



Find the voltage gain, v_o/v_i

1). DC analysis: set v_i to 0 Assume V_{BE} = 0.7V Assume active

Redraw circuit with just dc part:



$$I_B = \frac{V_{BB} - V_{BE}}{R_{BB}} = \frac{3-0.7}{100} = 0.023mA$$

$$I_C = \beta I_B = 2.3mA$$

$V_C = V_{CC} - I_C R_C = 10\text{-}2.3(3) = 3.1V$

Double check your values:

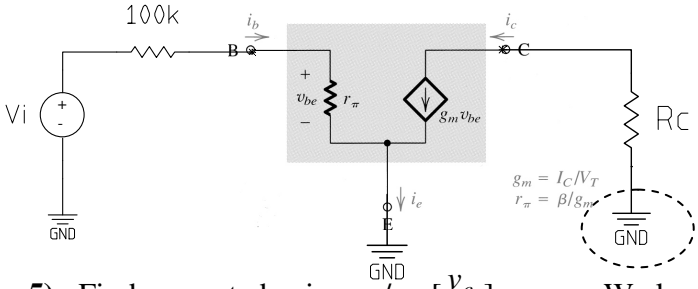
$V_C > V_B > V_E$ 3.1>0.7>0 YES!

2). Calculate small-signal parameters:

$$g_m = \frac{I_C}{V_T} = \frac{2.3}{25} = 92mA/V \qquad r_e = \frac{V_T}{I_E} = \frac{25}{(2.3/0.99)} = 10.8\Omega \qquad r_\pi = \frac{\beta}{g_m} = \frac{100}{92} = 1.09k\Omega$$

3). And 4). Set dc sources to 0 and replace transistor with equivalent model

Model:



Vcc grounded for ac!

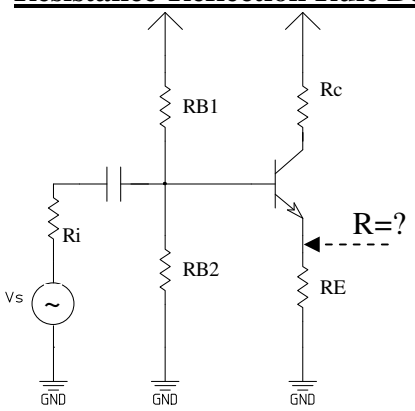
5). Find requested gain: $v_o/v_i=[\frac{v_c}{v_i}]$ We know $v_o = v_c = -g_m\, v_{be}\, R_C$

Now need v_{be} in terms of v_i

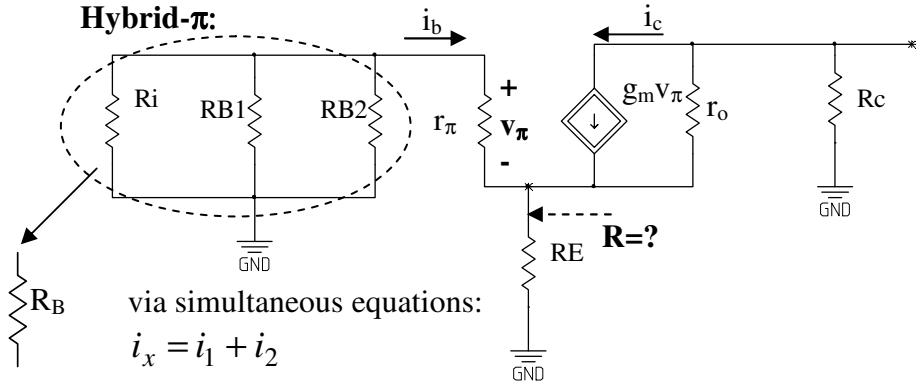
Voltage division: $v_{be} = \dfrac{r_\pi}{r_\pi + 100k} v_i$

$$\frac{v_o}{v_i} = -g_m \frac{r_\pi}{r_\pi + 100k} R_C = -92.3k \frac{1.09k}{100k + 1.09k} = \boxed{-3.04V/V}$$

Resistance-Reflection Rule Between Base and Emitter:



Hybrid-π:



via simultaneous equations:

$$i_x = i_1 + i_2$$

$$i_1 = \frac{v_x}{R_E}, \quad i_2 = -i_e = -(i_b + i_c) = -i_b(\beta + 1)$$

$$v_\pi = i_b r_\pi, \quad i_c = g_m v_\pi$$

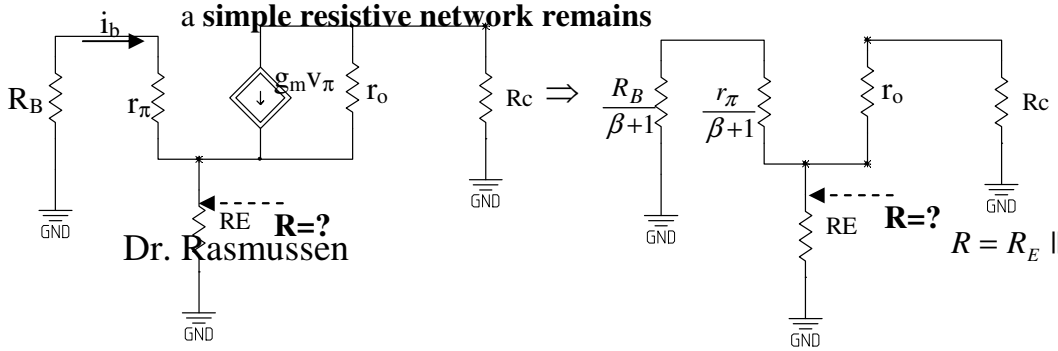
etc.

⋮

$$R_x = R_E \,\|\, \frac{r_\pi + R_B}{(\beta+1)} \,\|\, (r_o + R_e) \approx R_E \,\|\, (r_e + \frac{R_B}{(\beta+1)})$$

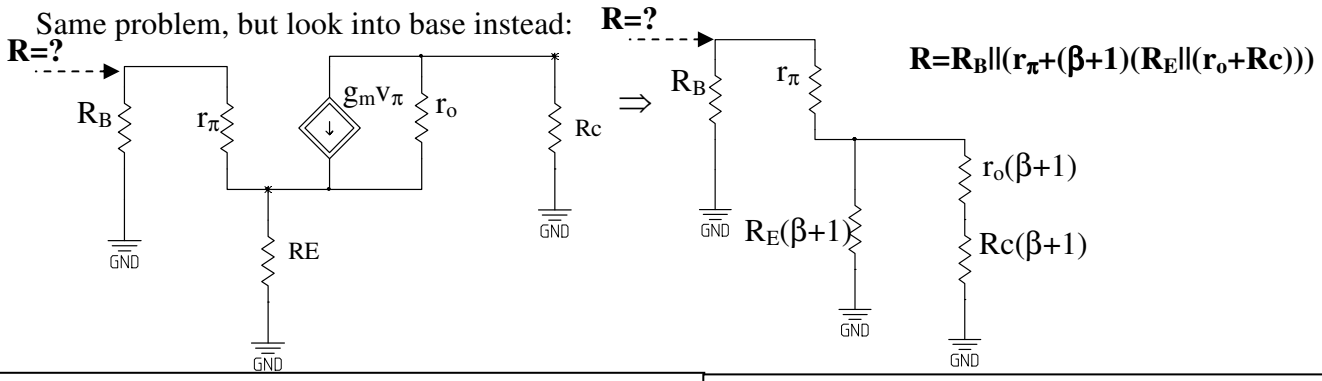
1. Eliminate VCCS
2. Scale all resistors with i_b through Thevenin by $\dfrac{1}{(\beta+1)}$ and

a **simple resistive network remains**



$$R = R_E \,\|\, \frac{r_\pi + R_B}{(\beta+1)} \,\|\, (r_o + R_e)$$

Same problem, but look into base instead:



Summary of Resistance-Reflection Rule between base and emitter:

Applies only when you want to reflect a resistor from emitter to base or base to emitter circuit

Review of rule:

1). Temporarily remove dependent source βi_b or $g_m v_{be}$

2). When looking into base: Replace resistors on emitter side with

"R" x (β + 1) or

When looking into emitter: Replace resistors on base side with "R" / (β + 1)

3). Treat circuit as a resistive network and find equivalent resistance

This works because $i_b = \frac{i_e}{\beta+1}$

In a nutshell: To reflect a resistor from:

E→ B multiply by (β + 1)

B→E divide by (β + 1)

Things to keep in mind:

- Rule does NOT work for impedance looking into colle – it is a reflection rule between base and emitter
- It works because $i_b = \frac{i_e}{\beta+1}$ which is a relationship betw the base and emitter current!
- Finding R_{in} or R_{out} → this is just finding Thevenin equivalent resistance, R_{Th}

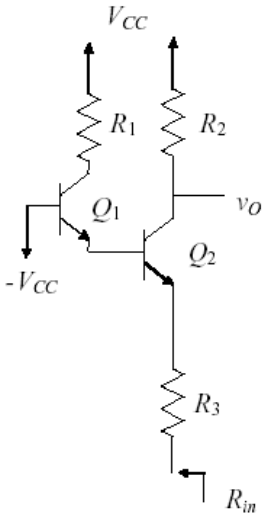
  Possible methods now that you can use:

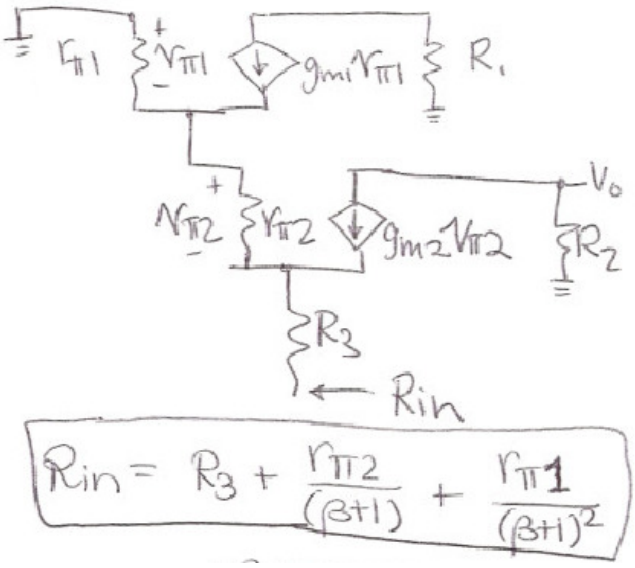
  1). Using the resistance Reflection Rule

  2). Using Thevenin equivalent methods– use these to double check homework, but on exam will not likely have time
- R_{in} or R_{out} is always between a node and ground – follo all paths to ground from that node
- Applying the Reflection Rule is like turning off depend sources and multiplying resistances by (β + 1) or divid resistance by (β + 1) and treating circuit as just a resist network → Note that this only works because the dependent source is being accounted for through the (β 1) factor!

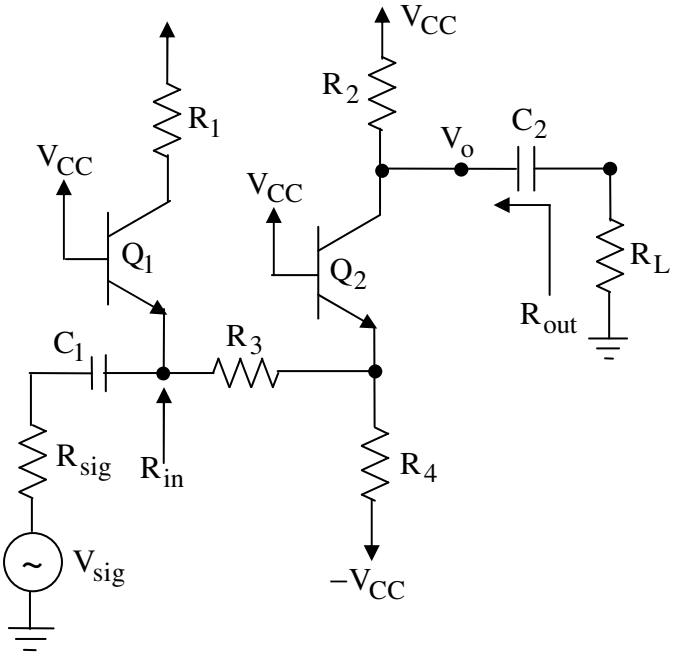
Example: Assume the transistors below have a finite β and an infinite Early voltage.

- Write an expression for the input resistance R_{in} in the circuit shown below. Your expression should include *only* real resistances (R_1, R_2, R_3, or a subset of these) and possibly β, r_{e1} or $r_{\pi 1}$, and r_{e2} or $r_{\pi 2}$. (Assume both transistors have the same β.) Circle your answer. *Hint: Use Resistance-Reflection rule*





Common-Base

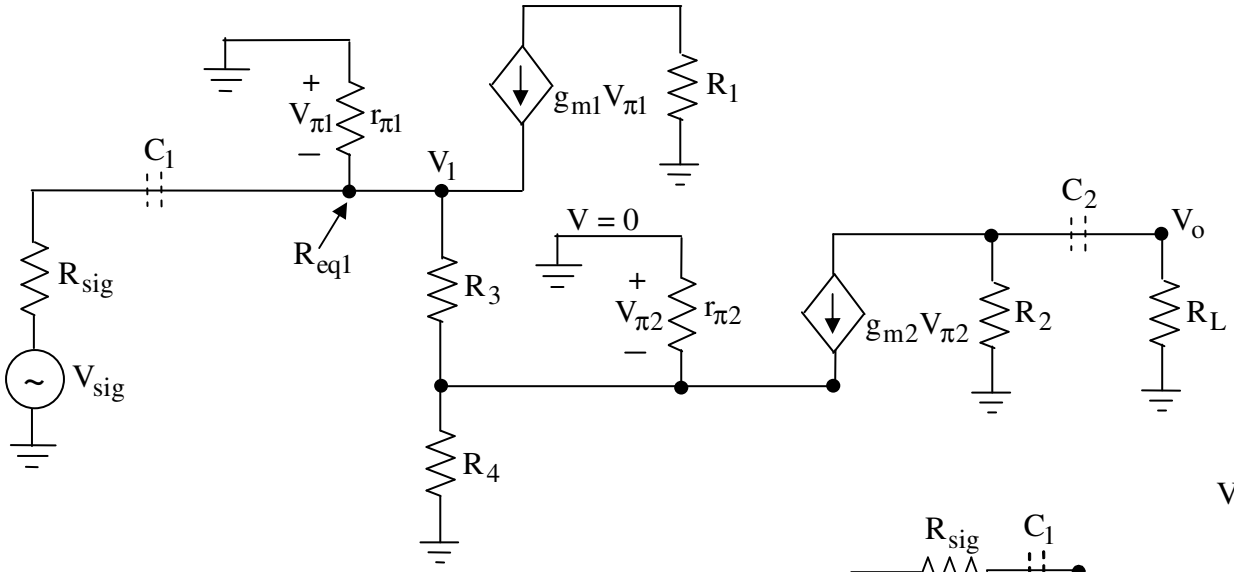


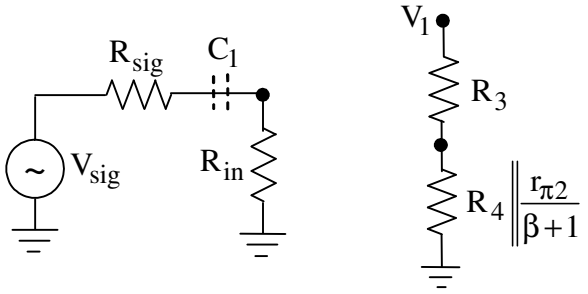
$C_1 = 10\text{ pF}, \quad C_2 = 10\text{ nF}, \quad \beta = 100$

Ignore r_o

$$\boxed{R_{out} = R_2}$$

$$\boxed{R_{in} = \frac{r_{\pi 1}}{\beta+1} \left\| \left(R_3 + R_4 \left\| \frac{r_{\pi 2}}{\beta+1} \right. \right) \right.}$$





$$V_o = -g_{m2} V_{\pi 2} \left(R_2 \| R_L \right)$$

$$V_{\pi 2} = \frac{-V_1 \left(R_4 \left\| \frac{r_{\pi 2}}{\beta+1} \right. \right)}{\left(R_4 \left\| \frac{r_{\pi 2}}{\beta+1} \right. \right) + R_3} \qquad V_1 = \frac{V_{sig} \left(R_{in} \right)}{R_{in} + R_{sig}}$$

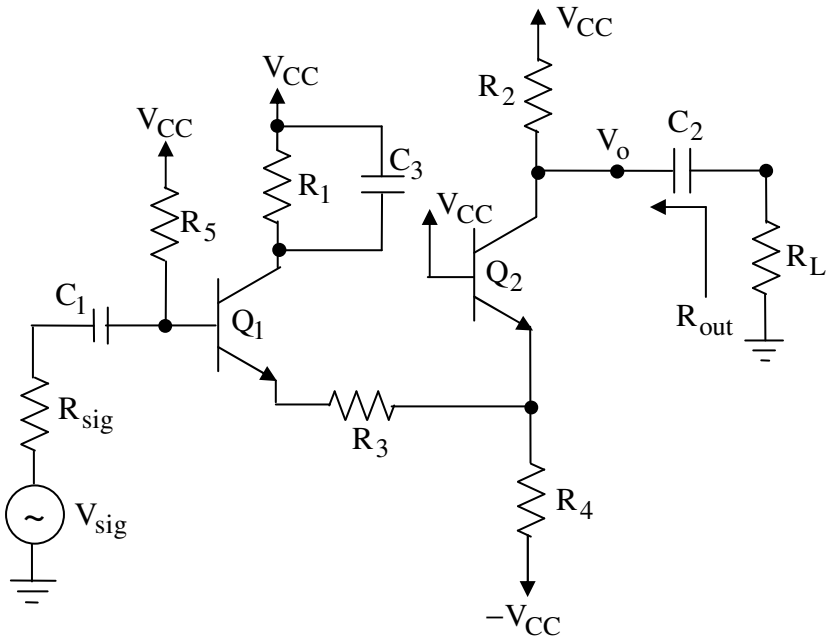
$$\boxed{\frac{V_o}{V_{sig}} = \frac{g_{m2} \left(R_2 \| R_L \right) \left(R_4 \left\| \frac{r_{\pi 2}}{\beta+1} \right. \right) R_{in}}{\left[\left(R_4 \left\| \frac{r_{\pi 2}}{\beta+1} \right. \right) + R_3 \right] \left[R_{in} + R_{sig} \right]}}$$

Low frequency poles $\Rightarrow$

① $\boxed{\dfrac{1}{C_2 \left(R_2 + R_L \right)}}$ ② $\boxed{\dfrac{1}{C_1 \left(R_{sig} + R_{in} \right)}}$

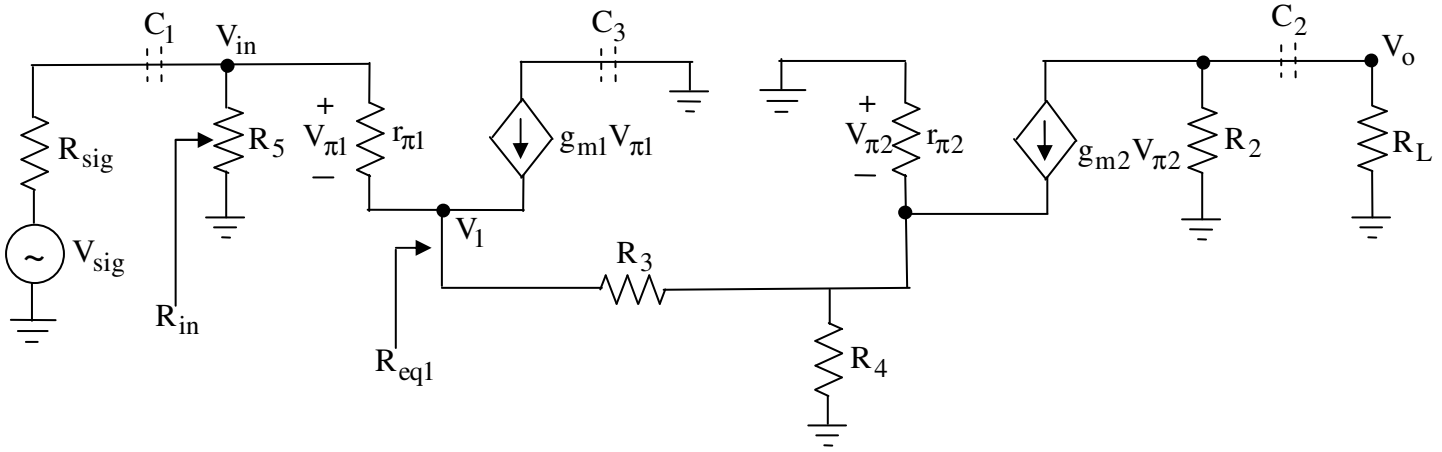
Capacitor * (R seen at cap nodes)

2 Stage ⇒ Common Collector/Common Base



$$R_{out} = R_2$$

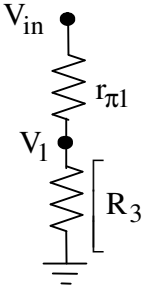
$$R_{in} = R_5 \left\| \left[r_{\pi 1} + \left(R_3 + R_4 \left\| \frac{r_{\pi 2}}{\beta+1} \right. \right) (\beta+1) \right] \right.$$



$$V_o = -g_{m2} V_{\pi 2} \left(R_2 \| R_L \right)$$

$$V_{\pi 2} = \frac{-V_1 \left(R_4 \left\| \frac{r_{\pi 2}}{\beta+1} \right. \right)}{\left(R_4 \left\| \frac{r_{\pi 2}}{\beta+1} \right. \right) + R_3}$$

$$V_1 = \frac{V_{in} \cdot R_{eq1}}{R_{eq1} + r_{\pi 1}}$$



$$\left[R_3 + \left(R_4 \left\| \frac{r_{\pi 2}}{\beta+1} \right. \right) \right] (\beta+1) = R_{eq1}$$

$$V_{in} = \frac{V_{sig} \cdot R_{in}}{R_{in} + R_{sig}}$$

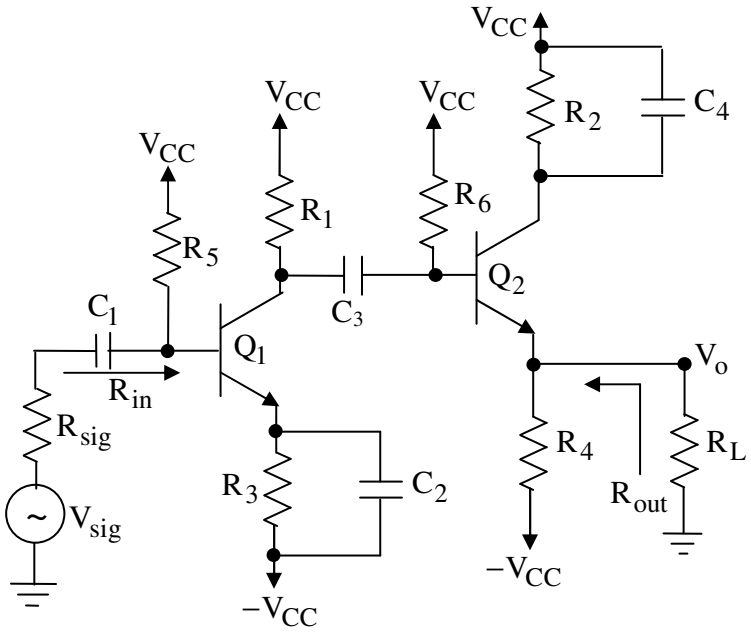
Low frequency poles ⇒

$$\frac{V_o}{V_{sig}} = \frac{g_{m2} \left(R_2 \| R_L \right) \left(R_4 \left\| \frac{r_{\pi 2}}{\beta+1} \right. \right) R_{in} \cdot R_{eq1}}{\left[\left(R_4 \left\| \frac{r_{\pi 2}}{\beta+1} \right. \right) + R_3 \right] \left[R_{in} + R_{sig} \right] \left[R_{eq1} + r_{\pi 1} \right]}$$

① $\dfrac{1}{C_2 \left(R_2 + R_L \right)}$ ② $\dfrac{1}{C_3 \cdot R_1}$

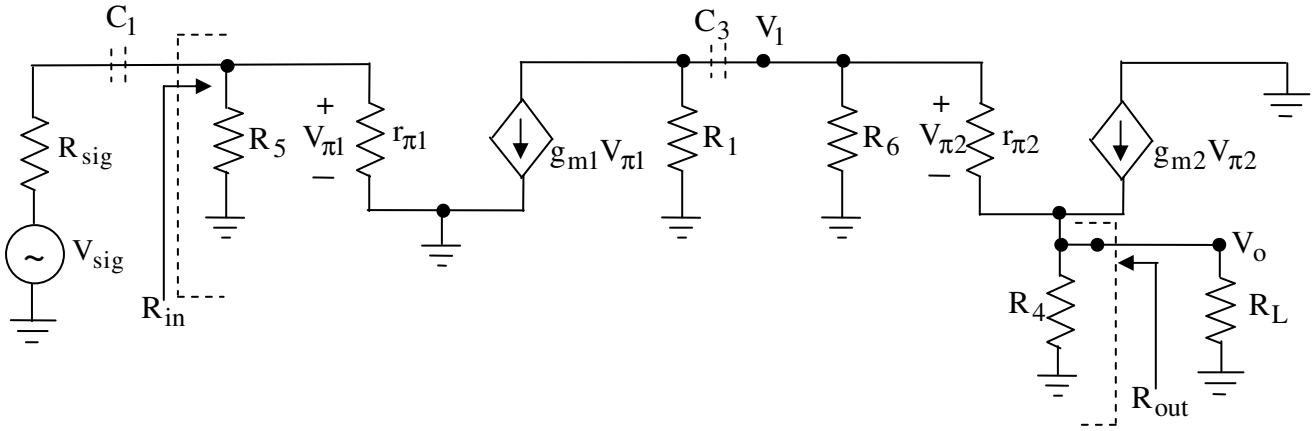
③ $\dfrac{1}{C_1 \left(R_{sig} + R_{in} \right)}$

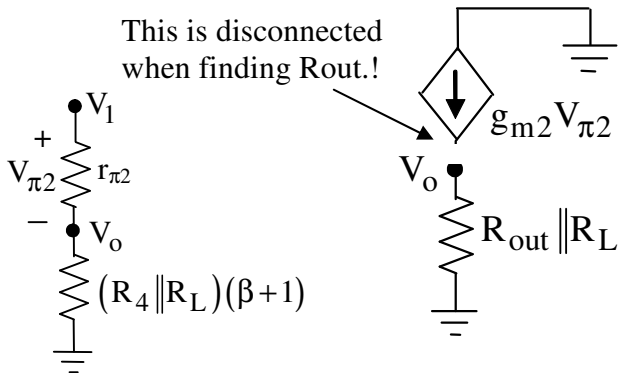
2 Stage ⇒ Common-Emitter/Common-Collector



$$R_{out} = \left[R_4 \left\| \left(\frac{r_{\pi 2}}{\beta+1} + \frac{R_6 \| R_1}{\beta+1} \right) \right. \right]$$

$$R_{in} = R_5 \| (r_{\pi 1})$$





$$Vo = V_1 - V_{\pi 2} \text{ OR } Vo = \frac{(R_4 \| R_L)(\beta+1)V_1}{[(R_4 \| R_L)(\beta+1)) + r_{\pi 2}]}$$

$$V_1 = -g_{m1} V_{\pi 1} \left[R_1 \left\| R_6 \right\| \left(r_{\pi 2} + (R_4 \| R_L)(\beta+1) \right) \right]$$

$$V_{\pi 2} = \frac{V_1 (r_{\pi 2})}{r_{\pi 2} + (R_4 \| R_L)(\beta+1)}$$

$$V_{\pi 1} = \frac{V_{sig} (R_5 \| r_{\pi 1})}{(R_5 \| r_{\pi 1}) + R_{sig}}$$

$$\frac{Vo}{Vsig} = \frac{(R_4 \| R_L)(\beta+1))}{[(R_4 \| R_L)(\beta+1)) + r_{\pi 2}]} \cdot \frac{(-g_{m1})[R_1 \| R_6 \| (r_{\pi 2} + (R_4 \| R_L(\beta+1))))]}{[(R_5 \| r_{\pi 1}) + R_{sig}]}$$

Low frequency poles ⇒ **NOTE THAT C_4 IS NOT SEEN BY OUTPUT – Do not need**

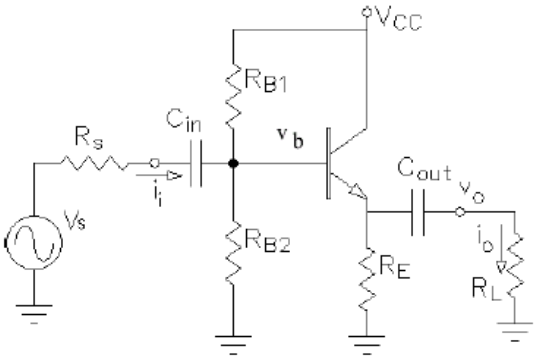
$$\frac{1}{C_1 (R_{sig} + R_{in})}$$ en $$\frac{1}{C_2 \cdot R_3}$$ $$\frac{1}{C_3 \left(R_1 + \left(R_6 \left\| \left(r_{\pi 2} + (R_4 \| R_2)(\beta+1) \right) \right) \right)}$$ ing $$\frac{1}{C_4 \cdot R_2}$$

Common collector (CC)

The circuits shown are typical arrangements. Note that V_{EE} is often 0 V (ground). The equations below are for these circuits, adapt them as necessary to fit your actual circuit.

Voltage gain about 1. Good for current gain, or to match a high impedance source to a low impedance load.

The small-signal emitter resistance is right in the emitter of the transistor (where the arrow is).



Recall that the emitter resistor looks β times as big from the base's point-of-view. That's also true for signals

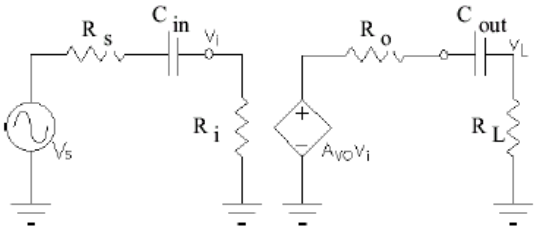
Input impedance: $R_i = R_{B1} \| R_{B2} \| \beta \cdot (r_e + R_E \| R_L)$

The opposite effect also works, resistors at the base look β times smaller from the emitter's point-of-view.

Output impedance: $R_o = R_E \| \frac{r_e + R_{B1} \| R_{B2} \| R_S}{\beta}$

Low frequency corner frequencies

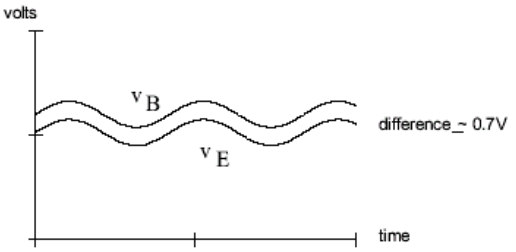
$$f_{CL1} = \frac{1}{2 \cdot \pi \cdot (R_S + R_i) \cdot C_{in}} \qquad f_{CL2} = \frac{1}{2 \cdot \pi \cdot (R_L + R_o) \cdot C_{out}}$$



From the signal analysis, the only thing between the base signal and the output signal is r_e. To find the output, just use the voltage divider equation.

Voltage gain: $A_v = \frac{v_o}{v_b} = \frac{R_E \| R_L}{r_e + R_E \| R_L} \simeq 1$

OR: $\frac{v_o}{v_s} = \frac{R_i}{R_S + R_i} \cdot \frac{R_E \| R_L}{r_e + R_E \| R_L}$

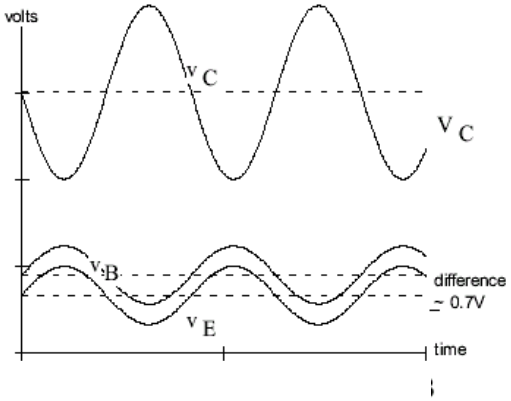


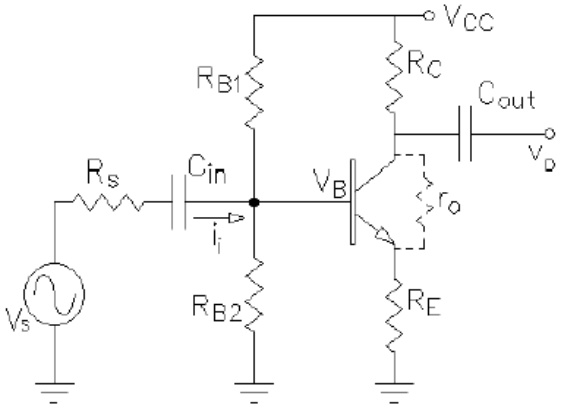
You could think of the ouput as simply 0.7V DC less than the input, which doesn't make the AC signal any less. Of course this doesn't account for the r_e effects.

Current gain: $A_i = \frac{i_o}{i_i} = \frac{R_E \| R_L}{r_e + R_E \| R_L} \cdot \frac{R_i}{R_L} = A_v \cdot \frac{R_i}{R_L} \simeq \frac{R_i}{R_L}$

Common emitter (CE)

Now let's add a resistor in the collector (R_C). Nearly the same current that flows through R_E flows through R_C.



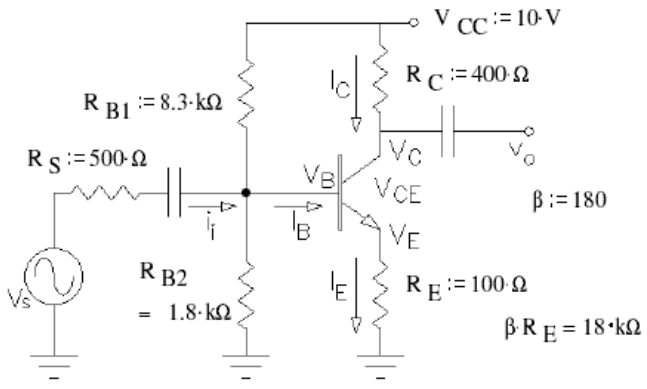


$v_c = -i_c \cdot R_C \qquad v_e = i_e \cdot R_E \simeq v_b$

$i_c \simeq i_e$ so: $\frac{v_c}{v_b} \simeq -\frac{R_C}{R_E}$ gain

Common emitter (CE)

Common Emitter amplifier, example:



Bias:

$$V_{BB} := \frac{R_{B2}}{R_{B2}+R_{B1}} \cdot V_{CC} \qquad V_{BB} = 1.782 \cdot V$$

$$R_{BB} := \frac{1}{\left(\frac{1}{R_{B2}} + \frac{1}{R_{B1}}\right)} \qquad R_{BB} = 1.479 \cdot k\Omega$$

$$I_B := \frac{V_{BB} - 0.7 \cdot V}{R_{BB} + \beta \cdot R_E} \qquad I_B = 0.056 \cdot mA$$

$$I_E := \frac{V_E}{R_E} \qquad I_C := I_E \qquad I_C = 10 \cdot mA$$

$$V_E := I_B \cdot (\beta \cdot R_E) \qquad V_E = 1 \cdot V$$

$$V_B := V_E + 0.7 \cdot V \qquad V_B = 1.7 \cdot V$$

$$V_C := V_{CC} - I_C \cdot R_C \qquad V_C = 6 \cdot V$$

What if we put in an AC input signal: $v_B(t) := V_B + 0.5 \cdot V \cdot \cos\left(6280 \cdot \frac{rad}{sec} \cdot t\right)$ $\qquad v_E(t) := v_B(t) - 0.7 \cdot V$

$$i_C(t) := \frac{v_E(t)}{R_E} \qquad v_C(t) := V_{CC} - i_C(t) \cdot R_C$$

$$\frac{R_C}{R_E} = \frac{400 \cdot \Omega}{100 \cdot \Omega} = 4$$

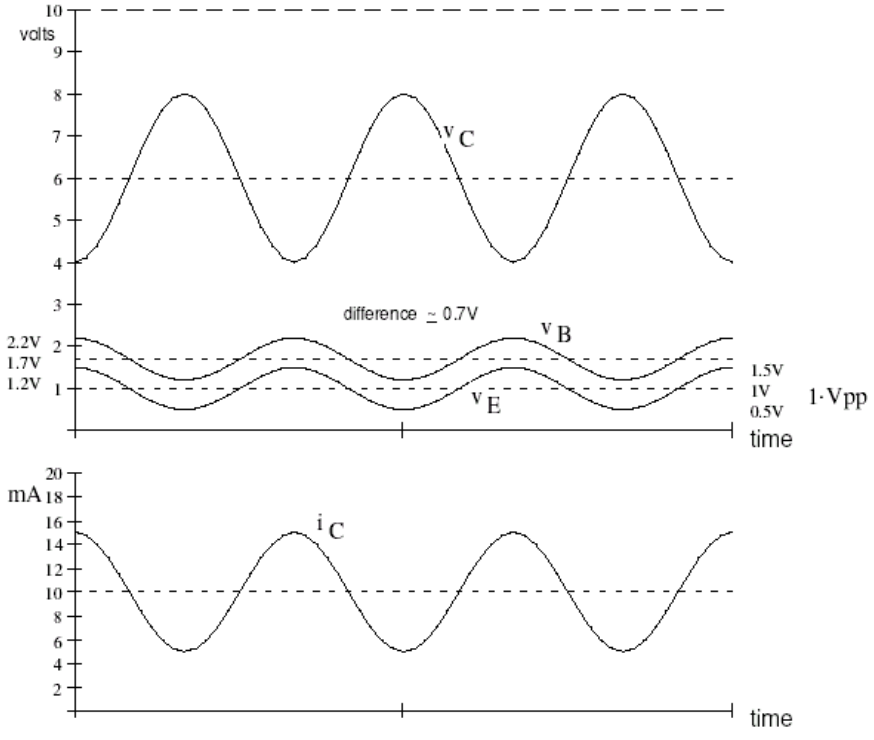
v_C is 4 times bigger and inverted

Actually, to be more correct, we should account for the small-signal resistance of the base-emitter junction.

$$r_e := \frac{V_T}{I_C} \qquad r_e = 2.5 \cdot \Omega$$

gain is really:

$$\frac{R_C}{R_E + r_e} = 3.902$$



Input impedance: $R_i = R_{B1} \| R_{B2} \| \beta \cdot (r_e + R_E)$

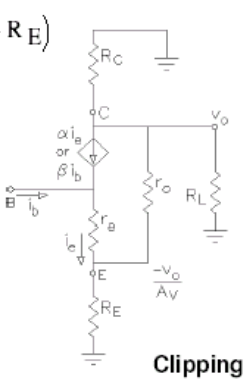
Output impedance: $R_o = R_C \| r_o$

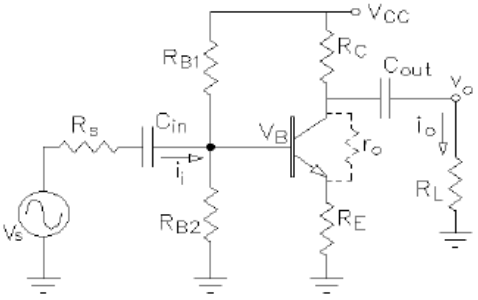
Often neglected $r_o = \dfrac{V_A}{I_C}$ Early voltage. (guess $V_A \simeq 100$ V if no data)

AC collector resistance: $r_c = R_C \| R_L \| r_o$

More correct, use: $r_o \cdot \dfrac{A_v}{A_v + 1}$

instead of r_o very rarely done.

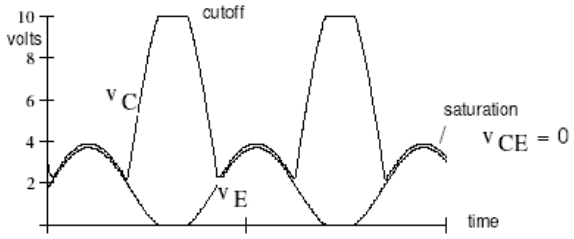




Voltage gain: $A_v = \dfrac{v_o}{v_b} = \dfrac{r_c}{r_e + R_E}$

Current gain: $A_i = \dfrac{i_o}{i_i} = \dfrac{r_c}{r_e + R_E} \cdot \dfrac{R_i}{R_L} = A_v \cdot \dfrac{R_i}{R_L}$

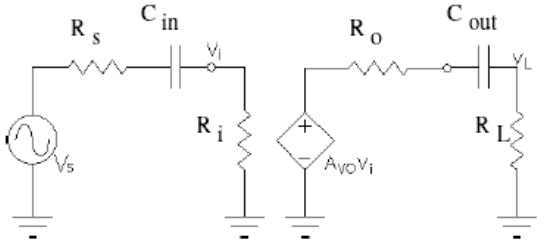
Clipping Cutoff clipping: $i_E = 0$



Low frequency corner frequencies

$$f_{CL1} = \frac{1}{2 \cdot \pi \cdot (R_S + R_i) \cdot C_{in}}$$

$$f_{CL2} = \frac{1}{2 \cdot \pi \cdot (R_L + R_o) \cdot C_{out}}$$



With bypass capacitor (C_E)

This basically makes the R_E dissapear at signal frequencies (If the cap is big enough).

Input impedance: $R_i = R_{B1} \| R_{B2} \| \beta \cdot r_e$ Much lower

Output impedance: $R_o = R_C \| r_o$ Same as above, but no r_o correction needed

AC collector resistance: $r_c = R_C \| R_L \| r_o$

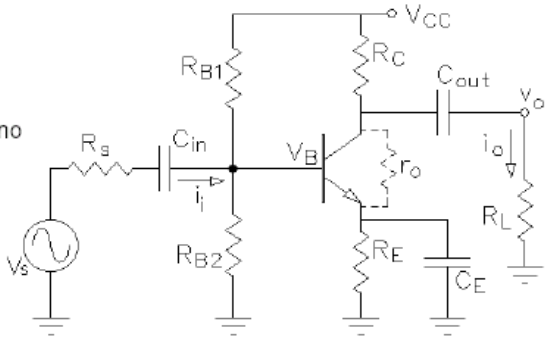
Voltage gain: $A_v = \dfrac{v_o}{v_b} = \dfrac{r_c}{r_e}$

Current gain: $A_i = A_v \cdot \dfrac{R_i}{R_L}$

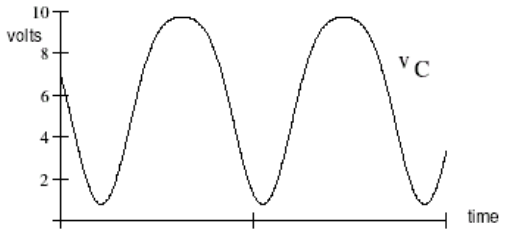
Another low frequency corner frequency:

$$f_{CL3} = \frac{1}{2 \cdot \pi \cdot C_E} \cdot \left(\frac{1}{r_e} + \frac{1}{R_E} \right)$$

Because r_e is so small, this will usually dominate, even when C_E is big.



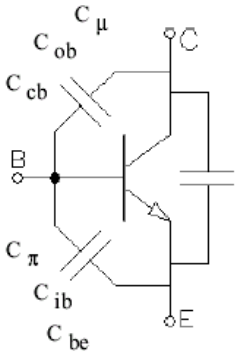
If the output swing is too big you'll get distortion because r_e varies with i_C



High-frequency response

In general, capacitors that are placed in the circuit intentionally, those you can see, cause low-frequency poles. The unseen capacitors inside the parts and between the leads and the board traces cause high-frequency poles. These unseen capacitors have many names, Your textbook uses C_μ and C_π

This capacitance causes the most trouble in common-emitter amplifiers because of it's location. It is connected between the input an the output, so it's effects are multiplied by the voltage gain. (The miller effect.)

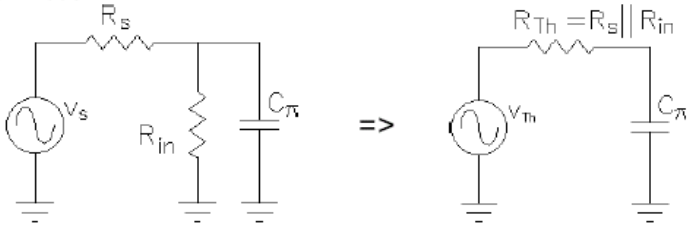


This cacacitance is usually small and unimportant.

This capacitance varies with the base current so much that it is not even specified on data sheets. f_T is given instead. f_T is the frequency where so much current flows through C_π that the effective β is reduced to 1.

$$f_T = \frac{1}{2\cdot\pi\cdot\left(C_\pi + C_\mu\right)\cdot r_e} \quad = \text{freq. where } \beta \sim 1$$

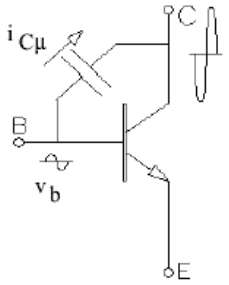
Input circuit model



$$f_{CH1} = \frac{1}{2\cdot\pi\cdot C_\pi}\cdot\left(\frac{1}{R_s}+\frac{1}{R_{in}}\right)$$

Miller Effect

In a common-emitter amplifier:



$$v_c = -\left|A_v\right|\cdot v_b$$

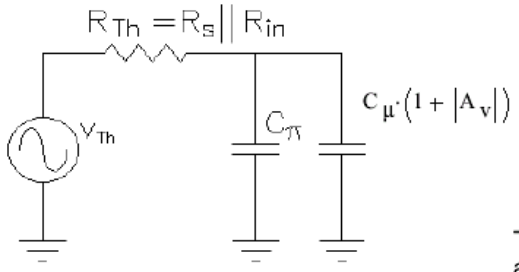
$$i_{C\mu} = \frac{v_b - v_c}{\left(\frac{1}{j\cdot\omega\cdot C_\mu}\right)} = \left[v_b - \left(-\left|A_v\right|\cdot v_b\right)\right]\cdot\left(j\cdot\omega\cdot C_\mu\right)$$

$$= v_b\cdot\left(1+\left|A_v\right|\right)\cdot\left(j\cdot\omega\cdot C_\mu\right)$$

$$= v_b\cdot j\cdot\omega\cdot C_\mu\cdot\left(1+\left|A_v\right|\right)$$

If you wanted to make an equivalent amount of current flow to ground, you'd need a capacitor that was $(1+A_v)$ times as big. This is the Miller effect.

Input circuit model



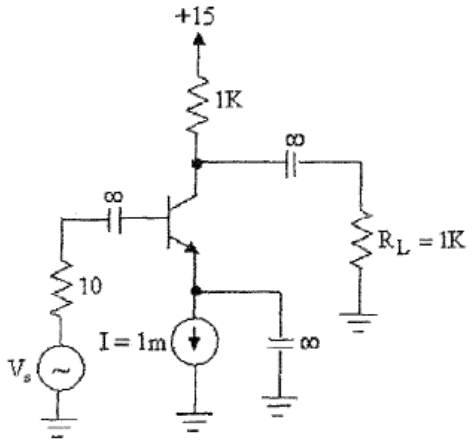
$$f_{CH} = \frac{1}{2\cdot\pi\cdot\left[C_\pi + C_\mu\cdot\left(1+\left|A_v\right|\right)\right]}\cdot\left(\frac{1}{R_s}+\frac{1}{R_{in}}\right)$$

The Miller effect will amplify any capacitance between the base and the collector, not just the capacitance within the transistor, so place leads and circuit traces carefully. If you're modeling a circuit in SPICE you'll have to model these "stray" capacitances if you want your high-frequency results to be any good.

Example:

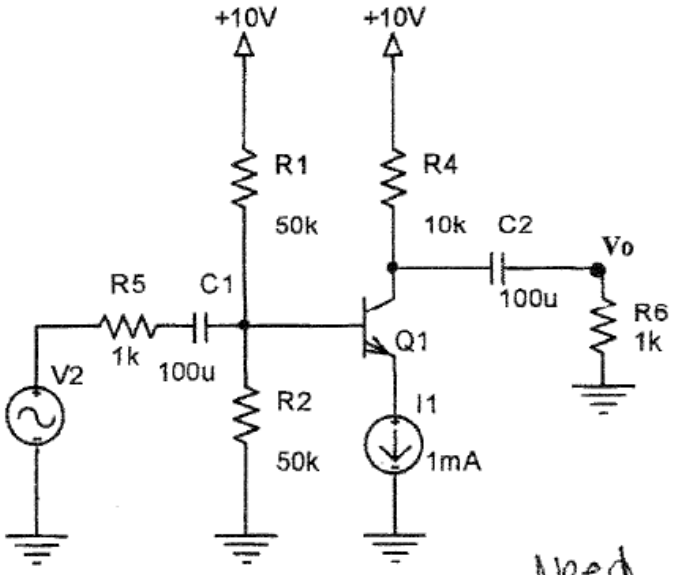
Use $|V_{BE}|=0.7$, $\beta=100$, $V_T=25mV$ (Vs is an ac source), ignore r_o.

Will this circuit work as an amplifier? Why or why not?



Example:

V2 = 0.1m sin(ωt) and β can vary from 20 to 200. The circuit shown below is suppose to amplify but does not. You expect the output at Vo to amplify V2. When you are testing the circuit, you find that it does not amplify. Explain why it does not and what exact resistor can be changed to allow it to amplify. I1 is not an ideal current source and can have a voltage drop across it.



$V_B = 5V$

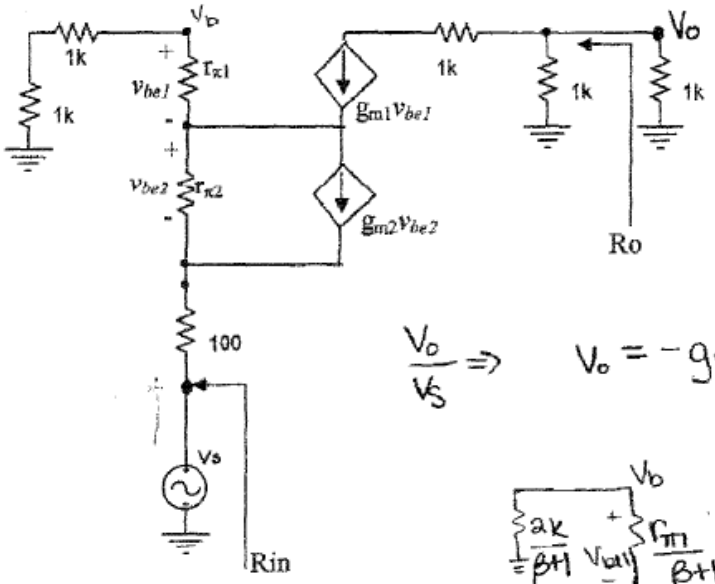
$V_c \approx 0V$

$V_c < V_B$

Not in active region. Therefore, it will not amplify.

Need to decrease R_4 so that $V_c > V_B > V_E$

Example



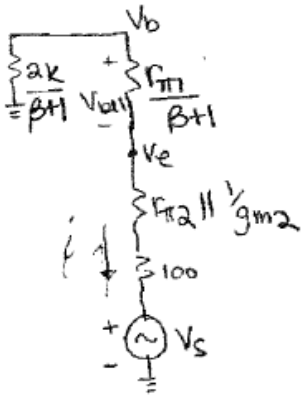
$r_{\pi 1} = 10K$

$r_{\pi 2} = 20K$

$g_{m1} = 2m$

$g_{m2} = 1m$

$\frac{V_o}{V_s} \Rightarrow \quad V_o = -g_{m1} V_{be1} (1k \| 1k)$



$i = \frac{-V_s}{R_{in}} = 616\mu \cdot V_s$

$V_{be} = +i \frac{r_{\pi 1}}{\beta+1} = -0.29 V_s$

$V_{be} = \frac{-r_\pi}{\beta+1} \cdot \frac{V_s}{R_{in}}$

$V_o = -g_{m1} \left(-\frac{r_{\pi 1}}{\beta+1}\right) \frac{V_s}{R_{in}} (500)$

$\frac{V_o}{V_s} = -2m \left(-\frac{10K}{21}\right) \frac{500}{1623} = +0.3 \ V/V$

Using voltage divider:

$$V_e = \frac{\left(\frac{r_{\pi 1}}{\beta+1} + \frac{2K}{\beta+1}\right) V_s}{\frac{(r_{\pi 1} + 2K)}{\beta+1} + r_{\pi 2} \| \frac{1}{g_{m2}} + 100} = 0.35 V_s$$

$$V_b = \frac{\frac{2K}{\beta+1} \cdot V_e}{\frac{r_{\pi 1}}{\beta+1} + \frac{2K}{\beta+1}} = .166 V_e = 0.058 V_s$$

$V_{be} = V_b - V_e = -.29 V_s$

5

Example:

Use $|V_{BE}|$=0.7, β=20, V_T=25mV (Vs is an ac source), ignore r_o.

This small-signal model circuit is drawn below. The original circuit is also shown below. It was found through a DC analysis that I_{C1}=50μ and I_{C2}=25μ.

(a) Find the ac parameters

a. $r_{\pi 1}$ **(3 points)**= $\frac{\beta}{g_{m1}} = \frac{20}{2m} =$ 10K

b. $r_{\pi 2}$ **(3 points)**= $\beta/g_{m2} = 20/1m =$ 20K

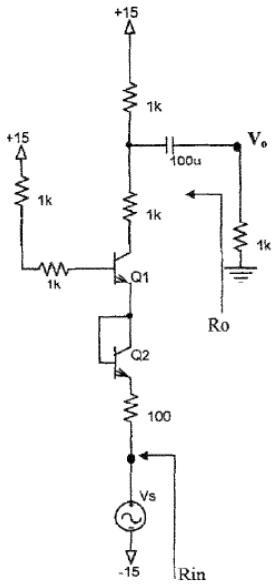
c. gm_1 **(3 points)**= $I_{C1}/V_T = 50\mu/25m =$ 2m

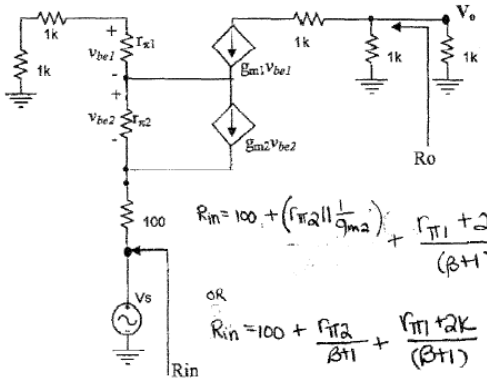
d. gm_2 **(3 points)**= $I_{C2}/V_T = 25\mu/25m =$ 1m

(b) Find that input resistance, R_{in}. (Ignore the AC input source Vs, include the 100 ohm) **(12 points)**

(c) Find the output resistance, R_o. (Ignore the load resistor of 1k to the right of arrow) **(6 points)**

(d) Find the overall gain, Vo/Vs **(25 points)**





$R_{in} = 100 + \left(r_{\pi 2} \| \frac{1}{g_{m2}}\right) + \frac{r_{\pi 1} + 2K}{(\beta+1)}$

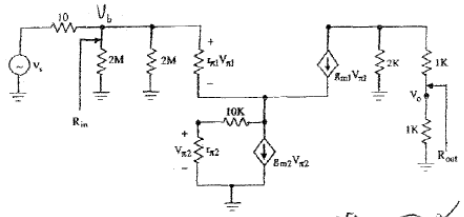
OR

$R_{in} = 100 + \frac{r_{\pi 2}}{\beta+1} + \frac{r_{\pi 1} + 2K}{(\beta+1)}$

$R_{in} = 100 + 952 + 571 =$ 1623Ω

$R_o =$ 1K ⇒ $g_m v_{be1}$ becomes open so that the 1K tied to it is floating

Example:



$I_{E1} = 2.525m$

$I_{E2} = 1.2625M$

$I_{\pi 1}$

$r_{\pi 2}$

g_{m1}

g_{m2}

a) $I_{B1} = \frac{I_{E1}}{\beta+1} = 25\mu$ $\quad r_{\pi 1} = \frac{25m}{I_{B1}} =$ (1kΩ) ✓ $\quad g_{m1} = \frac{\beta}{r_{\pi 1}} =$ (100mA/V) ✓

$I_{B2} = \frac{I_{E2}}{\beta+1} = 12.5\mu$ $\quad r_{\pi 2} = \frac{25m}{I_{B2}} =$ (2KΩ) ✓ $\quad g_{m2} = \frac{1}{r_{\pi 2}} =$ (50mA/V) ✓

b) $R_{in} = 2M \| 2M \| \left[r_{\pi 1} + (\beta+1)(10K + r_{\pi 2})\right]$

$= 1M \| 1.213M$

$=$ (548KΩ) ✓

c) $R_{out} = 1K + 2K =$ (3KΩ) ✓

d) $V_o = \frac{-g_{m1} V_{\pi 1}}{2} \cdot 1K$ ✓

$V_b = V_s \cdot \frac{R_{in}}{10 + R_{in}}$

$\cong V_s$ ✓

$V_{\pi 1} = V_b \cdot \frac{r_{\pi 1}}{r_{\pi 1} + (10K + r_{\pi 2})(\beta+1)} = V_s \cdot 824.4\mu$

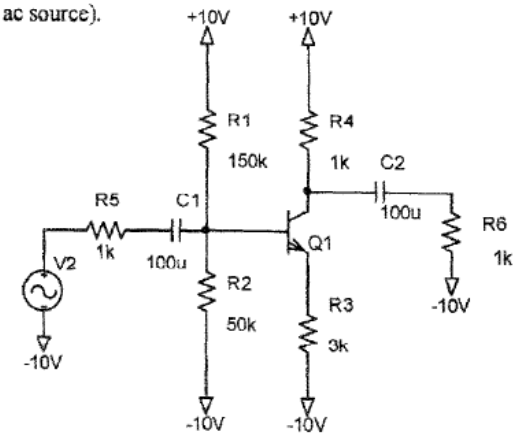
$\frac{V_o}{V_s} = \frac{-g_{m1} 824.4\mu \cdot 1K}{2}$

$=$ (−41.2mV/V) ✓

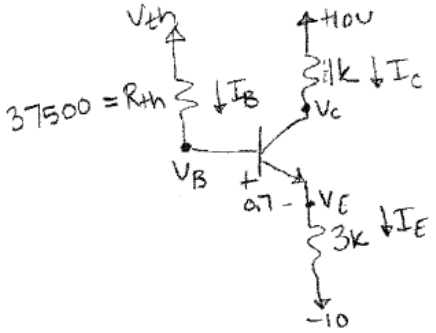
Example:

Use $|V_{BE}|$=0.7, β=100, V_T=25mV (V2 is an ac source).

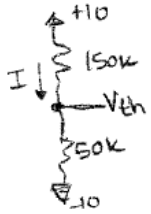
- Find the DC values for the following
  a. I_{E1} **(15 points)**
  b. I_{C1} **(3 points)**
  c. V_{B1} **(6 points)**
  d. V_{C1} **(6 points)**
  e. V_{B1} **(5 points)**



Thevenin of R_1 and R_2:



V_{th} ⇒ (Thevenin is calculated by finding open-circuit voltage)



$I = \frac{20}{150k+50k} = \frac{20}{200k}$

$I = 100\mu$

$-V_{th} + I(50k) - 10 = 0$

$V_{th} = 100\mu(50k) - 10$

$V_{th} = -5V$

$-V_{th} + I_B(37500) + 0.7 + I_E(3k) - 10 = 0$

$I_B = \frac{I_E}{\beta+1}$

R_{th} ⇒ (short sources and find resistive network) ⇒ 150k||50k

$I_E = 1.3mA$ $\quad V_E = I_E(3k) - 10 = -6.1$

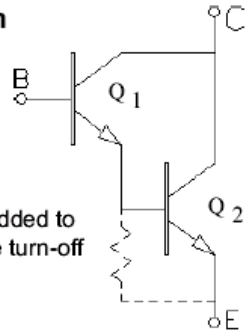
$I_C = \alpha I_E = 1.26m$ $\quad V_B = V_{th} - I_B(R_{th}) = -5.4$

$I_B = 12.9\mu$ $\quad V_C = 10 - I_C(1k) = 8.74$

$V_C > V_B > V_E$

Special multiple-transistor connections,
often wired together in a single package

Darlington



R is often added to improve the turn-off speed.

For the pair taken together:

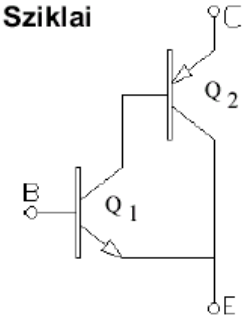
$V_{BE} = 1.4 \cdot V$

$\beta = \beta_1 \cdot \beta_2$

Saturation:

$V_{CE} = 0.9 \cdot V$

Sziklai



For the pair taken together:

$V_{BE} = 0.7 \cdot V$

$\beta = \beta_1 \cdot \beta_2$

Saturation:

$V_{CE} = 0.9 \cdot V$