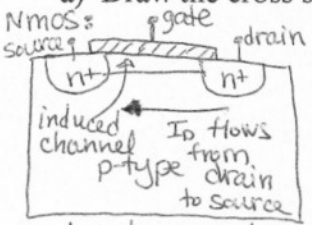
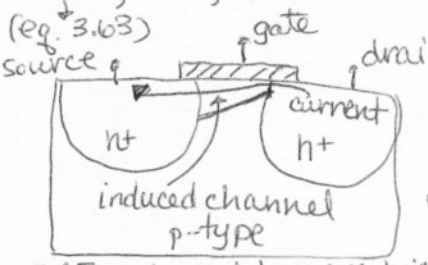
1. Referring to a forward biased pn junction diode, determine the following:
   a) For p-type and n-type material, state the majority and minority carriers (holes or electrons).
   p-type: majority = holes, minority = e^- / n-type: majority = e^-, minority = holes
   b) Explain what happens as the temperature changes (increase and decreases) to the number of MAJORITY carriers in this p-type and n-type material? T ↑↓: p-type holes No change $p_{po} = N_A$, n-type e^- $n_{no} = N_D$
   c) Explain what happens as the temperature changes (increase and decreases) to the number of MINORITY carriers in this p-type and n-type material? T ↑, p-type e^- ($n_{po} = n_i^2/N_A$) ↑, T ↓ both ↓, n-type holes ($p_{no} = n_i^2/N_D$) ↑, n_i depends on I (eq. 3.36)
   d) Explain in your own words, how the diffusion current, I_D, is created.
   • when p-n junction is forward biased, depletion region becomes smaller and e^- from n-type are injected into p-type which creates current flow I_D.
   e) Explain what happens as the temperature changes (increase and decreases) to the diffusion current, I_D?
   T ↑ ⇒ I_S ↑ (eq. 3.64) which causes I_D ↑, T ↓, I_D ↓ (same reason)

2. a) Draw the cross section of a mosfet.

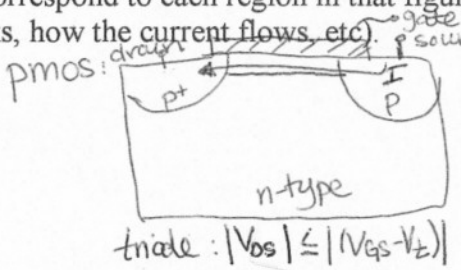


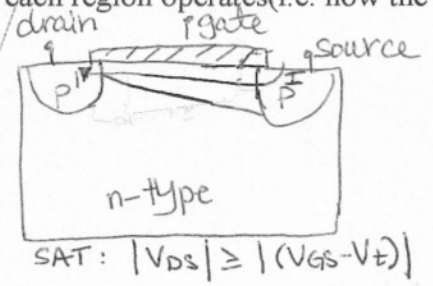


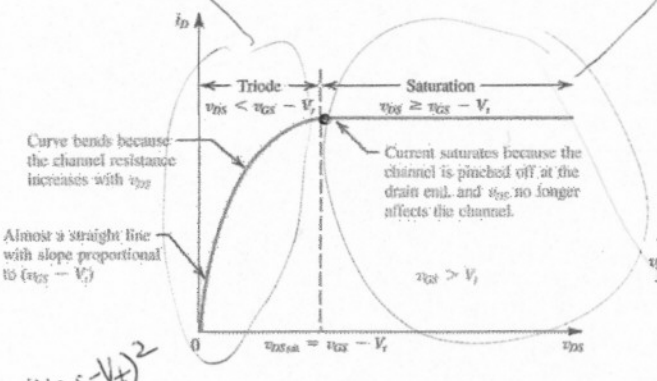
$V_{DS} \leq (V_{GS} - V_t)$ triode ⇒ rectangular shaped channel

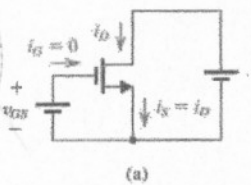
SAT ⇒ channel becomes triangular shaped and then pinched off

   b) Explain in your own words and drawings as needed how, when (under what conditions), and in what direction the current flows in the mosfet. $V_{GS} \geq V_t$ for I to flow ⇒ NMOS I flows D to S. PMOS I flows S to D.
   c) Explain in your own words all the different regions for Fig. 4.6 by drawing cross-sections of the mosfet to correspond to each region in that figure and explaining how each region operates (i.e. how the channel looks, how the current flows, etc).









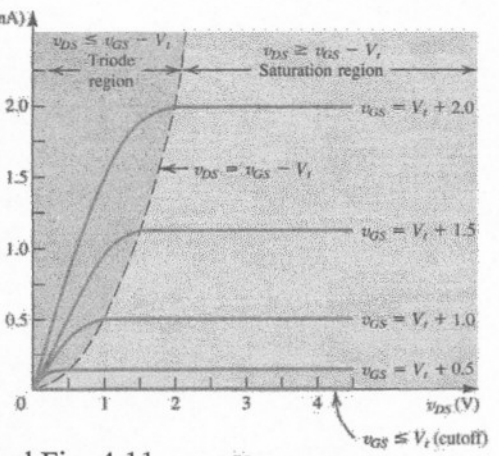
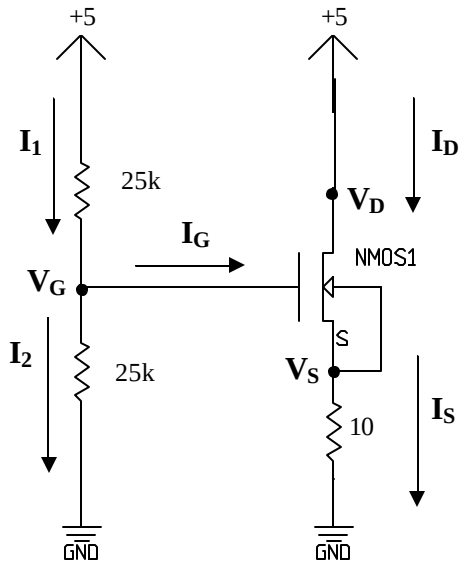


Fig 4.6 Fig. 4.11

$i_D = \frac{1}{2} k_n' \left(\frac{W}{L}\right)(V_{GS} - V_t)^2$ SAT

   d) Explain in your own words what the difference between Fig. 4.6 and Fig. 4.11.
   e) What equation and region of operation is graphed in Fig. 4.12. one V_{GS} curve multiple V_{GS} curves
   f) Explain in your own words how the PMOS differs from the NMOS transistor.
   pmos: I flows source to drain
   same eq. as nmos just take absolute values for comparisons. V_t is negative

3. Analyze the circuit shown below to determine the voltages (V_D, V_G, V_S) at all nodes and the currents through all branches (5 currents). Let V_t=1.5V and $k_n'(W/L)$=2A/V^2. Neglect the channel length modulation effect (i.e. λ=0).



$I_1 = \frac{5}{50K} = 100\mu A$

$I_G = 0A$

$V_G = \frac{5(25k)}{50k} = 2.5V$

$I_D = I_S = \frac{1}{2}k_n'\left(\frac{W}{L}\right)(V_{GS}-V_t)^2$

$V_{GS} = V_G - V_S = 2.5 - 10(I_D)$

$I_D = \frac{1}{2}(2)(2.5-10(I_D)-1.5)^2 = (1-10I_D)^2 = 1-20I_D+100I_D^2$

$0 = 1-21I_D+100I_D^2$

$I_D = \frac{21 \pm \sqrt{21^2-4(100)}}{200} = 0.137 \text{ or } 0.073$

$I_D = 0.137$:

$V_{GS} = V_S$ 2.5 − 1.37 = 1.13 < V_t (would be off)

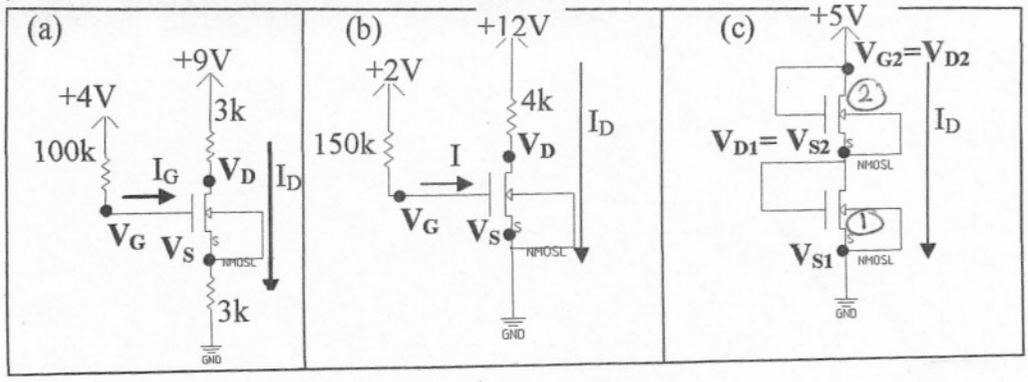
$\therefore I_D = 0.073A \Rightarrow V_S = 0.73V$

$V_D = 5V$

SATURATION conditions satisfied ⇒

$V_{DS} \geq V_{GS} - V_t$

4. Solve the circuits below to find V_G, V_D, and V_S. Find the currents in all branches. Assume $\lambda=0$ and $k_n'(W/L)=1mA/V^2$.



a. Assume sat ⇒

$I_G=0$

$V_G=+4V$ $V_S=I_D(3k)$

$I_D=\frac{1}{2}(1m)(4-I_D(3k)-1)^2$

$2KI_D=(3^2-18KI_D+I_D^2(9K^2))$

$\therefore I_D^2(9K^2)-20KI_D+9=0$

$I_D=\frac{+20K\pm\sqrt{400M-324M}}{2(9K^2)}$

$I_D=\frac{20K\pm 8.7K}{18M}\cong 1.6m, 628\mu$

$I_D=1.6m \Rightarrow V_S=4.8V$

$V_{GS}=4-4.8=-0.8V<V_t$ ✗ off

$I_D=628\mu \Rightarrow V_S=1.884$

$V_{GS}=2.116>V_t$ ∴ ON

$+9-I_D(3k)=V_D$

$V_D=7.116V$

$V_{DS}\geq(V_{GS}-V_t)$ ✓ SAT

b. Assume Sat ⇒

$I=0$, $V_G=+2V$

$V_{GS}=+2V>V_t$ ON

$I_D=\frac{1}{2}k_n'(\frac{W}{L})(V_{GS}-V_t)^2$

$I_D=\frac{1}{2}(1m)(+2-1)^2$

$I_D=500\mu A$

$V_D=+12-4k\cdot I_D$

$V_D=+10V$

$V_{DS}\geq(V_{GS}-V_t)$ ✓ SAT

$V_S=0V$

c. $V_{G2}=V_{D2}=+5V$

$V_{S1}=0V$

$I_D=\frac{1}{2}k_n'(\frac{W}{L})(+5-V_{S2}-1)^2$

For ②

$I_D=\frac{1}{2}k_n'(\frac{W}{L})(V_{S2}-1)^2$

From ①

$\frac{1}{2}k_n'(\frac{W}{L})(4-V_{S2})^2=\frac{1}{2}k_n'(\frac{W}{L})(V_{S2}-1)^2$

$(4-V_{S2})=(V_{S2}-1)$

$4+1=V_{S2}+V_{S2}$

$V_{S2}=\frac{+5}{2}$

Use ② or ①

② $I_D=\frac{1}{2}(1m)(5-\frac{5}{2}-1)^2=1.125mA$

① $I_D=\frac{1}{2}(1m)(\frac{5}{2}-1)^2=1.125mA$

5. Use: V_t=2V, K_n'(W/L)=50μA/V^2, λ=0

$V_I = 5+0.001\sin(10t)$

Assume all capacitors are open for DC analysis and shorted for AC analysis

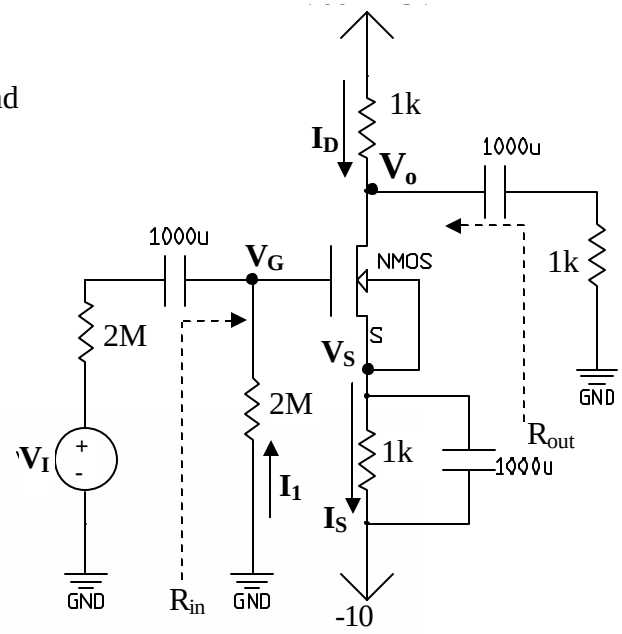
(a) Solve for the DC currents: I_1, I_D, and I_S

(b) Solve for the DC voltages: V_G, V_S, and V_o

(c) State the operating point, bias point, or quiescent point for this amplifier

(d) Draw the small-signal equivalent circuit

(e) Analyze the small-signal circuit for V_o/V_I.



a. $I_1 = 0$ $\quad I_D = I_S$

$I_D = \frac{1}{2}(50\mu)(V_{GS}-V_t)^2$

$V_{GS} = V_G - V_S$

$V_G = 0$

$V_S = I_D(1k) - 10$

$\therefore I_D = \frac{1}{2}(50\mu)(0 - I_D(1k) + 10 - 2)^2$

$I_D(40k) = (I_D^2(1k)^2 + 64 - 16(1k)I_D)$

$I_D = \frac{56k \pm \sqrt{(56k)^2 - 4(1k)^2(64)}}{2(1k)^2} = 1.2m,\ 54.8m$ → Gives $V_{GS} \cong -45$

$V_S = -8.8V$

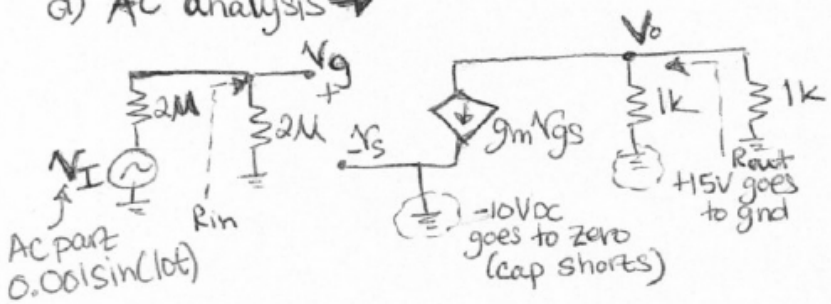
d) $V_{GS} = 8.8V$ which gives $\Rightarrow I_D = 1.2m$

$V_D = V_o = 15 - I_D(1k) = 13.8V$

$\therefore V_{DS} = 22.6 > (V_{GS}-V_t) = 6.8V$

$\therefore$ bias point (operating point, or q point) is the voltage, V_{GS}.

d) AC analysis →



$V_g = \frac{V_I(2M)}{4M} = \frac{1}{2}V_I$

$V_s = 0$ $\quad \therefore V_{gs} = \frac{1}{2}V_I$

$V_o = -g_m V_{gs}(\frac{1}{2}1k)$ DC value

$g_m = K_n'(\frac{W}{L})(V_{GS}-V_t) = 50\mu(8.8-2)$

$g_m = 340\mu A/V$

$\therefore V_o = -340\mu(\frac{1}{2}V_I)(500)$

$\frac{V_o}{V_I} = -85m$

Note: $R_{in} = 2M$

R_{out} (ignore load 1kΩ) = 1k

6. For the following hybrid-π equivalent circuit, find the following values:

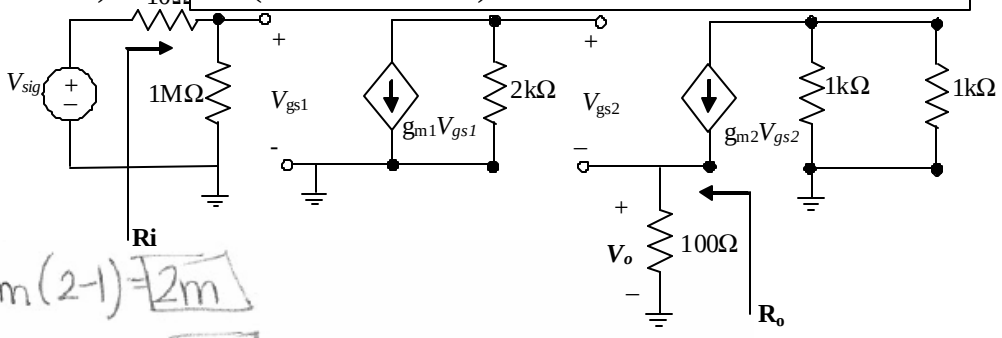
(a) R_i (input resistance –ignore the 10Ω and Vsig)

(b) Ro (output resistance-ignore the 1k load)

(c) gain, $\frac{Vo}{Vsig}$

(d) Draw the transistor schematic of this circuit

Use: V_t=1V, K_n'(W/L)=2mA/V^2, V_{sig} is an AC source
Transistor 1 has DC values: VGS1=2V, ID1=1mA
Transistor 2 has DC values: VGS2=3V, ID2=4mA
λ=0 (for all transistors)



$g_{m1} = \sqrt{2(2m)1m} = 2m(2-1) = \boxed{2m}$

$g_{m2} = \sqrt{2(2m)4m} = 2m(3-1) = \boxed{4m}$

a) $\boxed{R_i = 1M}$

b) $R_o = 100\Omega \,||\, \frac{1}{g_{m2}} = 100 \,||\, 250 \cong \boxed{71\Omega}$

c) $V_o = +g_{m2} V_{gs2} (100)$

$V_{gs2} = V_{g2} - V_o = -g_{m1} V_{gs1} (2K) - g_{m2} V_{gs2} (100)$

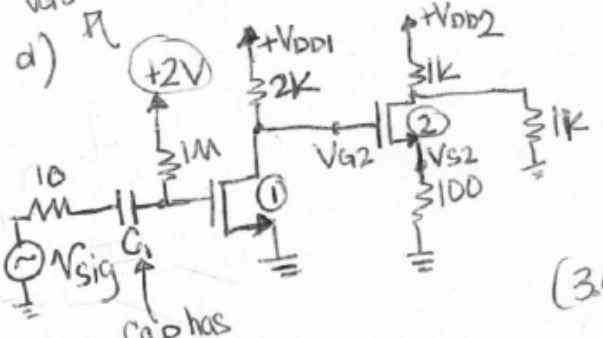
$V_{gs1} = \frac{Vsig(1M)}{1M+10} \approx Vsig$

$V_{gs2} = \frac{-g_{m1}(2K)\, Vsig}{1 + g_{m2}(100)}$

$\frac{V_o}{V_{sig}} = \frac{g_{m2}(100)(-g_{m1})(2K)}{1+g_{m2}(100)} = \boxed{-1.14\,V/V}$

$V_{GS1} = 2V$

a)



$V_{S2} = 4m(100) = 0.4V$

$V_{G2} = V_{GS2} + V_{S2} = 3 + 0.4 = 3.4V$

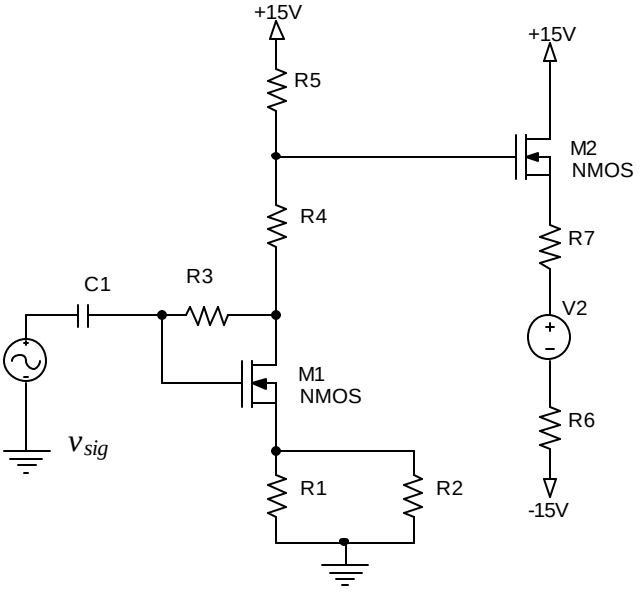
$(3.4V = V_{G2}) = V_{DD1} - 1m(2k)$

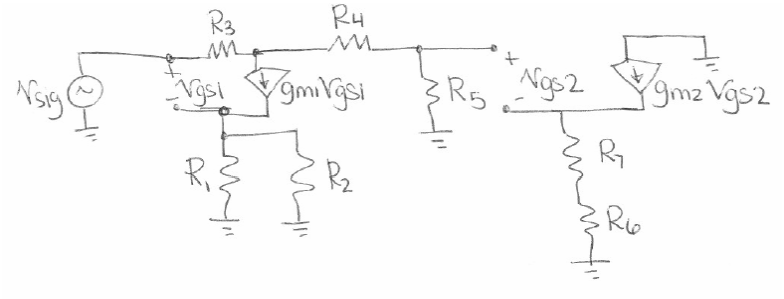
$\therefore V_{DD1} = \boxed{5.4V}$

$V_{DD2} - 4m(1k) \geq (V_{G2} - V_t) = 3.4 - 1 = 2.4V$

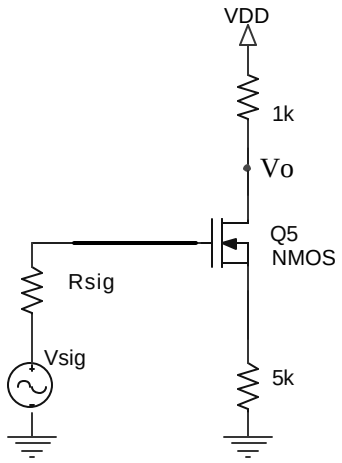
$\therefore \boxed{V_{DD2} \geq 2.4 + 4 = 6.4V}$

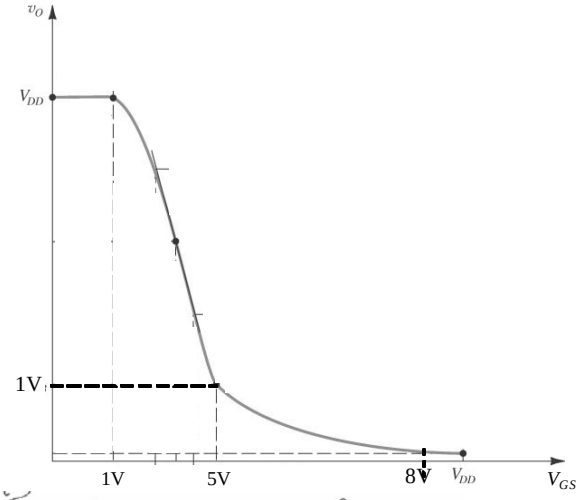
7. For the circuit shown below, **draw** the AC small-signal equivalent circuit(use hybrid-π or model T). Make sure that everything is labeled in terms of the transistor number. (e.g. g_{m1}, v_{gs2}, etc.). λ=0 for all transistors. v_{sig}=0.001sin(10t) AC and V2=10V DC.





8. v_{sig} ={8+0.01sin(ωt)}Volts. Does this circuit operate as a **linear** AC amplifier? If so, what is the gain, $\frac{Vo}{Vsig}$, of the following circuit in terms of VDD, Vsig, Rsig, k'(W/L)? If not, explain why. The graph below shows measurements for this circuit.





This mosfet is biased at a gate voltage of V_G=8V and V_S=0.
∴ V_{GS} = 8V.
It looks like the transistor will be in triode ⇒
$V_{DS} \cong 0 < (V_{GS}-V_t) = 8-1 = 7V$
∴ TRIODE Region → will not amplify linearly