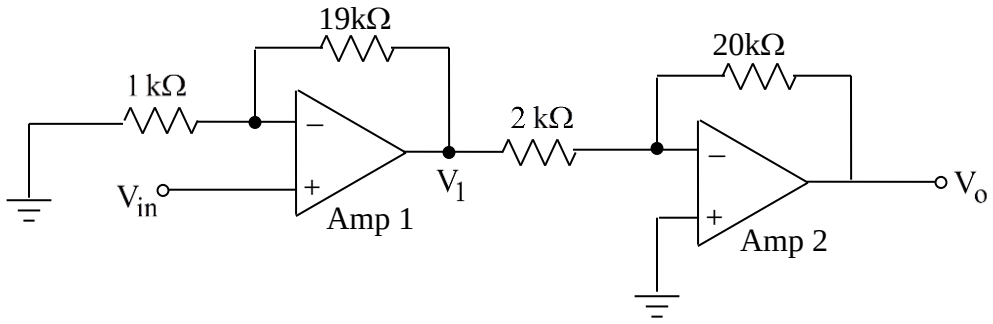
ECE2280 Homework #9 Spring 2014

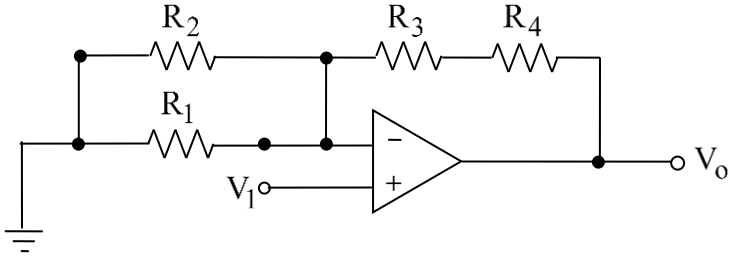
Practice exam example questions:

1. Use the circuit below:



Modify the above circuit to compensate for input bias current on both amplifiers.

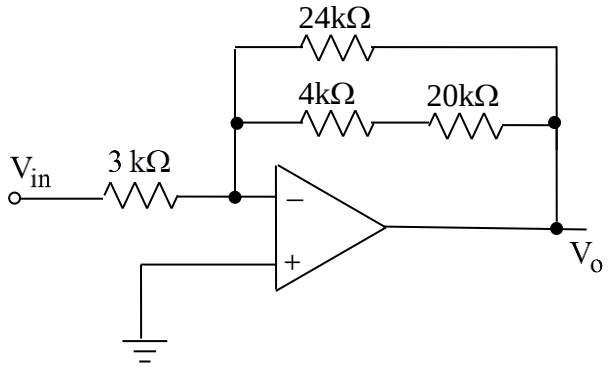
2. Redraw or add to the schematic below to show how to reduce the effect of the **input bias current**. State the symbolic value(s) of any components added to the schematic. State the answer in terms of R_1, R_2, R_3, and R_4.



3. You are given the following characteristics for a real amplifier:

Input offset voltage,	V_{ios}=5mV
Input Resistance,	R_i=1MΩ
Unity-gain bandwidth,	f_T=12MHz
Output swing limits,	within 2Volts of power supply
Slew Rate,	SR=4 $\frac{V}{\mu sec}$

Given the following circuit with the operational amplifier powered at ±12V.



a) Find the ideal gain of the above circuit.
b) For small input signals, what is the bandwidth of the circuit
c) What is the bandwidth when the circuit is operated to produce the maximum possible peak voltage value?

d) For V_{in}=0.001sin($2\pi 90kt$), what is the ideal value for the peak to peak voltage value at the output?

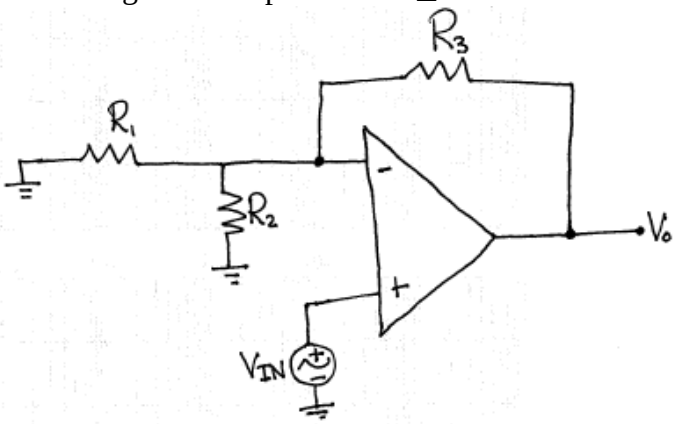
e) For V_{in}=0.002sin($2\pi 90kt$), what is the peak to peak voltage value at the output considering the input offset voltage?

f) How should the circuit above be modified to minimize the effect of the input bias current? Draw the schematic of the modified circuit and state values of added component(s).

4. You are given the following characteristics for a real amplifier:

Input offset voltage,	V_{ios}=4mV
Input Resistance,	R_i=2MΩ
Unity-gain bandwidth,	f_T=10MHz
Output swing limits,	within 2Volts of power supply
Slew Rate,	SR=5 $\frac{V}{\mu sec}$

The following circuit is powered at ±12V:



a) State the equation for Vo. Include no more than V_{IN}, R_1, R_2, and R_3.

b) If R_1= R_2=10k and R_2=100k, what is the bandwidth of the circuit. Consider both the effect due to slew rate (use the maximum output value possible) compared to the effect due to the unity gain bandwidth.

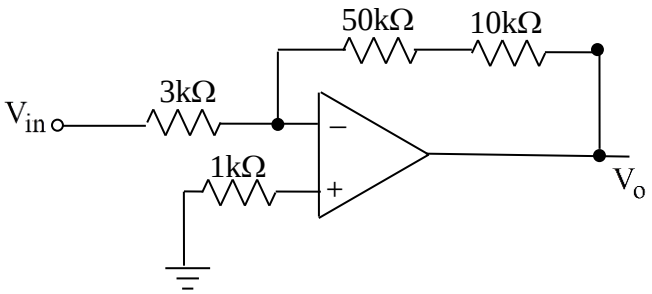
c) For V_{in}=0.001sin($2\pi 90kt$), what is the PEAK(not peak to peak) value at the output considering the input offset voltage?

a) How should the circuit above be modified to minimize the effect of the input bias current? Draw the schematic of the modified circuit and state values of added component(s).

5. You are given the following characteristics for a real amplifier:

Input offset voltage,	V_{ios}=3mV
Input Resistance,	R_i=2MΩ
Unity-gain bandwidth,	f_T=80MHz
Output swing limits,	within 2Volts of power supply
Slew Rate,	SR=3 $\frac{V}{\mu sec}$

The following circuit is powered at ±9V:



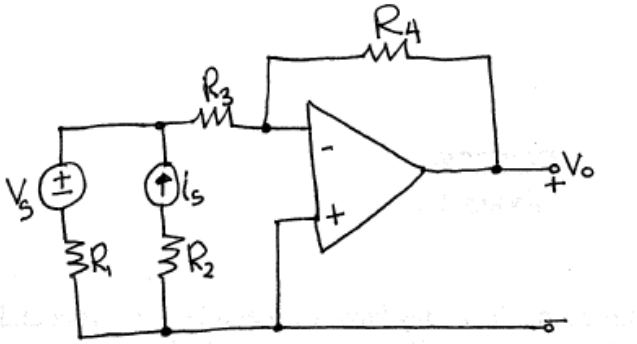
a) What value is the ideal gain?

b) What is the bandwidth of the circuit considering both the Unity-gain bandwidth limitations and the slew rate effect for an input of V_{in}=0.001sin(ωt)?

6. Use the information from problem 5:
a) For V_{in}=0.001sin(ωt), what is the **maximum** and **minimum** values seen at the output considering only the input offset voltage?

b) How should the circuit above be modified(do not remove any resistors) to minimize the effect of the input bias current? Draw the schematic of the modified circuit and state values of added component(s).

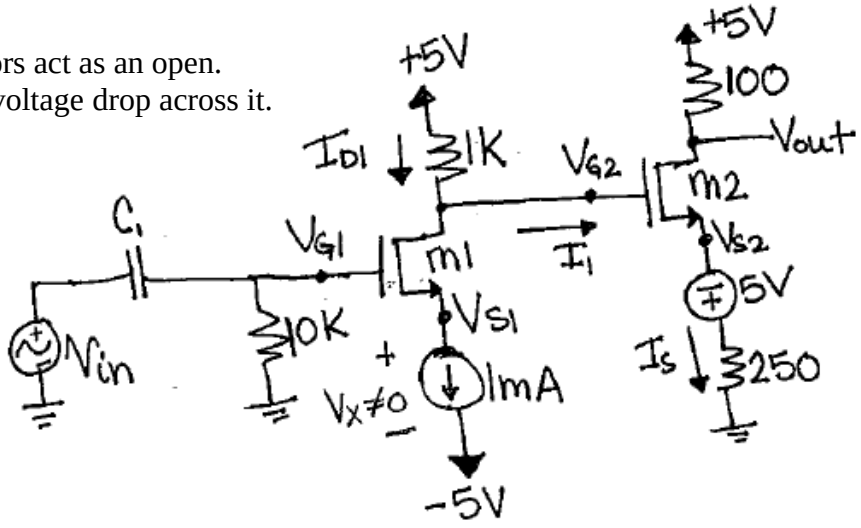
7. Derive an expression for V_o in terms of not more than V_s, i_s, R_1, R_2, R_3, and R_4 of the circuit below by assuming an ideal operational amplifier:



8. **Use: V_t=1V**
k_n'(W/L)=2mA/V^2
λ=0
V_{IN} = (5+100msin(20t))V

For DC analysis, assume that the capacitors act as an open.
The current source is not ideal and has a voltage drop across it.

(a) Solve for the DC currents:
   a. I_1
   b. I_S



(b) Solve for the DC voltages:
   a. V_{G2}
   b. V_{S2}
   c. V_{S1}

(c) Verify that transistor M2 is saturated.

(d) State the DC bias point for transistor M1.

9. Use the information from problem 6. Assuming that the transistor amplification is V_{out}/V_{IN} = +5V/V. Assume the input frequency is operating within the circuits operating range. Assume that the amplification does not pull the transistors out of saturation. Will V_{out} ever be 0.1V? Why or why not?

10. Use: V_t=1V
    $k_n'(W/L)$=2mA/V^2
    V_{sig} is an AC source
    Transistor 1 has DC values: V_{GS}=2V, I_D=1mA
    Transistor 2 has DC values: V_{GS}=2.5V, I_D=2.25mA
    λ=0 (for all transistors) and assume all transistors are saturated

For the following hybrid-π equivalent circuit, find the following values:
(a) R_{in} (input resistance –ignore the input source, Vsig)
(b) ideal overall midband gain, $\frac{V_o}{v_{sig}}$.