

Problem 1 – (40 points)

Solution

Use: $V_t = 1V$

$k_n'(W/L) = 1mA/V^2$

$\lambda = 0$

$V_{IN} = (5 + 10msin(20t))V$

For DC analysis, assume that the capacitors act as an open. The current source is not ideal and has a voltage drop across it.

(a) Solve for the DC currents:

- a. $I_1 = 0$
- b. $I_S = 1.4mA$

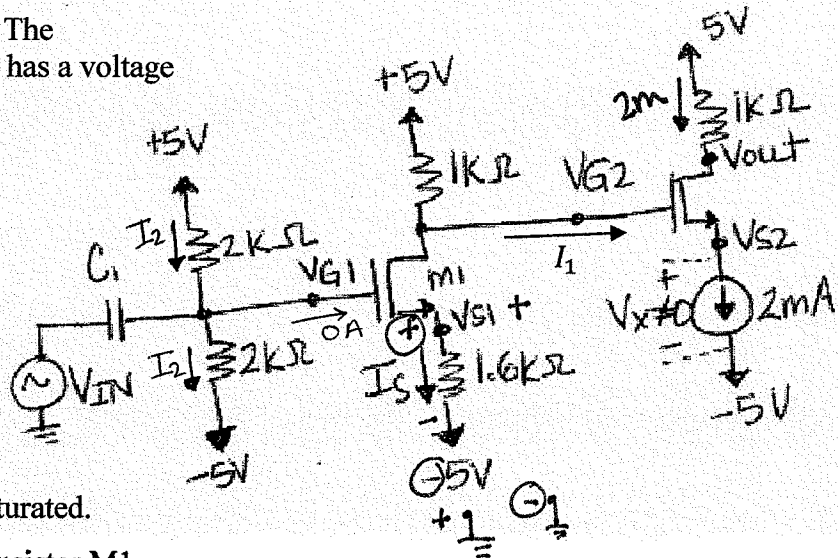
(b) Solve for the DC voltages:

- a. $V_{G2} = 3.6V$
- b. $V_{S2} = 0.6V$
- c. $V_{S1} = -2.7V$

(c) Verify that transistor M2 is saturated.

(d) State the DC bias point for transistor M1.

(e) Assuming that the transistor amplification is $V_{out}/V_{IN} = +5V/V$. Assume the input frequency is operating within the circuits operating range. Assume that the amplification does not pull the transistors out of saturation. Draw a rough sketch of the **total instantaneous value** seen at V_{out} using the V_{IN} value stated above.



a) $I_1 = 0$

b)
$$I_S = \frac{1}{2} k_n' \left(\frac{W}{L}\right) (V_{GS1} - V_t)^2 = \frac{1}{2} (1m) (V_{G1} - V_{S1} - 1)^2$$

$V_{G1} = 0$ OR $+5 - I_2(2k) - I_2(2k) + 5 = 0$

$$I_2 = \frac{10}{4k} = 2.5mA$$

$$-5 + I_2(2k) = V_{G1} = 0$$

$$V_{S1} = -5 + I_S(1.6k)$$

$$\frac{2 I_S}{1m} = (0 + 5 - I_S(1.6k) - 1)^2 = (4 - I_S(1.6k))^2 = 16 - 12800 I_S + I_S^2(1.6k)^2$$

$$0 = I_S^2(1.6k)^2 - 14,800 I_S + 16$$

$$I_S = \frac{14,800 \pm \sqrt{14,800^2 - 4(16)(1.6k)^2}}{2(1.6k)^2} = 4.3mA \text{ and } 1.4mA$$

If $I_s = 4.3\text{mA}$ then $V_{s1} = -5 + I_s(1.6\text{k}) = +1.88$
 $V_{GS1} = 0 - 1.88 = -1.88 < V_t \times \underline{\text{NO}}$

$I_s = 1.4\text{mA}$

$V_{s1} = -5 + (1.4\text{mA})(1.6\text{k}) = -2.7\text{V} = V_{s1}$

$\therefore V_{GS1} = 2.7\text{V} > V_t \therefore \text{ON}$

$V_{D1} = V_{G2} = 5 - 1\text{k}(1.4\text{mA}) = 3.6\text{V} = V_{G2}$

$3.6 = V_{D1} - V_{s1} > V_{G1} - V_{s1} - V_t = 0 - 1 \checkmark \text{ TRUE, SAT}$

$I_{D2} = I_{s2} = 2\text{mA} = \frac{1}{2}(1\text{mA})(3.6 - V_{s2} - 1)^2$

$4 = (2.6 - V_{s2})^2$

$\pm\sqrt{4} = 2.6 - V_{s2}$

$\therefore V_{s2} = 2.6 \pm 2 = 4.6 \text{ OR } 0.6$

If $V_{s2} = 4.6$ then $V_{GS2} = 3.6 - 4.6 = -1 < V_t = 1 \therefore \text{NOT ON!}$

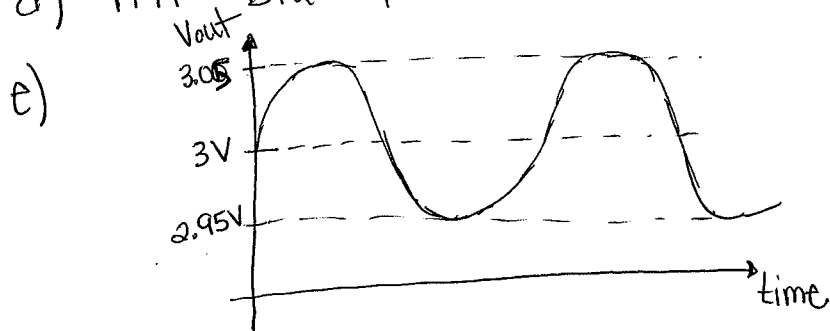
$V_{s2} = 0.6\text{V}$

c) $V_{GS2} = 3.6 - 0.6 = 3\text{V} > V_t = 1 \therefore \underline{\text{ON}}$

$V_{D2} = 5 - 1\text{k}(2\text{mA}) = 3\text{V}$

$3\text{V} = V_{D2} - V_{s2} > V_{G2} - V_{s2} - V_t = 2.6\text{V} \checkmark \underline{\text{SATURATED}}$

d) m1 bias point is $I_D = 1.4\text{mA}$ OR $V_{GS1} = 2.7\text{V}$



$V_{out_total} = V_{out_DC} + V_{out_AC}$

$V_{out_total} = 3 + 5(10\text{ms}\sin(20t))$

Problem 2 – (35 points)

Use: $V_t = 1V$

$k_n' (W/L) = 10mA/V^2$

V_{sig} is an AC source

Transistor 1 has DC values: $V_{GS} = 9V, I_D = 3.2A$

Transistor 2 has DC values: $V_{GS} = 1.18V, I_D = 162\mu A$

$\lambda = 0$ (for all transistors) and assume all transistors are saturated

$$g_{m1} = k_n' \left(\frac{W}{L}\right) (V_{GS1} - V_t) = 10m(9-1)$$

$$g_{m1} = 80m$$

$$\text{OR } g_{m1} = \sqrt{2k_n' \left(\frac{W}{L}\right) I_D} = \sqrt{2(10m)(3.2)}$$

$$g_{m1} = 0.253$$

$$g_{m2} = 10m(1.18-1) = 1.8m$$

$$\text{OR } g_{m2} = \sqrt{2(10m)(162\mu)}$$

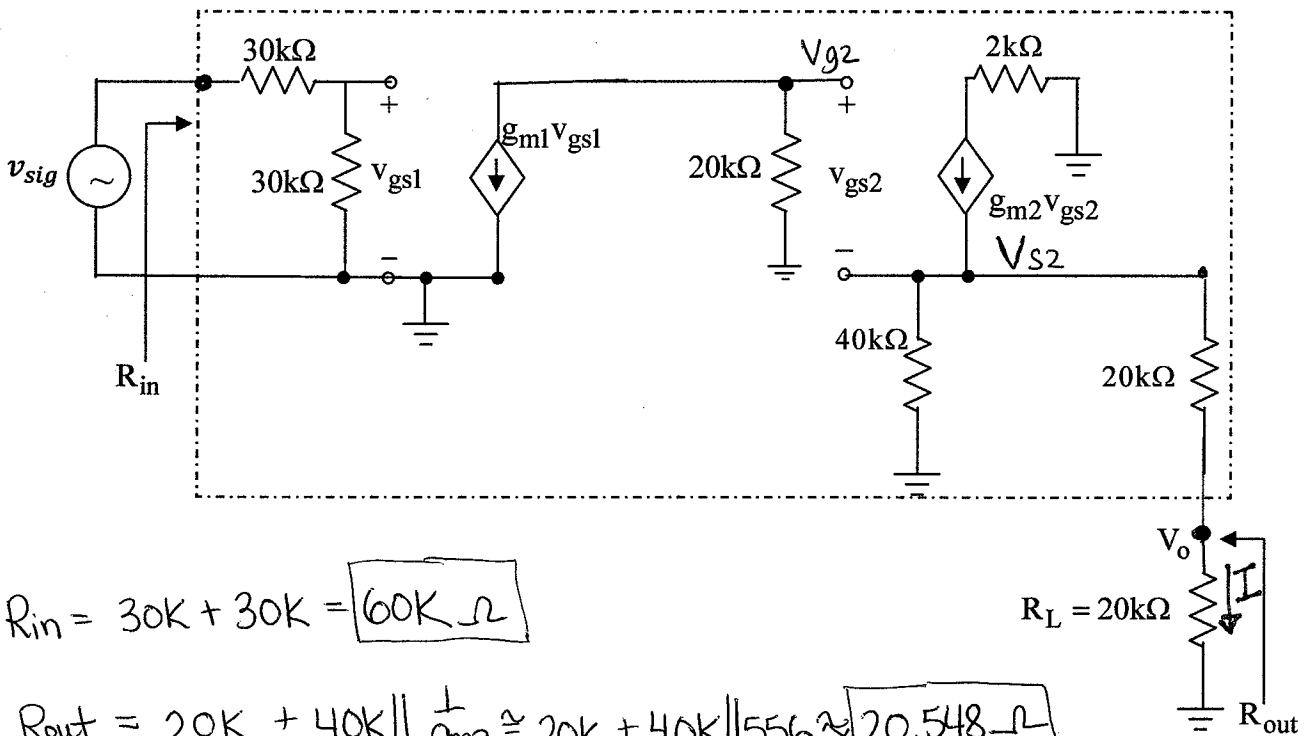
$$g_{m2} = 1.8m$$

For the following hybrid- π equivalent circuit, find the following values:

(a) R_{in} (input resistance – ignore the input source, V_{sig})

(b) R_{out} (output resistance – ignore R_L)

(c) ideal overall midband gain, $\frac{V_o}{v_{sig}}$ (make sure to include R_L).



a) $R_{in} = 30k + 30k = \boxed{60k \Omega}$

b) $R_{out} = 20k + 40k \parallel \frac{1}{g_{m2}} \approx 20k + 40k \parallel 556 \approx \boxed{20,548 \Omega}$

c) $V_o = I \cdot R_L = \underbrace{g_{m2} V_{gs2}}_I \left(\frac{40k}{80k} \right) \cdot 20k = (1.8m) \left(\frac{1}{2} \right) (20k) V_{gs2} = 18 V_{gs2}$

$$V_{gs2} = \underbrace{-g_{m1} V_{gs1} (20k)}_{V_{g2}} - \underbrace{g_{m2} V_{gs2} (40k \parallel 40k)}_{V_{s2}}$$

$$V_{gs2} (1 + g_{m2} (20k)) = -g_{m1} (20k) V_{gs1}$$

$$V_{gs2} = \frac{-g_{m1} (20k) V_{gs1}}{(1 + g_{m2} 20k)}$$

$$V_{gs1} = \frac{1}{2} V_{sig}$$

$$\therefore V_o = 18 \left(\frac{-g_{m1} (20k)}{(1 + g_{m2} 20k)} \right) \cdot \frac{1}{2} V_{sig}$$

For $g_{m1} = 80m \Rightarrow$

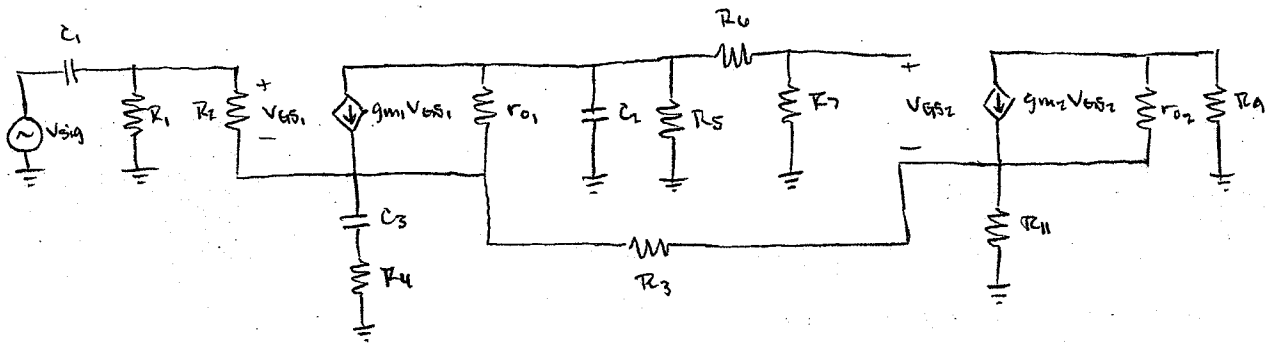
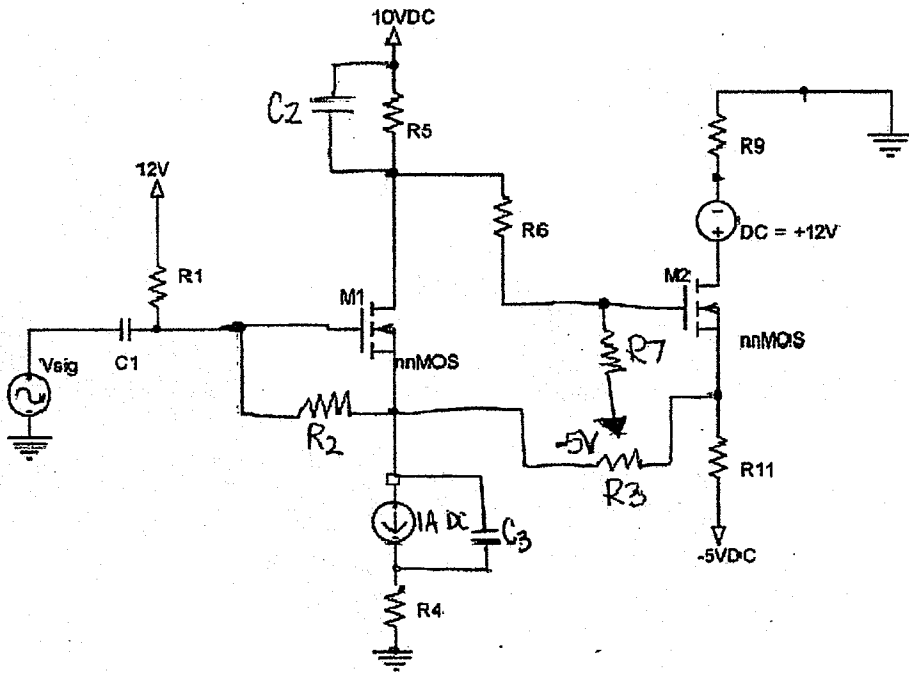
$$\frac{V_o}{V_{sig}} = 18 \left(\frac{-1,600}{37} \right) \frac{1}{2} \approx \boxed{-389 \text{ V/V}}$$

For $g_{m1} = 0.253$

$$\frac{V_o}{V_{sig}} = 18 \left(\frac{-5,060}{37} \right) \frac{1}{2} \approx \boxed{-1231 \text{ V/V}}$$

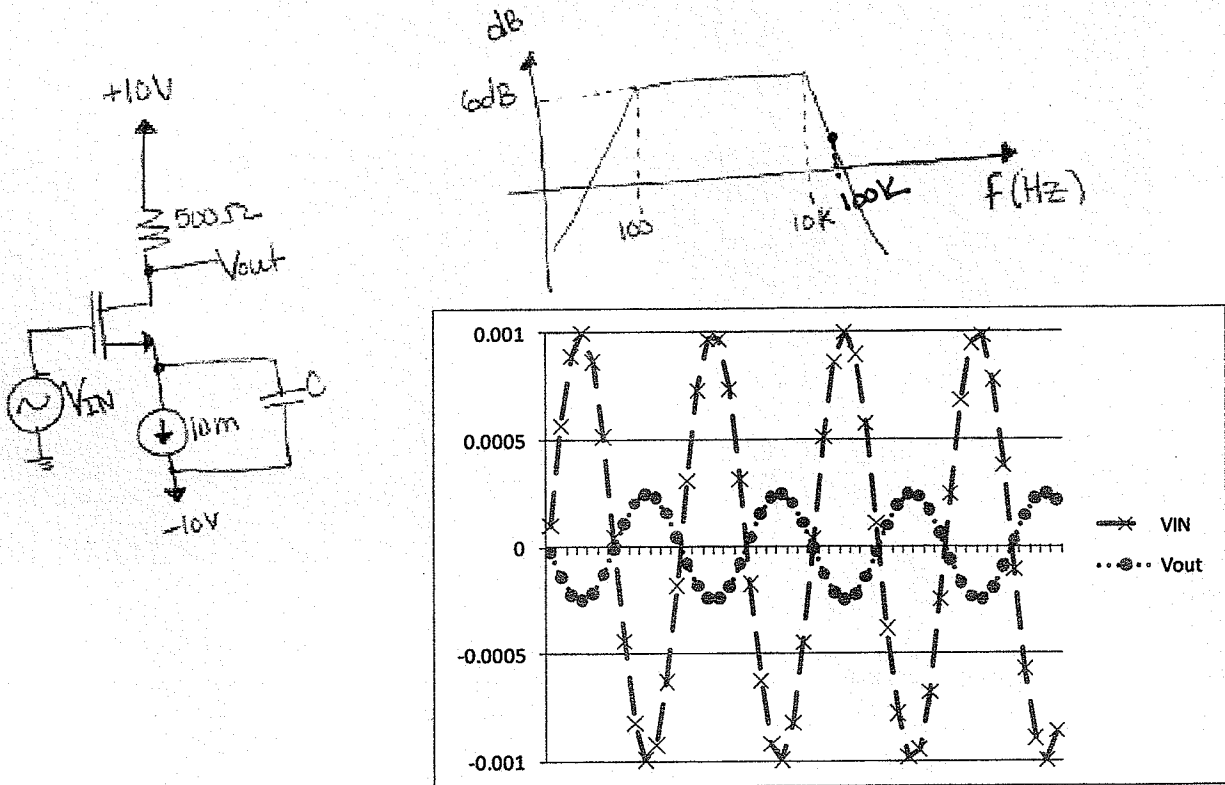
Problem 3 – (13 points)

For the circuit shown below, draw the AC small-signal equivalent circuit (use hybrid- π or model T) with the capacitors in it. Make sure that everything is labeled in terms of the transistor number. (e.g. g_{m1} , v_{gs2} , r_{o1} , etc.). $\lambda \neq 0$ for all transistors. (i.e. draw the small-signal with r_o included). Make sure to include drawing all R's unless they are floating.



Problem 4 – (12 points)

Let $V_t = 2V$, $\lambda = 0$, $k_n'(W/L) = 1 \text{ mA/V}^2$, $V_{IN} = 5 + 1 \text{ m sin}(\omega t)$. This amplifier was designed to achieve an overall gain of $-2V/V$. The magnitude Bode plot of the amplifier is shown below. An AC graph (DC is removed) of V_{in} and V_{out} is shown for an input frequency of 100 kHz . Why is the output peak not 2 mV ?



$$I_D = 10 \text{ mA} = \frac{1}{2} k_n (V_{GS} - V_t)^2 = \frac{1}{2} (3V - V_s)^2 \text{ mA/V}^2$$

$$V_s = 3V \pm \sqrt{20} \text{ V}$$

$$V_{GS} > V_t \text{ for operation}$$

$$5V - V_s > 2V$$

$$\text{thus } V_s = 3V - \sqrt{20} \text{ V}$$

$$V_D > V_G - V_t \text{ for saturation}$$

$$10V - (500\Omega)(10 \text{ mA}) > 5V - 2V \checkmark$$

therefore the transistor is saturated

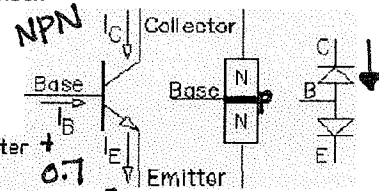
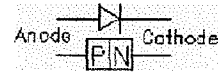
The transistor is both operating and saturated for an input signal with an offset of $5V$. The peak values of the input signal are not enough to throw the transistor out of saturation. The circuit is set to operate linearly, however, the frequency of the input signal is beyond the bandwidth of frequencies for which this circuit operates linearly. Therefore the expected value of 2 mV is not reached.

Introduction to Bipolar Junction Transistors (BJTs)

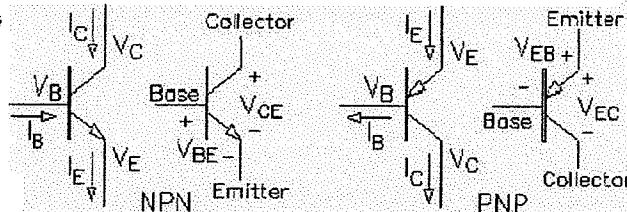
A transistor has three terminals-- the base, the collector, and the emitter. The current flow from the collector to the emitter (through the transistor) is controlled by the current flow from the base to the emitter. A small base current can control a much larger collector current.

Bipolar junction transistors (BJTs) consist of three layers of doped silicon. The NPN transistor has a thin layer of P-doped silicon sandwiched between two layers of N-doped silicon. Each P-N junction can act like a diode. In fact, this is a fairly good way to check a transistor with an ohmmeter (set to the diode setting).

The base-emitter junction always acts like a diode, but because the base is very thin, it makes the other junction act like a controlled valve (details to come later).



Symbols and conventions



PNP: Replace v_{BE} with v_{EB} and v_{CE} with v_{EC} in equations below

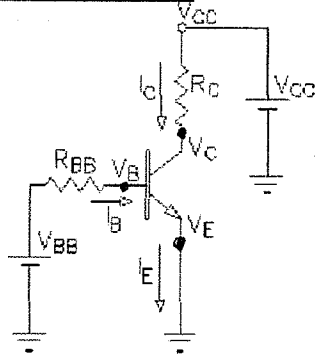
Very High Level Overview of how a transistor works:

- A small amount of base current controls a large emitter (collector) current

Analogy:

- Think of the transistor as an "electronic" tap able to control a large flow of electrons (from collector to emitter) with only a small variation in the "handle" (base)
- Water Tap Analogy: (water spigot)
 - Large amounts of H_2O controlled by very small movement of the tap

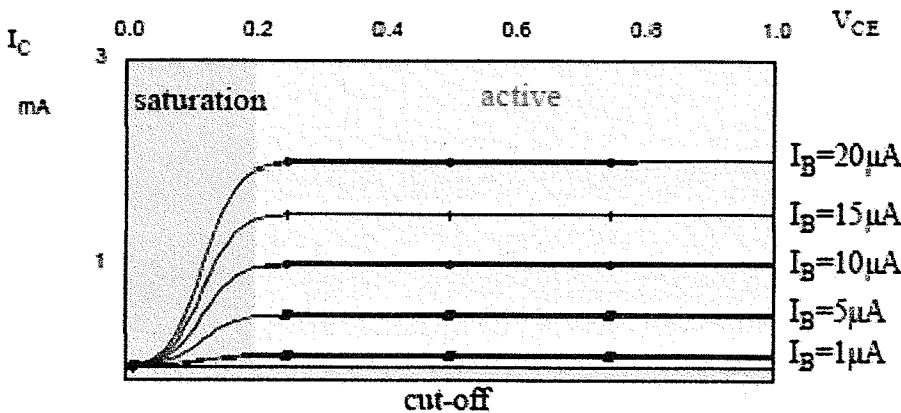
BJT Operation



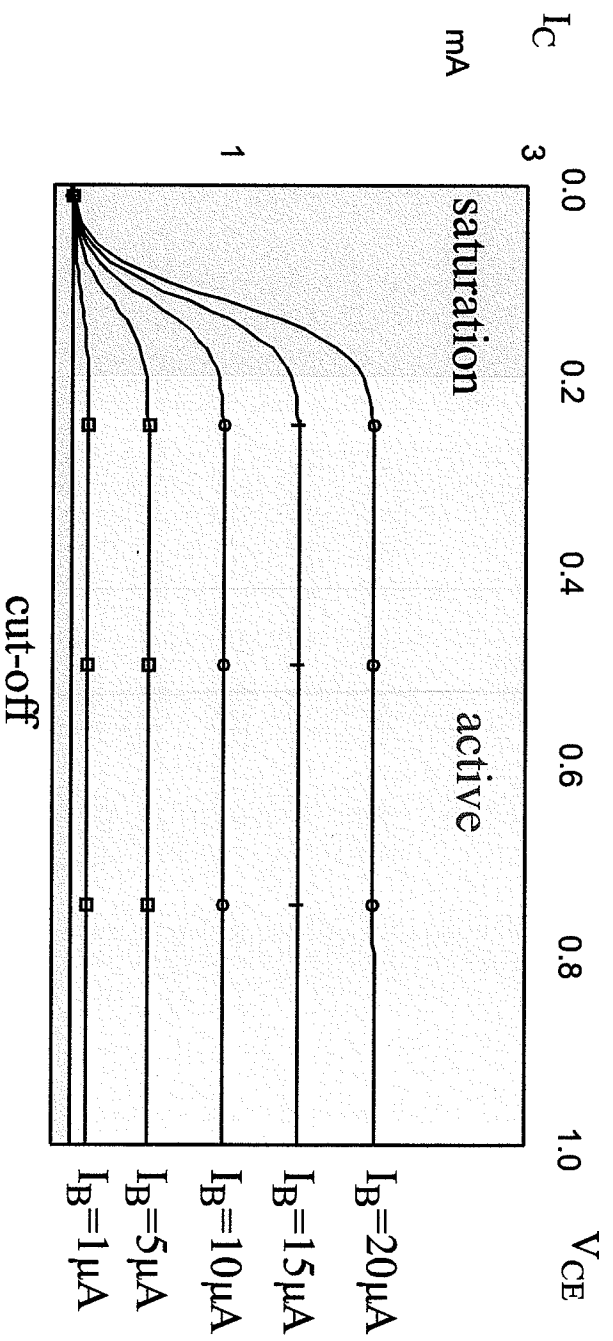
FOR PNP: Active: $V_C < V_B$; SAT: $V_B > V_C$

Modes or regions of operation (v_{BE} and v_{CE} are approximate)

Cutoff (off)	Active (partially on)	Saturation (fully on)
$v_{BE} < 0.7V$	$v_{BE} \approx 0.7V$	$v_{BE} \approx 0.7V$
$i_B = 0$	$i_B > 0$	$i_B > 0$
$i_C = 0$	$v_{CE} \geq 0.7V$	$v_{CE} = 0.2 \text{ to } 0.7V$
	$i_C = \beta i_B = \alpha i_E$ controlled by the transistor	$i_C < \beta i_B$ limited by something outside of the transistor



Regions of Operation



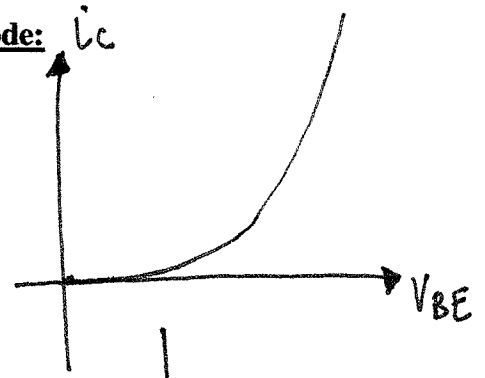
Summary of BJT Current-Voltage Relationships in the Active Mode:

$i_c = I_S e^{v_{BE}/V_T}$ (n=1 always for BJT) {Ebers-Moll equation}

$i_B = \frac{i_C}{\beta} = \left(\frac{I_S}{\beta}\right) e^{v_{BE}/V_T}$

$i_E = \frac{i_C}{\alpha} = \left(\frac{I_S}{\alpha}\right) e^{v_{BE}/V_T}$

V_T : Thermal Voltage
 $\approx 25\text{mV}$ at Room Temp.



ACTIVE

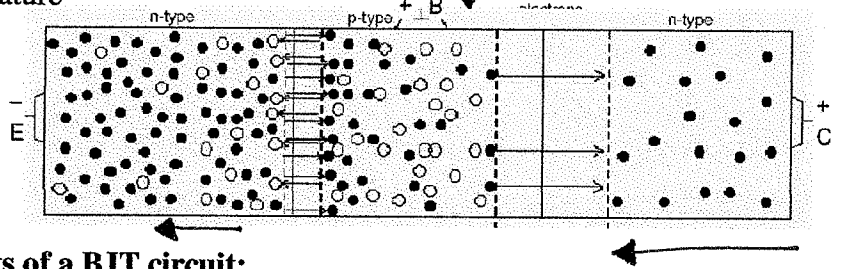
Note: For the pnp transistor, replace v_{BE} with v_{EB}
 $I_C = \alpha I_E = \beta I_B$ $I_E = (\beta + 1) I_B$ $\left[\beta = \frac{\alpha}{1 - \alpha} \quad \alpha = \frac{\beta}{\beta + 1} \right]$
 $V_T = \text{thermal voltage} \cong \sim 25\text{mV}$ at room temperature

Temperature dependencies

$v_{BE} = 0.7\text{V}$ (decreases about $2.1\text{mV}/^\circ\text{C}$)

at constant i_C : $\Delta v_{BE} = \frac{-2.1\text{mV}}{\text{degC}}$

at constant v_{BE} : i_C increases by 8% per $^\circ\text{C}$ (10x per 30°C)



Method for solving DC voltages and currents of a BJT circuit:

1). Start by assuming transistor is in active mode

Either use given values for base-emitter voltage, or use

$V_{BE} = 0.7\text{V}$ (npn)

$V_{EB} = 0.7\text{V}$ (pnp)

2). Solve for the BJT node voltages and currents

* Always take a loop from base through to emitter

- Voltages: sometimes can read off directly, otherwise use loop equation
- Once you have one current, you can get the other two from the active mode equations

3). Check to see if the solution is consistent!

$V_C \geq V_B > V_E$ npn active more explicitly: $V_{CB} \geq 0, V_{BE} \geq 0.7\text{V}$

$V_E > V_B \geq V_C$ pnp active more explicitly: $V_{CB} \geq 0, V_{EB} \geq 0.7\text{V}$

4). If the solution is consistent, stop → you are done

If not, the transistor is either in saturation or cutoff

→ go to 2) however active mode equations **do not** apply!

→ Now use: saturation: $v_{BE} \approx 0.7\text{V}$ and $v_{CE} \approx 0.3\text{V}$ for npn

($v_{EB} \approx 0.7\text{V}$ and $v_{EC} \approx 0.3\text{V}$ for pnp)

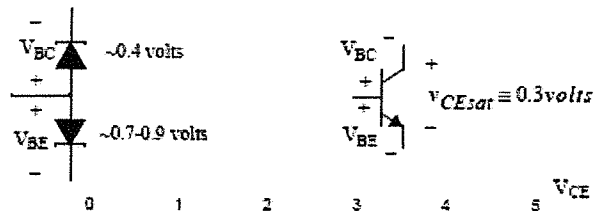
cutoff: set all currents to

approximately 0:

$i_C = 0 \quad i_E = 0 \quad i_B = 0$

- With both diodes forward biased, the collector-to-emitter voltage, v_{CE} , saturates toward a constant value

Saturation



NPN ACTIVE AND ON when:

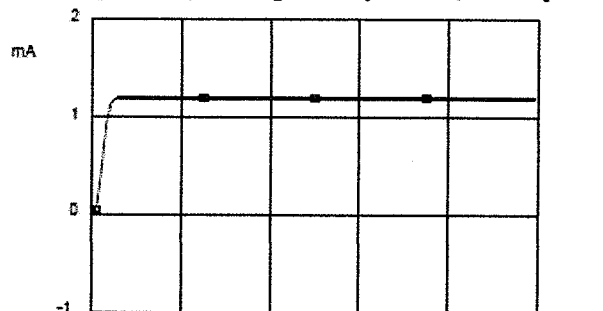
$v_{BE} \geq V_{BEon}$ ($V_{BEon} \cong 0.4\text{V}$)

$V_C \geq V_B > V_E$ and $V_{CE} > 0.3\text{V}$

PNP ACTIVE AND ON when:

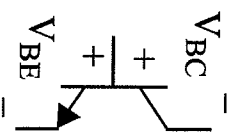
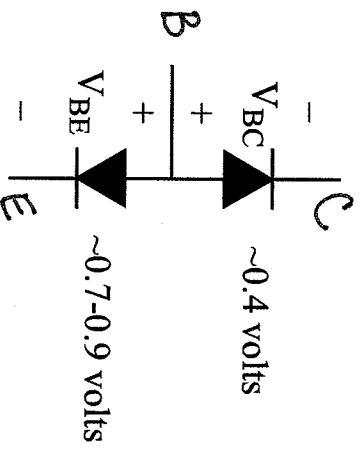
$v_{EB} \geq V_{EBon}$

$V_E > V_B \geq V_C$ and $V_{EC} > 0.3\text{V}$

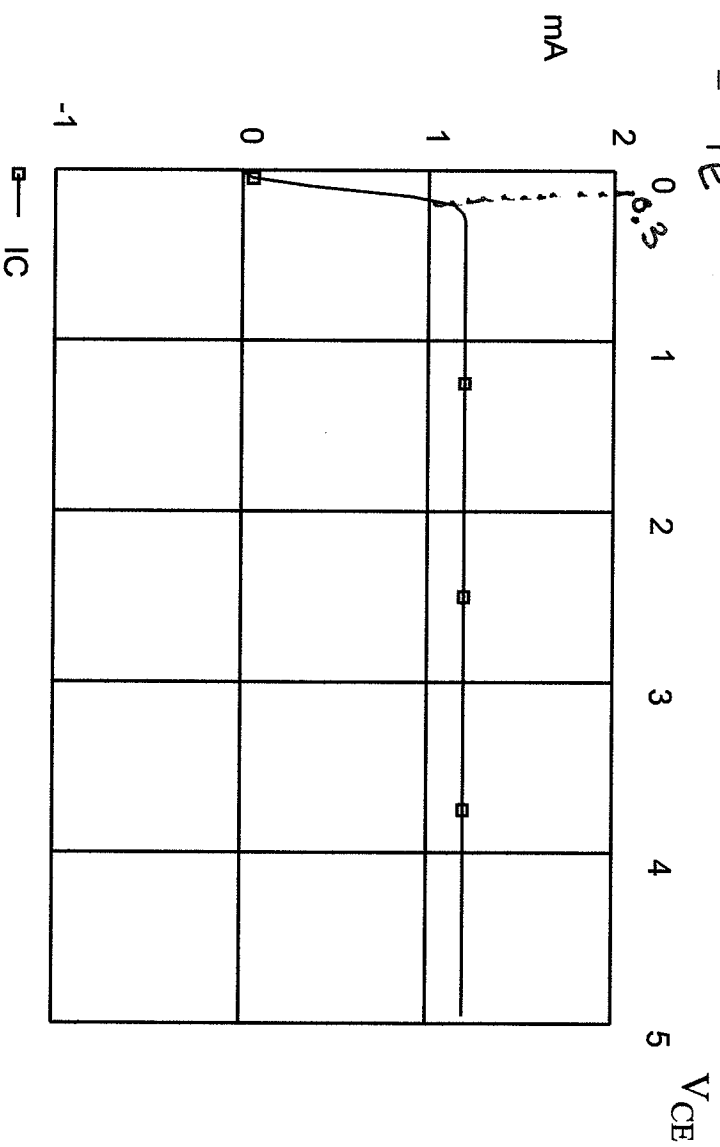


Saturation

- With both diodes forward biased, the collector-to-emitter voltage, V_{CE} , saturates toward a constant value

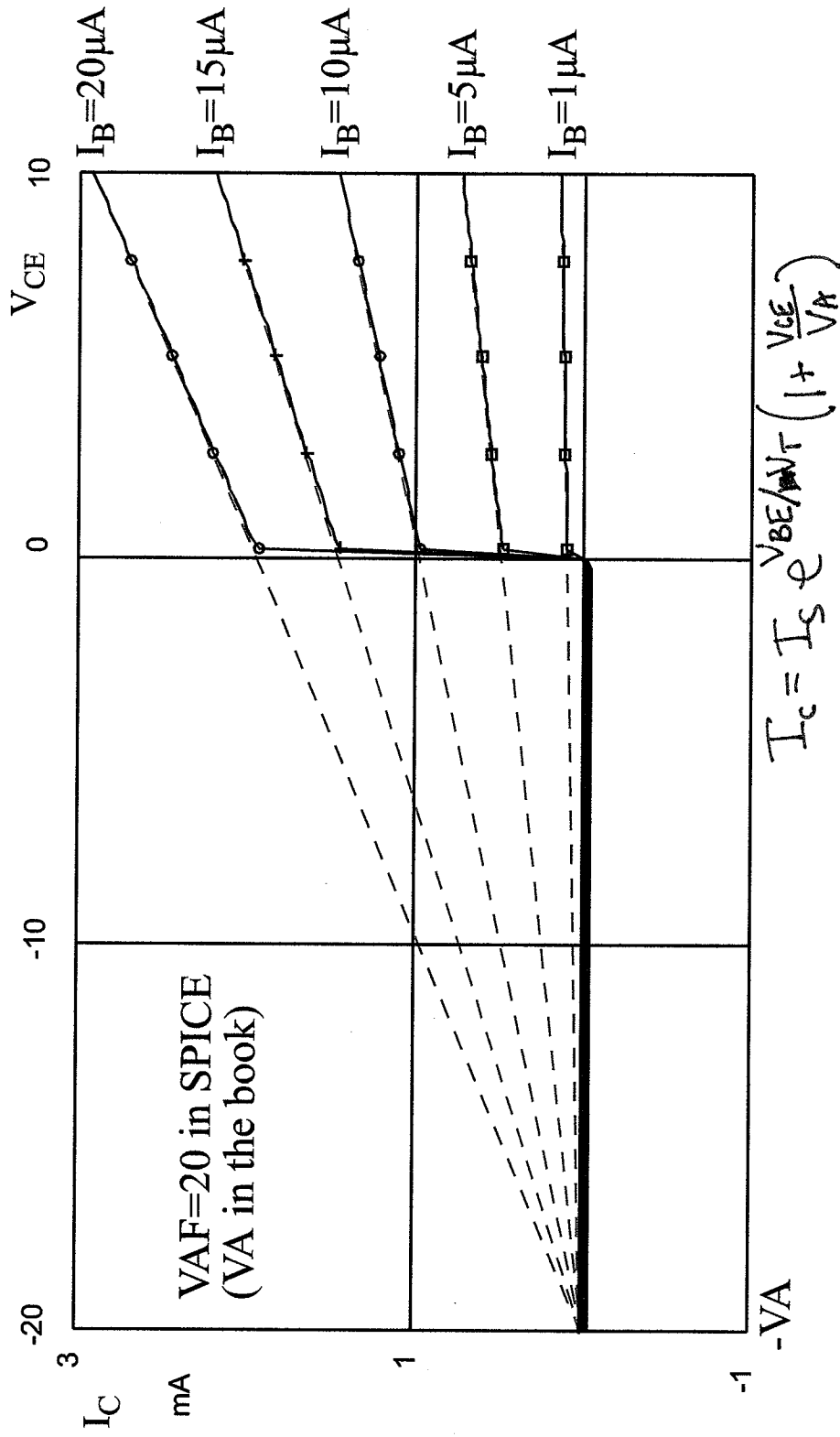


Do NOT USE $I_c = \alpha I_E = \beta I_B$ for SAT Analysis
 $V_{CEsat} \approx 0.3 \text{ volts}$



Early Voltage

- The I_C vs. V_{CE} curves in the active region have a finite slope to them due to this i_C dependence on V_{CB}
- *Early* showed that these slopes all converge to one negative voltage point



Example 29:

Find V_E and I_c for each circuit. Assume that $|V_{BE}| = 0.7V$ and $\beta = 40$. Both transistors are being operated in the active mode.

(a) NPN Assume Active

$+5 - 0.7 - I_E(1k) = 0$
 $I_E = \frac{4.3}{1k} = 4.3mA$
 $I_C = \alpha I_E = \beta I_B$
 $I_C = \frac{\beta}{\beta + 1} I_E = \frac{40}{41}(4.3m) = 4.2mA$
 $V_E = I_E(1k) = 4.3V$
 $V_B = 5V$
 $V_C = 12 - I_C(1k) = 7.8V$
 $V_C > V_B \therefore \text{ACTIVE}$

$I_C + I_B = I_E$

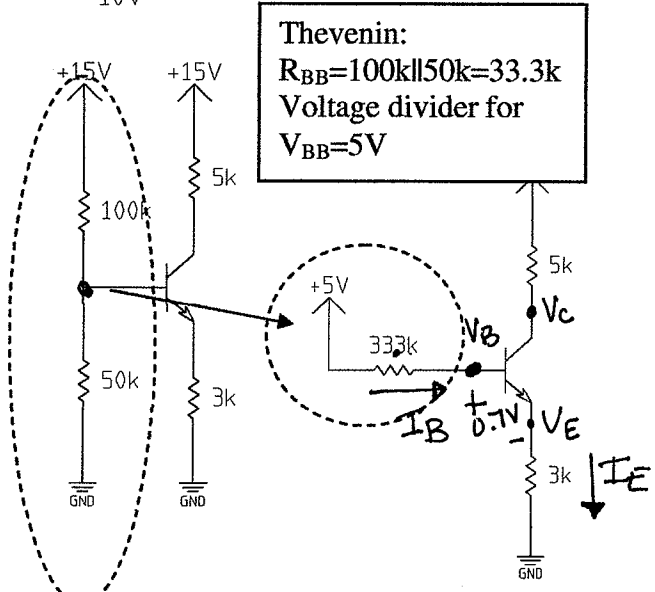
(b) PNP Assume ACTIVE

$+10 - I_E(2k) - 0.7 = 0$
 $I_E = \frac{9.3}{2k} \approx 4.7mA$
 $I_B = \frac{\beta}{\beta + 1} I_E = \frac{40}{41}(4.7m) = 4.5mA$
 $V_E = 10 - I_E(2k) \approx 0.7V$
 $V_B = 0$
 $V_C = -10 + I_C(1k)$
 $V_C = -5.5V$
 $V_C < V_B \checkmark \text{ ACTIVE}$
 $I_E = I_B + I_C$

Example 31

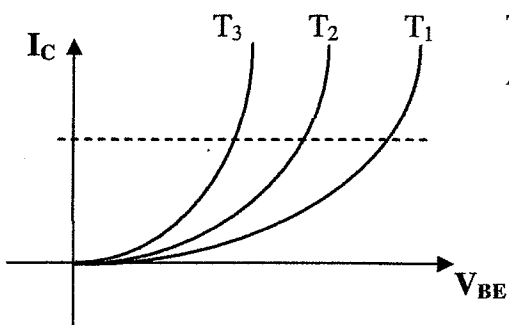
$\beta = 100$
Assume Active

$+5 - I_B(333k) - 0.7 - I_E(3k) = 0$
 $I_B = \frac{I_E}{\beta + 1}$
 $I_E = \frac{4.3}{3k + \frac{33.3k}{101}} = 1.29mA$
 $I_B = \frac{1.29m}{101} = 12.8\mu A$
 $I_C = \alpha I_E = \frac{100}{101}(1.29m) \approx 1.28mA$
 $+5 - I_B(33.3k) - V_B = 0$
 $V_B \approx 4.6V$
 $V_E = V_B - 0.7 \approx 3.9V$ OR $V_E = I_E(3k) = 3.87V$
 $V_C = 15 - I_C(5k) = 8.6V$
 $V_C = 8.6 > V_B = 4.6V \checkmark \text{ ACTIVE!}$



Temperature Effects:

NPN Transistor Characteristic



$T_3 > T_2 > T_1$
 As $T \uparrow, I \uparrow$ for fixed V_{BE}

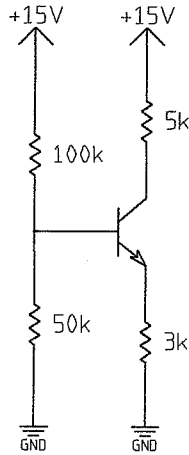
Thermal runaway: $T \uparrow \rightarrow I_C \uparrow \rightarrow P_D \uparrow \rightarrow T \uparrow \rightarrow I_C \uparrow \rightarrow P_D \uparrow \rightarrow \dots$

Bias BJT in the ACTIVE region

Goals:

- Stable I_C for any temperature. (Does not go into saturation region - similar to triode region for MosFet)
- Not dependant on the value of β .
- Not dependant on V_{BE} .

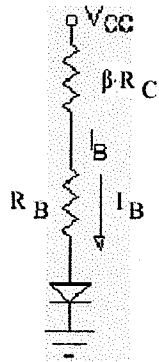
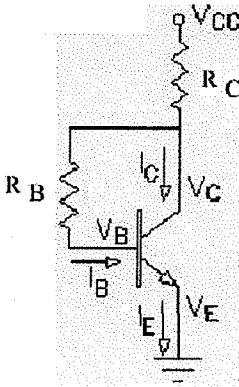
Configurations:



Rules of Thumb:

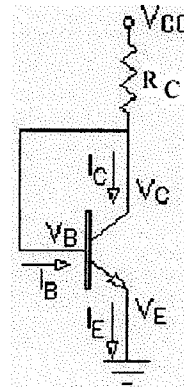
- $\beta R_E > R_{BB}$

A couple of other bias schemes



$$I_B = \frac{V_{CC} - 0.7V}{R_B + \beta R_C}$$

The bigger R_C is with respect to R_B , the more stable I_C is



Taken to extremes, I_C is now very stable at:

$$I_C = \frac{V_{CC} - 0.7V}{R_C}$$

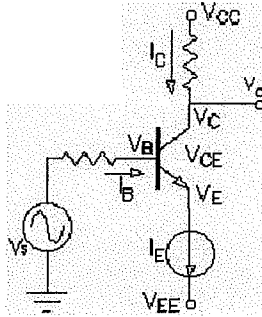
Seems like a useless circuit, but...

OR

Use Current Mirror:

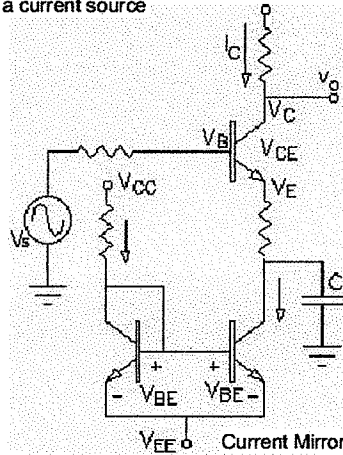
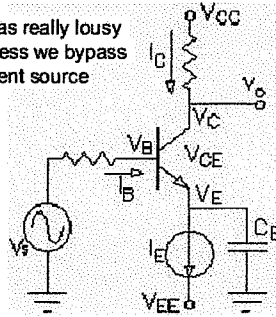
Current source bias: We could make the bias current very stable if we had a current source

If we can make current sources (drains), then...



For a perfect current source, $R_E = \infty$

which has really lousy gain unless we bypass the current source



Current Mirror

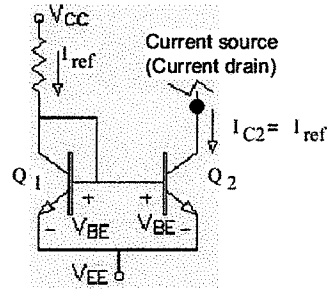
Current mirrors A way to make a current source (drain)

$$I_{C1} = \frac{V_{CC} - V_{EE} - 0.7V}{R_C} = I_{ref}$$

Recall that v_{BE} is really not exactly 0.7V, from Ebers-Moll eq.: $I_C = I_S e^{\frac{v_{BE}}{V_T}}$
 Because $v_{BE1} = v_{BE2}$, $I_{C1} = I_{C2}$

We can get a current source (usually called a current drain in this type of configuration). I could make a positive source if I used PNP transistors.

But, the transistors must be identical, and at the same temperature, like in an IC.



$$I_{REF} = I_{mA} \Rightarrow \frac{V_{CC} - V_{BE} - V_{EE}}{I_{REF}} = R$$