

## Not graded

1. An amplifier has the following transfer function:

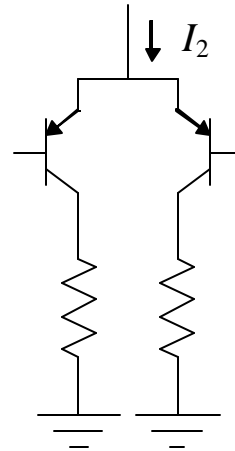
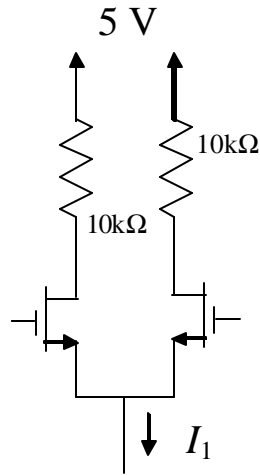
$$A(s) = \frac{10s(s/30,000 + 1)}{(s + 10)(1/20,000 + s)(s/60,000 + 1)}$$

- Sketch the bode plots for this transfer function.
- List the low-frequency and high-frequency 3dB points in rad/sec ( $\omega_L$  and  $\omega_H$ .)
- What is the midband gain in dB?
- List the pole frequencies
- List the zero frequencies
- What is  $\beta$  for a phase margin of  $90^\circ$ ?
- What is  $A_f$  for a  $\beta=2$ ?

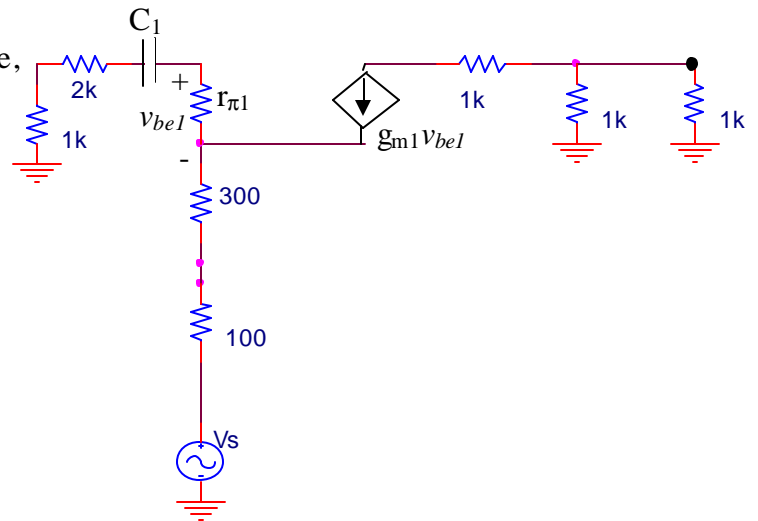
2. An uncompleted circuit consisting of two differential pairs is shown below. We wish to create a biasing network so that the *NMOS* differential pair transistors each have a differential gain equal to  $50V/V$ , and the *pnP* differential pair transistors each have a  $g_m$  of  $1.5 A/V$ . Assume that  $\beta$  is very large,  $|V_{BE}| = 0.7 V$ ,  $V_T = 25 mV$ ,  $|V_t|=1V$ , and  $k'(W/L)=1 mA/V^2$  for this entire problem. You may neglect the Early effect.

- What value of  $I_1$  and  $I_2$  is required?
- Using the schematic below, draw a current mirror biasing network to provide the required dc currents. You may use no more than 2 npn transistors, 5 *pnP* transistors, and one resistor of any value. Assume all transistors are identical in size. You may only use the +5 V power supply shown.

(Don't worry about connecting anything to the inputs or outputs of the differential pairs; we're only concerned with the biasing network in this problem. Assume that the MOSFET's are biased to a saturation region. Also, don't worry about the value of the collector resistors shown.)



3. (a) Using the short-circuit time constant technique, what is the resistance seen by  $C_1$ ?

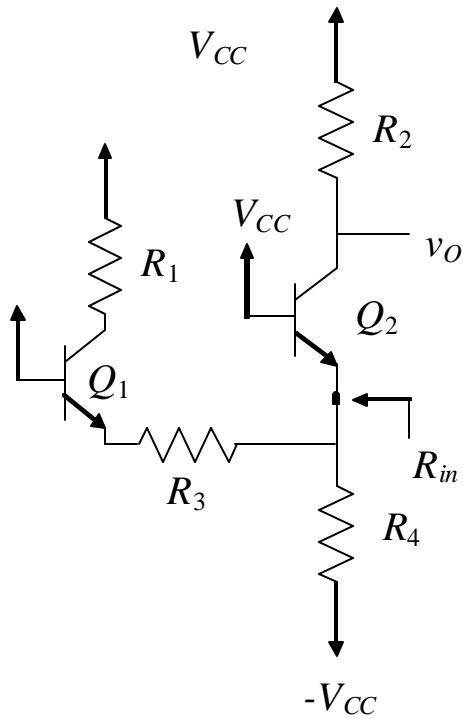


(b) Describe in your own words the Miller Effect.

(c) As a general rule of thumb (discussed in lecture), if your low frequency poles are 4 and 9 rad/sec and your low frequency zeros are 16 rad/sec, find  $\omega_L$ .

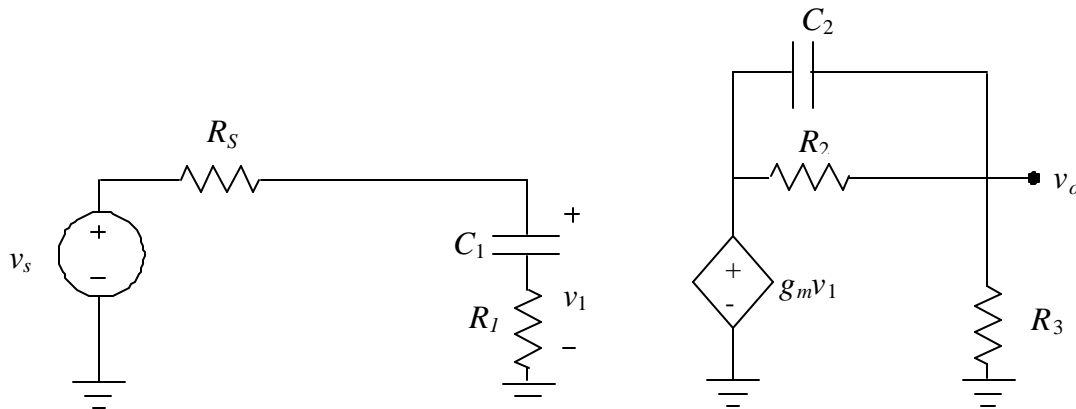
4. Assume the transistors below have a finite  $\beta$  and an infinite Early voltage.

Write an expression for the input resistance  $R_{in}$  in the circuit shown below. Your expression should include *only* real resistances ( $R_1, R_2, R_3, R_4$ , or a subset of these) and possibly  $\beta$ ,  $r_{e1}$  or  $r_{\pi 1}$ , and  $r_{e2}$  or  $r_{\pi 2}$ . (Assume both transistors have the same  $\beta$ .) Circle your answer.



5. For the circuit shown below, derive expressions for:

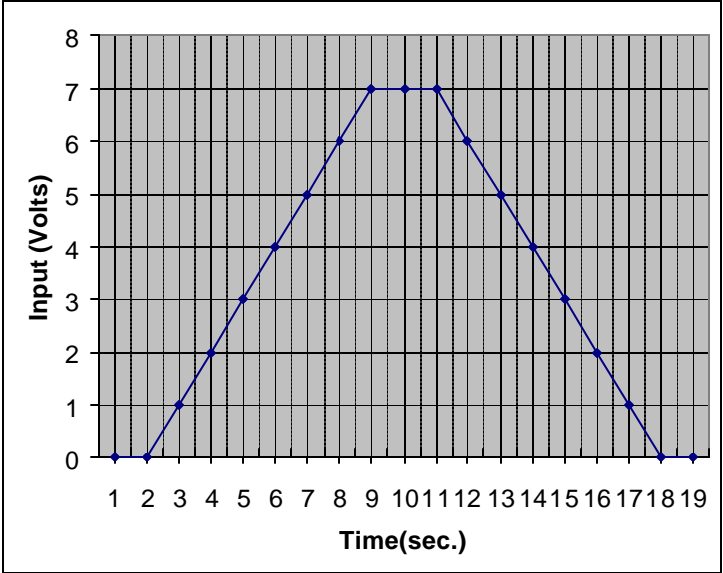
- the midband gain  $A_M$ , the low-frequency poles and/or zeros (if any; state if none), and the high-frequency poles and/or zeros (if any; state if none)



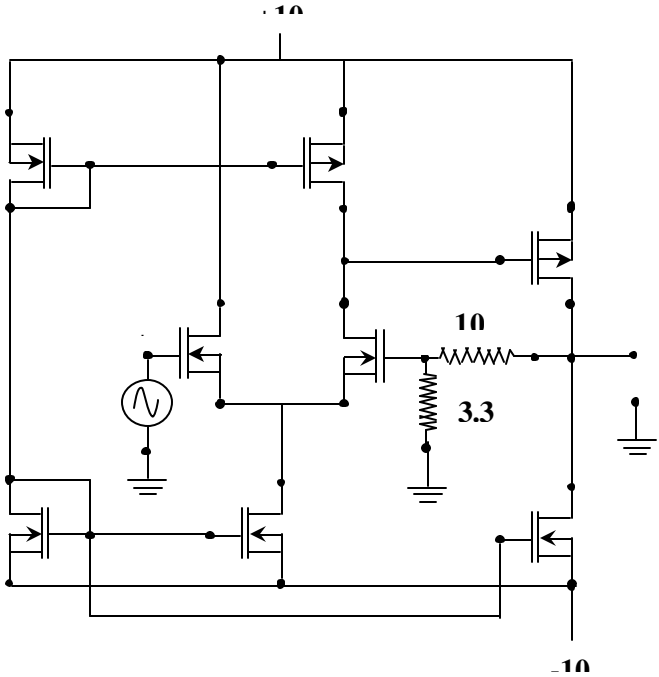
6. Design a MosFet differential amplifier to operate with a dc current bias of 2mA through each transistor and to provide a differential gain equal to 100V/V. The transistors have  $k'_n W/L=4\text{ma/V}^2$ ,  $V_t=1\text{V}$ .

- State the required dc bias voltage ( $V_{GS}$ ) needed for the amplifier to work correctly.
- Design a current mirror to supply the needed current bias. Draw the schematic and all values. Any value of R can be used.
- After choosing your current mirror configuration, state the minimum value for the gate voltage in order for the amplifier to operate correctly.

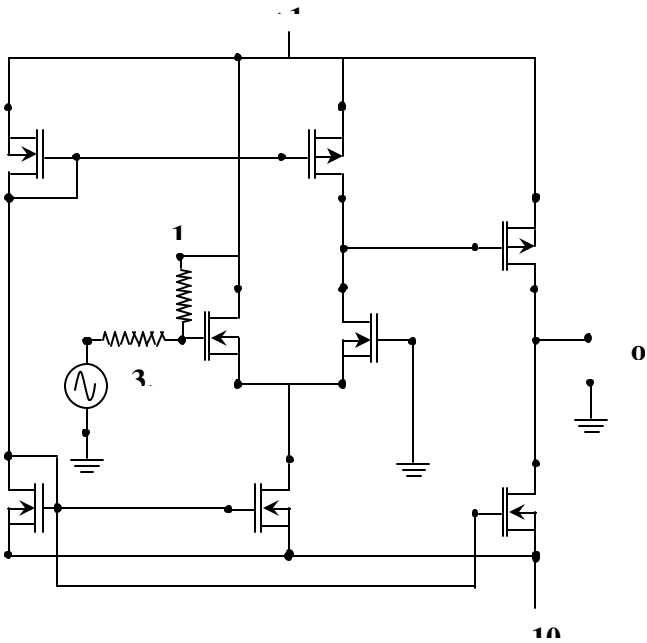
7. (a) Using the input signal below, sketch output voltages for  $v_o$  for a class A, class B, and a class AB amplifier. Assume that all transistors in each class are biased correctly and  $V_{CC}=5V$ ,  $V_{BE}=0.7V$  (assume constant),  $V_{CE,sat}=0.3V$ , and  $R_L=2k\Omega$  for each output stage.



8. (a) What type of feedback is employed in the circuits below:

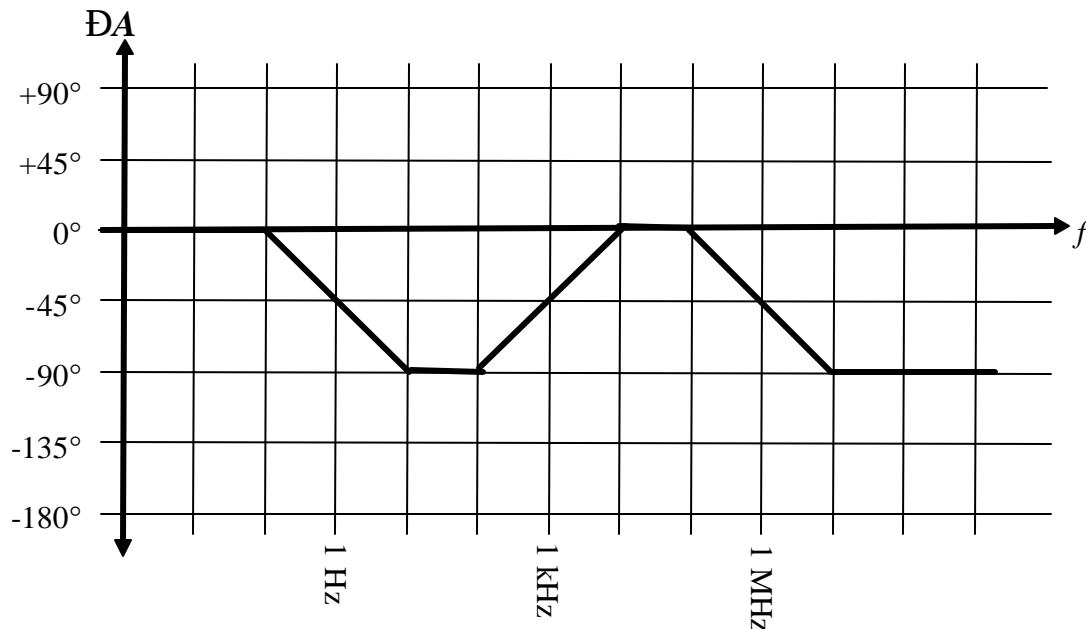


(i)



(ii)

9. The Bode approximation of an amplifier's phase response is shown at below. Draw the Bode magnitude plot of this amplifier below. The gain of the amplifier at 0.001 Hz is 120 dB.



10. A voltage amplifier (voltage input, voltage output) having an open-circuit gain of 300, an input resistance of  $20 \text{ k}\Omega$ , and an output resistance of  $500 \Omega$  is connected in a negative-feedback loop.

(a) Which feedback topology (e.g., series-shunt, series-series, etc.) would be used in this situation?

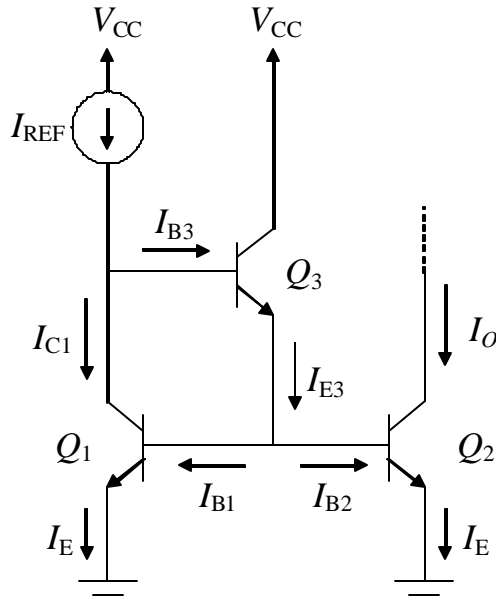
The feedback network has an  $R_{11}$  and  $R_{22}$  of  $10 \text{ k}\Omega$  and provides a feedback factor  $b = 0.2$ . The amplifier is fed by a voltage source having  $R_S = 4 \text{ k}\Omega$ , and a load resistance  $R_L = 5 \text{ k}\Omega$  is connected at the output.

(b) What is  $A$ ? (Hint: It is *not* 300!)

(c) What is the closed-loop gain  $A_f$  of the feedback amplifier?

(d) What is the feedback amplifier's input resistance  $R_{in}$ ?

11. Improved Current Mirror. The basic BJT current mirror we studied in class produces an output current  $I_O$  equal to  $I_{REF}/(1 + 2/\beta)$ . The output current  $I_O$  is not *exactly* equal to  $I_{REF}$  is due to the base currents of the transistors. An improved BJT current mirror (a very commonly-used circuit) is shown below:



We have begun the analysis of this circuit by noting that  $Q_1$  and  $Q_2$  must have the same emitter current ( $I_E$ ) since they have the same base-emitter voltage.

(a) Write expressions for the following currents as functions of  $\beta$  and  $I_E$ . Assume that all transistors have the same finite value of  $\beta$ . The variables  $I_{REF}$  and/or  $a$  should *not* appear in any expression below.

$$I_{B1} =$$

$$I_{B2} =$$

$$I_{E3} =$$

$$I_{B3} =$$

$$I_{C1} =$$

$$I_O =$$

(b) Note that  $I_{REF} = I_{C1} + I_{B3}$ . Solve for  $I_O$  as a function of  $\beta$  and  $I_{REF}$ . (Eliminate the variable  $I_E$  from your expression.)

(c) For the case where  $\beta = 100$ , a basic current mirror has a gain of:

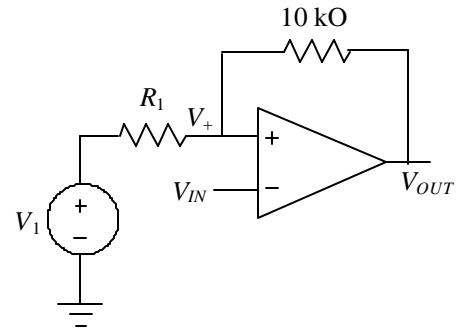
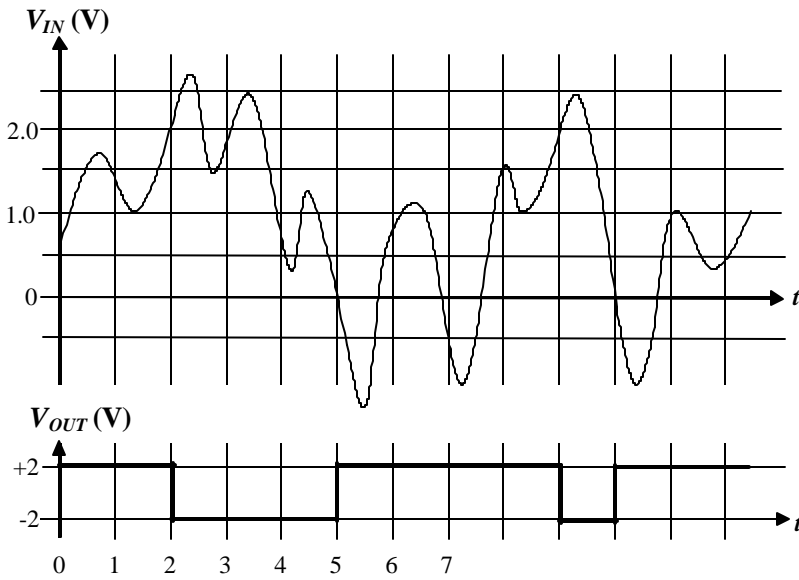
$$I_O/I_{REF} = 1/(1 + 2/\beta) = 0.98039$$

where we have expressed the result to five significant figures. Calculate the numerical gain of this improved current mirror for  $\beta = 100$ , and express your answer with five significant figures. You should see a significant improvement in performance.

$$I_O/I_{REF} =$$

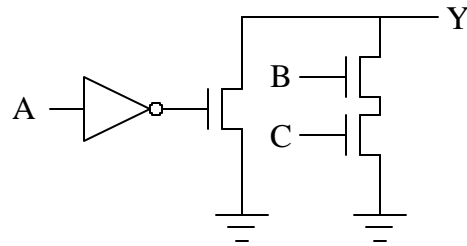
(d) If we assume that  $V_{BE} = 0.7$  V for all transistors, what voltage will appear at the bottom of the  $I_{REF}$  current source?

12. Hysteresis. The waveform  $V_{IN}(t)$  shown below is fed into the comparator-based circuit shown, and the output waveform  $V_{OUT}(t)$  is measured.  $V_1$  is a dc voltage source.



- (a) What is the value of  $V_+$  at time  $t = 1.999$ ?
- (b) What is the value of  $V_+$  at time  $t = 4.999$ ?
- (c) Find  $R_1$  and  $V_1$ . (Remember to include units in your expressions.)

13. Shown below is a pull-down network (PDN) for a CMOS digital logic gate:



- (a) Fill in the following logic table for a circuit using this pull-down network and a complementary pull-up network (not shown). Each value of  $Y$  should be either 0 or 1.

A	B	C	Y
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

- (b) If each transistor in this PDN has the same 'on' resistance  $r_{DS}$ , what is the equivalent resistance between the output and ground for the input  $A=0, B=C=1$  (in terms of  $r_{DS}$ )?

(c) If each transistor in this PDN has the same 'on' resistance  $r_{DS}$ , what is the equivalent resistance between the output and ground for the input  $A=B=C=1$  (in terms of  $r_{DS}$ )?

(d) Assume each transistor has  $W = 5\mu\text{m}$  and  $L = 0.5\mu\text{m}$ , and we are using a CMOS process where  $k_n' = 80 \mu\text{A}/\text{V}^2$ ,  $V_m = 0.5 \text{ V}$ , and  $V_{DD} = 5 \text{ V}$ . What is the 'on' resistance ( $r_{DS}$ ) of a single transistor? Don't forget units!

14. Power Dissipation in Digital CMOS Circuits. In the following problem, ignore the "short-circuit" power dissipation discussed in class. Assume that power is dissipated through (1) the ' $fCV_{DD}^2$ ' dynamic process of charging and discharging capacitances, and (2) the ' $I_{leak}V_{DD}$ ' static process caused by subthreshold leakage currents.

A digital CMOS chip consumes 100 mW at a power supply voltage of  $V_{DD} = 5 \text{ V}$  and a clock frequency of 100 MHz. When  $V_{DD}$  is reduced to 2.5 V and the clock frequency is held steady at 100 MHz, the power consumption drops to 40 mW.

- (a) What power dissipation  $P$  would you expect for  $V_{DD} = 4 \text{ V}$  and a clock frequency of 100 MHz?
- (b) What power dissipation  $P$  would you expect for  $V_{DD} = 5 \text{ V}$  and a clock frequency of 50 MHz?
- (c) What power dissipation  $P$  would you expect for  $V_{DD} = 2.5 \text{ V}$  and a clock frequency of zero (e.g., a standby or 'sleep' mode)?