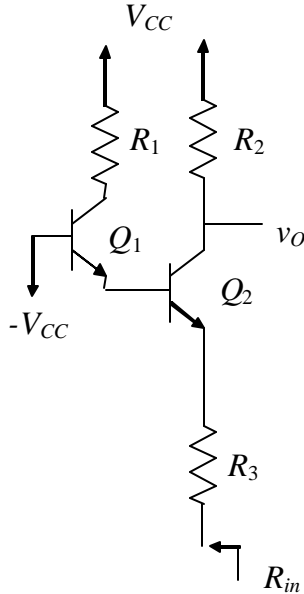


(Due Sept. 28 by 6pm in homework locker)

1. Assume the transistors below have a finite β and an infinite Early voltage.

- Write an expression for the input resistance R_{in} in the circuit shown below. Your expression should include *only* real resistances (R_1, R_2, R_3 , or a subset of these) and possibly β, r_{e1} or $r_{\pi 1}$, and r_{e2} or $r_{\pi 2}$. (Assume both transistors have the same β .) Circle your answer. *Hint: Use Resistance-Reflection rule*



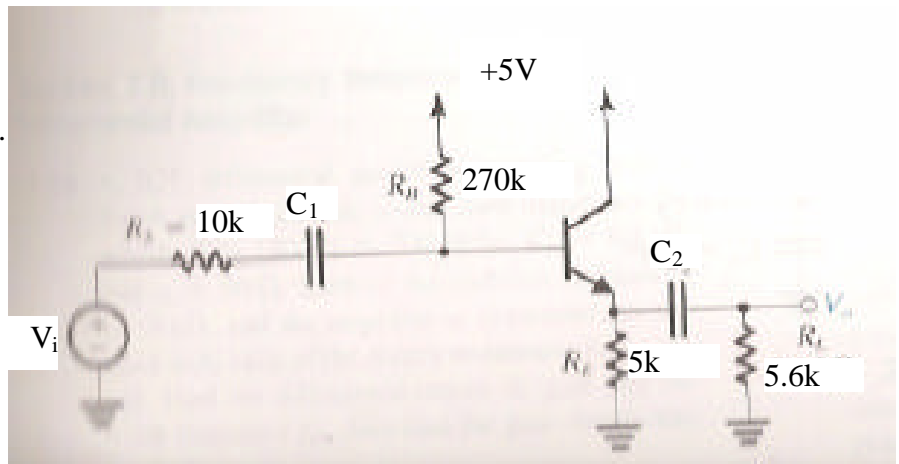
2. An amplifier has the following transfer function:

$$H(s) = \frac{10s(s/10 + 1)(s/100 + 1)(s/10000 + 1)}{(s/20 + 1)(s/200 + 1)(s/400 + 1)(s/1000 + 1)(s/2000 + 1)}$$

- List the pole frequencies
- List the zero frequencies
- State the midband gain in dB
- Sketch the Bode plots for this system, labeling frequencies, gains, and slopes of interest.
- Determine the low frequency 3dB corner, ω_L .
- Determine the high frequency 3dB corner, ω_H .

3. Design the circuit to find C_1 and C_2 so that a dominant pole at 100Hz is obtained. C_1 should be 10 times that of C_2 and the total capacitance should be minimized. Analyze the circuit using $\beta = 120, C_{\mu} = 0.5\text{pF}$, and $C_{\pi} = 0.25\text{pF}$ to find:

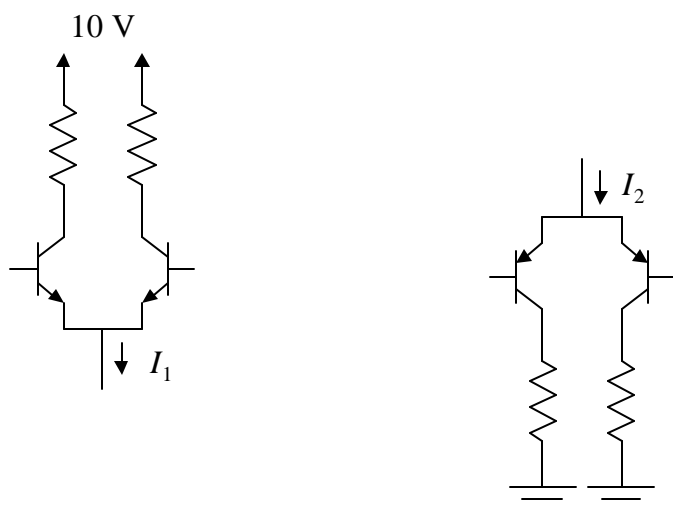
- midband gain A_M
- low-frequency 3-dB point, ω_L .
- high-frequency 3-dB point, ω_H .



4. An uncompleted circuit consisting of two BJT differential pairs is shown below. We wish to create a biasing network so that the *npn* differential pair transistors each have a g_m of 2 mA/V and the *pnp* differential pair transistors each have a g_m of 60 mA/V. Assume that β is very large, $|V_{BE}| = 0.7$ V, and $V_T = 25$ mV for this entire problem. You may neglect the Early effect.

Now draw the schematic of the current mirror biasing network to provide the required dc currents. You may use no more than 2 npn transistors, 3 *pnp* transistors, and two resistors less than 5k Ω . Assume all transistors are identical in size. You may only use the +10 V power supply shown.

(Don't worry about connecting anything to the inputs or outputs of the differential pairs; we're only concerned with the biasing network in this problem. Also, don't worry about the value of the collector resistors shown.)



5. Design a MosFet differential amplifier to operate with a dc current bias of 1mA through each transistor and to provide a differential gain equal to 50V/V. The transistors have $k'_n W/L = 4\text{ma/V}^2$, $V_t = 1\text{V}$.

- State the required dc bias voltage (V_{GS}) needed for the amplifier to work correctly.
- Design a current mirror to supply the needed current bias. Draw the schematic and all values. Any value of R can be used.
- After choosing your current mirror configuration, state the minimum value for the gate voltage in order for the amplifier to operate correctly.