

(Due by Nov. 9 by 6pm in homework locker)

1. An analog signal in the range of 0 to +9V is to be digitized with a quantization error less than 0.5% of full scale. What is the number of bits required? What is the resolution of the conversion? If the range is to be extended to +9V with the same requirement, what is the number of bits required? For an extension to a range of 0 to +20V, how many bits are required to provide the same resolution? What is the corresponding resolution and quantization error?
2. (a) Name a clever circuit structure used to generate binary-weighted currents that does not require binary-weighted resistors?

(b) All else being equal, which ADC consumes more power: a flash ADC or a successive-approximation ADC?

(c) All else being equal, which ADC is *fastest*: a flash ADC, a successive-approximation ADC, or a dual-slope ADC?

(d) All else being equal, which ADC is *slowest*: a flash ADC, a successive-approximation ADC, or a dual-slope ADC?
3. Consider Fig. 9.38. On the staircase output of the S/H circuit roughly sketch the output of a simple low-pass RC circuit with a time constant that is (a) one-half of the sampling interval and (b) equal to the sampling interval.
4. What is the input resistance seen by V_{REF} in the circuit of Fig. 9.41 if $R=1k\Omega$?
5. Design a 3-bit flash ADC such as that shown in Fig. 9.45. How many comparators are required? For an input signal in the range of 0 to +9V, what are the reference voltages needed? Show how they can be generated using a 9V reference and several $1k\Omega$ resistors? Indicate the digital code you expect at the output of the comparators and at the output of the logic for an input of (a) 0V, (b) 5.1V, (c) 9V