

HW #9 Sol'n

$$1. \quad \frac{1}{2} \cdot \frac{1}{2^N} \leq 0.005$$

$$\frac{1}{2^N} \leq \{2(0.005)\}^2 = 0.01$$

$$100 \leq 2^N \Rightarrow \log_2(100) \leq N \cdot \log_2(2)$$

$$\therefore 6.65 \leq N$$

$$\boxed{N=7}$$

$$\text{Resolution: } \frac{9V}{2^7} = \boxed{0.07V}$$

$$\log_2\left(\frac{18V}{0.07}\right) \approx \boxed{8=n} \leftarrow (+9V)$$

$$N = \log_2\left(\frac{20}{0.07}\right) \approx 8.16 \Rightarrow \boxed{N=9} \leftarrow 0 \text{ to } 20V$$

for 0 to +20V:

$$\text{Resolution} = \frac{20}{2^9} \approx \boxed{0.04V}$$

$$\text{error} = \frac{1}{2} \text{LSB} = \frac{1}{2}(0.04) = \boxed{0.02}$$

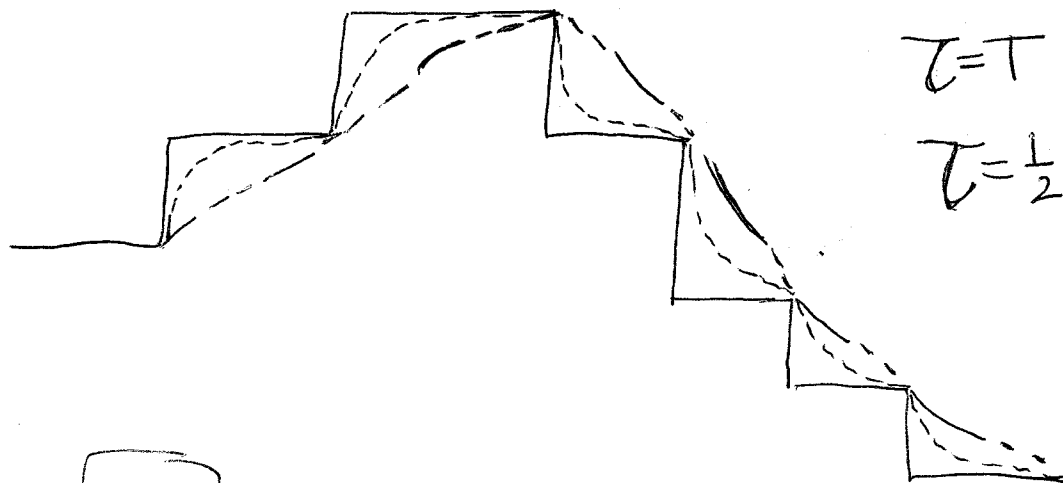
2. (a) R-2R resistive ladder

(b) Flash

(c) Flash

(d) Dual-slope ADC

3.



$T=T$ -----

$T=\frac{1}{2}T$ -----

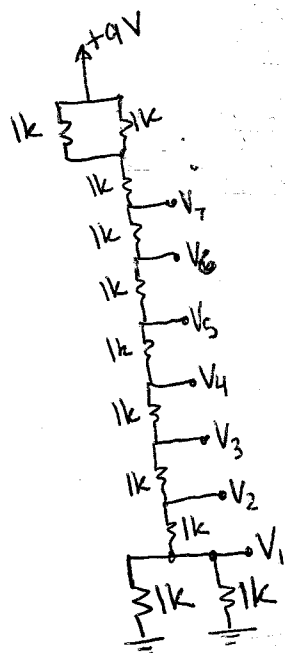
4. $R = 1k \Omega$

5. $2^N - 1 = 2^3 - 1 = 7$ comparators

0 to 9V:

1 LSB = $\frac{9}{2^3} = 1.125$

\therefore References \Rightarrow $\overset{V_1}{0.5625}$, $\overset{V_2}{1.6875}$, $\overset{V_3}{2.8125}$, $\overset{V_4}{3.9375}$,
 $\overset{V_5}{5.0625}$, $\overset{V_6}{6.1875}$, $\overset{V_7}{7.3125}$



Input	Comparator	Logic
0V	0000000	000
5.1V	0011111	101
9V	1111111	111

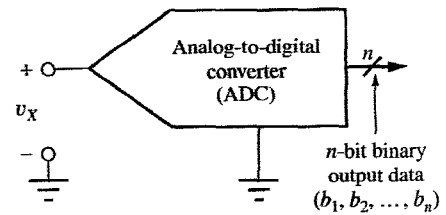


Figure 12.31 Block diagram representation for an A/D converter.

The n -bit number is a binary fraction representing the ratio between the unknown v_x and the converter's full-scale voltage $V_{FS} = K V_{REF}$.

12.4.1 A/D CONVERTER FUNDAMENTALS

Figure 12.32(a) is an example of the input-output relationship for an ideal 3-bit A/D. As the input increases from zero to full scale, the digital output code word stairsteps from 000 to 111. As the input voltage increases, the output code first underestimates the input voltage and then overestimates the input voltage. This error, called **quantization error**, is plotted in Fig. 12.32(b).

For a given output code, we know only that the value of the input voltage v_x lies within a 1-LSB quantization interval. For example, if the output code of the 3-bit converter is 101, then the input voltage can be anywhere between $\frac{9}{16} V_{FS}$ and $\frac{11}{16} V_{FS}$, a range of $V_{FS}/8$ or 1 LSB of the 3-bit converter. From a mathematical point of view, the circuitry of the converter should be designed to pick the values of the bits in the binary word to minimize the quantization error v_e between the unknown input voltage v_x and the nearest quantization level:

$$v_e = |v_x - (b_1 2^{-1} + b_2 2^{-2} + \dots + b_n 2^{-n}) V_{FS}|$$

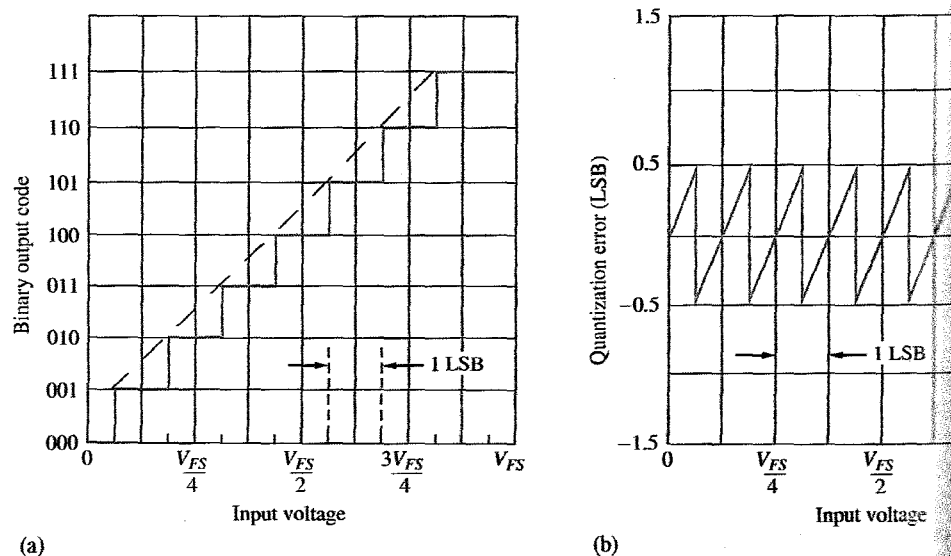


Figure 12.32 Ideal 3-bit ADC: (a) input-output relationship and (b) quantization error.

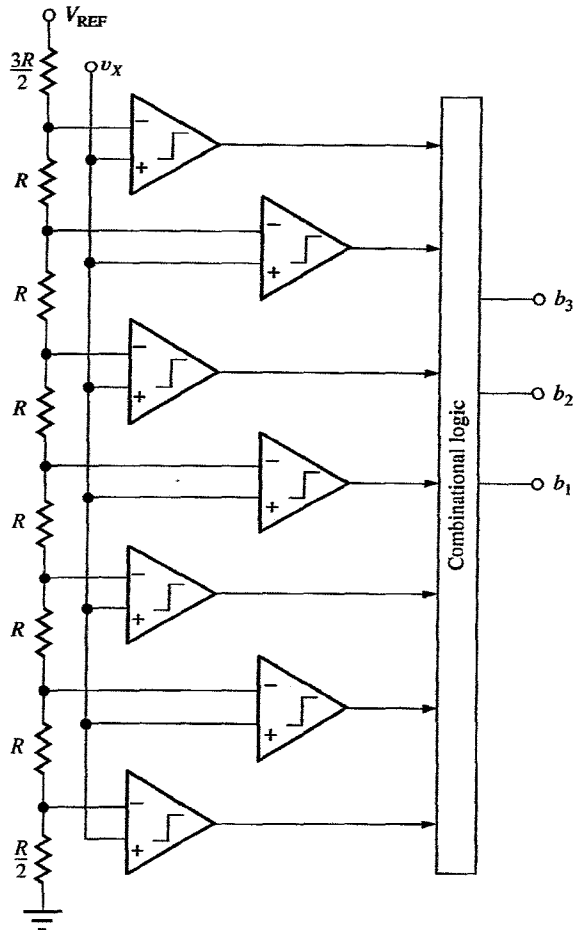


Figure 12.43 3-bit flash ADC.

parallel converter because of the device's inherent speed. Figure 12.43 shows a three-bit parallel converter in which the unknown input v_x is simultaneously compared to seven different reference voltages. The logic network encodes the comparator outputs directly into three binary bits representing the quantized value of the input voltage. The speed of this converter is very fast, limited only by the time delays of the comparators and logic network. Also, the output continuously reflects the input signal delayed by the comparator and logic network.

The parallel A/D converter is used when maximum speed is needed and is usually found in converters with resolutions of 10 bits or less because $2^n - 1$ comparators and reference voltages are needed for an n -bit converter. Thus the cost of implementing such a converter grows rapidly with resolution. However, converters with 6-, 8-, and 10-bit resolutions have been realized in monolithic IC technology. These converters achieve effective conversion rates as high as 10^8 – 10^9 conversions/second.

EXERCISE: How many resistors and comparators are required to implement a 10-bit flash ADC?

ANSWERS: 1024 resistors; 1023 comparators