

FEEDBACK AMPLIFIER

Create a SPICE schematic for the following circuit. For the opamp, use a 'ua741' from the 'eval' library.

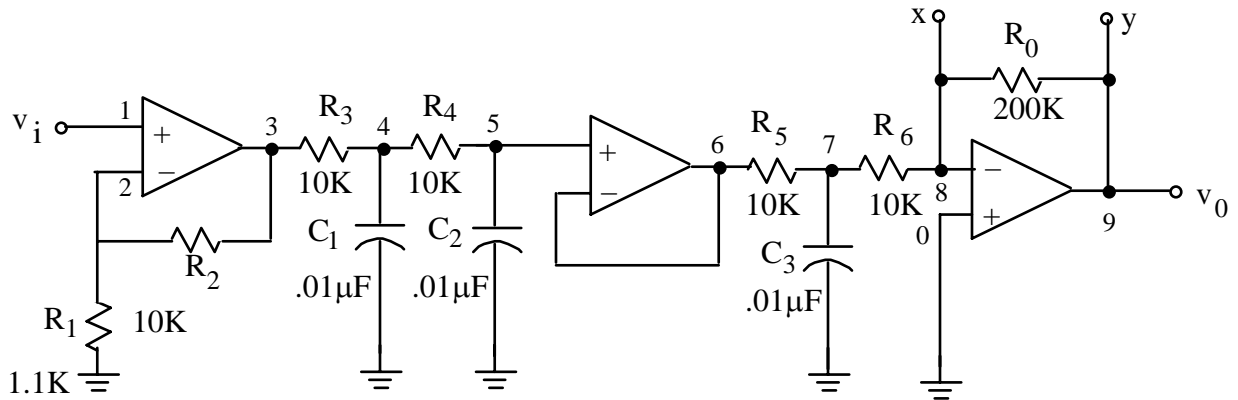


Fig. 1.

For the open loop amplifier above, simulate the magnitude and phase response. Then simulate the transient response to a 50-mV, 50-Hz, square wave. Report the rise and fall times.

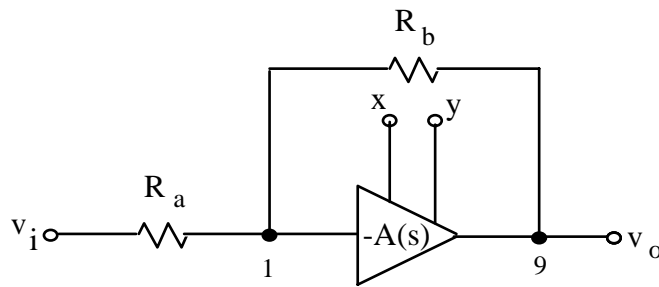


Fig. 2. Uncompensated shunt feedback amplifier.

Shunt Feedback

The circuit you just built is meant to act as a single op-amp, where v_i (in Fig. 1) is the negative input, and the positive input is implicitly grounded. This

circuit has a high input resistance, low output resistance, and reasonably high gain. The capacitors C_1 - C_3 limit the high-frequency response of this amplifier, playing the role that internal transistor parasitic capacitances play in actual IC (integrated circuit) op-amps.

In this part of the experiment we will close a feedback loop around the amplifier in several different ways and characterize its performance for each different feedback example. You will find that stability is not always assured, and the frequency-dependent properties of the op-amp (our Fig. 1 circuit) have a large effect on this stability or instability.

Connect a shunt feedback network around the amplifier, as shown in Fig. 2. The triangular block represents the entire 3-stage amplifier of Fig. 1. The triangular block represents the entire 3-stage amplifier of Fig. 1 (i.e., our “op-amp”). Note that this corresponds to the familiar “inverting amplifier” op-amp configuration. What would you expect the gain to be in this case? Terminals x and y should be left open. Note that the 200-Kilohm resistor labeled R_0 in Fig. 1 should **not** be removed.

First, referring to Fig. 2, let $R_a = 1 \text{ k}\Omega$ and $R_b = 3.3 \text{ k}\Omega$. Ground the input and run a transient simulation to observe the output. Does the feedback amplifier oscillate? If so, plot the waveform at v_o , and report the peak amplitude and the period.

Change the input to a 0.1 volt 50 Hz square wave and plot the output. Report the steady-state output voltage (flat portion of the waveform), and the voltage of the first (+) and second (-) peaks, and the ringing period.

Dominant Pole Compensation

Compensation is a technique used to make op-amps stable under closed-loop feedback conditions. Typically, a pole is introduced which is lower than the other high-frequency poles in the circuit. Will compensate our “op-amp” from Fig. 1 by adding a capacitance C_x across terminals x and y as shown in Fig. 3. Calculate the required value of C_x (see below).

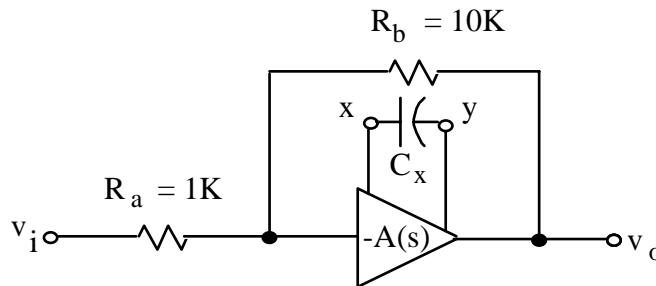


Fig. 3. Dominant pole compensated feedback amplifier.

Using the Bode magnitude plot from above to determine the dominant pole frequency. Then find the value of C_x as outlined on pp. 849-850 of the text. Wire C_x into the circuit between terminals x and y, as shown in Fig. 3.

Change the input to a 100-mV 50-Hz square wave and plot the output. Report the steady-state output voltage (flat portion of the waveform), and the voltage of the first (+) and second (-) peaks, and the ringing period.

Dominant Pole Compensation with Zero Cancellation

A slightly more complex compensation scheme is illustrated in Fig. 4. Compute the required values of R_x and C_x .

Change the input to a 100-mV 50-Hz square wave and plot the output. Report the steady-state output voltage (flat portion of the waveform), and the voltage

of the first (+) and second (-) peaks, and the ringing period.

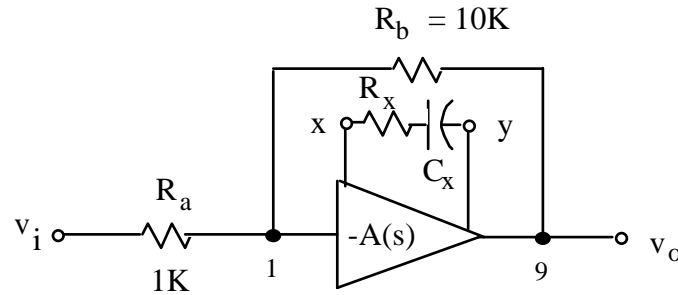


Fig. 4. Zero cancellation compensation.

Adjust R_x and C_x for optimum performance; that is, minimum overshoot consistent with smallest ringing and fastest rise and fall time.

Record the rise and fall time and overshoot of the waveform you consider optimum (in response to the same square wave as above simulations). Include a plot of the output waveform. Record the corresponding values of R_x and C_x .

What to turn in:

- 1) A printout of your SPICE schematic.
- 2) AC and transient response plots for the open loop amplifier.
- 3) Plots of transient responses from all three remaining sections (shunt feedback, dominant pole, and dominant pole with zero cancellation). Report the steady-state output voltage (flat portion of the waveform), and the voltage of the first (+) and second (-) peaks, and the ringing period for each configuration. Did the ringing period of the closed loop amplifier correlate with the ringing period of the compensated amplifier?

4) Anything else used to complete the assignment.