

UNIVERSITY OF UTAH  
ELECTRICAL AND COMPUTER ENGINEERING DEPARTMENT

ANALOG INTEGRATED CIRCUITS LAB

LAB 1  
MOSFET Characterization

**Objective:** In this lab, you will use the Keithley 4200 Semiconductor Characterization System to measure the current-voltage relationship of single  $p$ MOS and  $n$ MOS transistors. The 4200 is a fully automated device capable of measure currents below 100 pA. Using data taken in this assignment, you will fit first-order device equations to the subthreshold and above threshold regions of operation and extract basic process parameters such as threshold voltage and mobility.

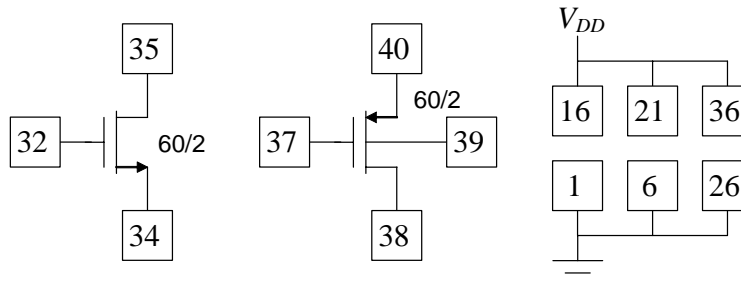
In all the lab assignments in this class, we will be using chips donated by AMI Semiconductor. These chips were fabricated in AMI's commercial ABN 0.5- $\mu$ m CMOS process, which has an oxide thickness  $t_{ox}$  of 140 Å (14 nm). We have two custom-designed chips for this class, labeled "A" and "B". One copy of each chip has already been placed in a solderless breadboard that you will use during this course. Your breadboard may be checked out at any time in the week when the teaching labs are open, but the breadboard and chips may not be removed from the labs under any circumstances. All work must be performed in the teaching labs, and breadboards should be checked back in when work is complete.

**Handling Chips.** Please note that CMOS chips can easily be damaged by static electricity, or electrostatic discharge (ESD). Make a point to ground yourself by touching a ground lead on your test equipment before wiring your breadboard. The leads on the chip packages are easily bent, so please refrain from removing the chips from your breadboard. If you have a problem with a chip, please talk to the T.A.

**Power:** We will be using a single-polarity power supply for this lab. You will need to use the power supplies that are located near the Keithley 4200s. Connect pins 1, 6, and 26 to ground. Connect pins 16, 21, and 36 to  $V_{DD} = 5.0$  V. Leave these power connections in place for all experiments. Even though the individual MOS transistors take no power from  $V_{DD}$ , it is necessary to set  $V_{DD}$  to 5.0 V to insure that the electrostatic discharge (ESD) protection circuits work correctly.

## Pin-out for Lab 1 – Chip A

All transistor dimensions are given in microns.



Part of the ESD protection circuitry on this chip is a  $300\ \Omega$  resistor in series with each pin. This resistor has no effect on gates since the current into a gate is zero, so the voltage drop across the resistor is zero. However, the source and drain pins pull current and will thus have voltage drops associated with the protection circuitry. To minimize errors caused by these internal voltage drops, you should only measure currents less than  $200\ \mu\text{A}$ . This will keep the voltage drop on the ESD protection resistor less than  $60\ \text{mV}$ . Higher currents will not cause damage to the chip, but they will result in inaccurate measurements in this lab (i.e., the internal  $V_{GS}$  will be significantly less than the  $V_{GS}$  you apply at the pins).

### Experiment 1: Measuring I-V curves of an nFET

**Procedure:** Before you begin make sure that the machines are powered on. The power switch is located on the front in the lower right. To log on to the machine wait for the login prompt and enter:

Username: kiuser

Password:

Note that there is no password; just enter the username and hit enter. Once you are logged into the machine the Keithley Interactive Test Environment (KITE) should automatically start. If it does not, simply click on the icon labeled KITE.

Verify that the open project is the “Advanced IC Lab” project. It will say this in the ‘project view’ in the window on the left side of the screen. If this is not the open project, click on File -> Open project and open the project file in `C:S4200\kiuser\projects\ECE6721_Lab1\`

**You should immediately save the project to a different file name (something specific to you and your partner) so any changes you make do not affect ECE6721\_Lab1.**

Once the project is open you should see a graphical representation of an nMOS transistor in the main window. If this is not the case, double click on the nMOS interactive test module (ITM) at the top of the project tree or click the definitions tab at the top of the main window. The project tree is located in the left-most window.

Now you need to make sure that the 4200 is configured properly to run the required test. In the main window you should be looking at a schematic symbol of an nMOS transistor. You will also see three boxes with lines drawn from them to the various terminals of the transistor. These boxes will be labeled “drain”, “gate”, and “source.”

Use the pull-down menu in the box that is labeled drain and select SMU1 (SMU stands for Source-Measure Unit). Now click on the “Force Measure” button. This button is located directly below the pull-down menu. A window should pop up. This is where you define the function of each probe. For the drain of the transistor you should set a DC voltage of 5.0V and at the same time measure the current Id.

To do this set the “Forcing Function” to Voltage Bias. This is done by using the pull-down menu. Now fill in the rest of the fields: the level should be set to the voltage at which you want to hold the drain (5.0 V). The compliance is the maximum current that the 4200 will allow to flow through the device. Set it to something reasonable, perhaps 10 mA. At the bottom of the window you will see a section called “Measuring Options”. Check the current box to measure current and the range to auto. Click OK.

You have set up SMU1 to supply 5.0 V to the drain and measure and record the drain current. We will now do the same thing for the gate of the transistor.

In the box that is labeled “gate” select SMU2. Again click on the “Forcing Measure” button. Instead of supplying a steady DC voltage to the gate, we want to sweep the gate from 0 V to some higher voltage. This is done by selecting “Voltage Sweep” for the forcing function. Set the sweep type to linear, the start voltage to 0 V, the stop voltage to 1.3 V, and the step to 0.01 V or less. The reason that we stop at 1.3 V is because we are only interested in currents less than 200  $\mu$ A since the protection resistors on the chip reduce our measurement accuracy at higher currents. The source range should be set to best fixed and the compliance to something low. After all, we are driving the gate of a MOSFET, so there should be zero current flow. Under measure options check the voltage box and select measured instead of programmed for the type of measurement.

Lastly you need to configure the source node. Because the source is going to be at ground this is done a little bit differently. In the box labeled source, select GNDU from the pull down menu. There is nothing to configure under the “Force Measure” button.

Now that everything is configured click the save button at the top of the screen, or go to File -> Save. Now it is time to connect your circuit. The four probes are labeled SMU1, SMU2, SMU3, and GNDU. Connect SMU1 to pin 35, the drain pin. Connect SMU2 to the gate, pin 32. Leave SMU3 unconnected. Finally connect the GNDU probe to pin 34, the source. It is important to make sure that the source of the transistor is connected to both GNDU *and* to the GND terminal of your power supply. This allows the 4200 to have the same reference as the power supply and is important for accurate measurements.

There is a field labeled 'Speed' located directly above the box labeled 'drain'. Make sure that 'Quiet' is selected from the pull down menu for the most accurate low-current measurements.

Once everything is connected properly and the power supply is turned on, click the green play button at the top of the screen. This starts the measurement. You can click the red stop button at any time to stop the currently running measurement. You can tell when the 4200 is finished taking the measurement when the red stop button is grayed out, or when the status window at the bottom reads:

“Stop execution...  
Total Execution time...”

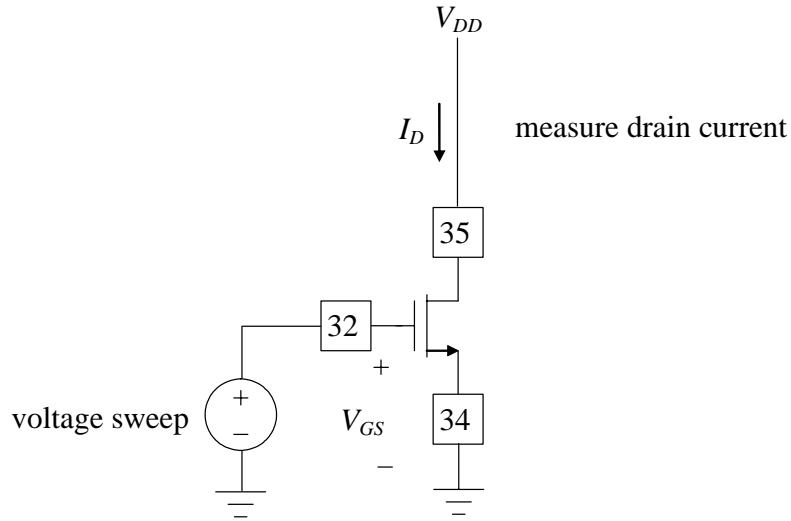
To view a plot of the data just measured click on the graph tab at the top of the main window. Now right click anywhere in the graph and select “Define Graph.” You should see a window with all of the data measured down one side and the X, Y1, and Y2 axis along the top. Click the box at the intersection of GateV and X. This sets the X axis to be the swept Gate voltage. Now set the Y1 axis to DrainI. Click OK.

Right click again on the plot and select axis properties. In this window there are three tabs at the top of the window. Select the Y1 tab and check the Log box. This will set the Y1 axis to a log axis and allow you to see the exponential behavior of the drain current. Click OK.

Right click on the graph once again and select auto scale. You should now see a plot of your drain current vs. gate voltage.

In order to save your data for later use in MATLAB, click the “sheet” tab at the top of the main window. This shows all of the data values taken by the 4200 when running the measurement. Insert a 3.5 inch floppy drive into the disk drive and click on the “save as...” button. You can save your data in .xls, .txt, or .csv format. If you save in csv (comma-separated values) format, you can directly load the data into MATLAB (e.g., “load mydata.csv”).

(a)  $I_D$  vs.  $V_{GS}$ . We have just measured the effect of the gate-to-source voltage on drain current. The experimental configuration is summarized below:



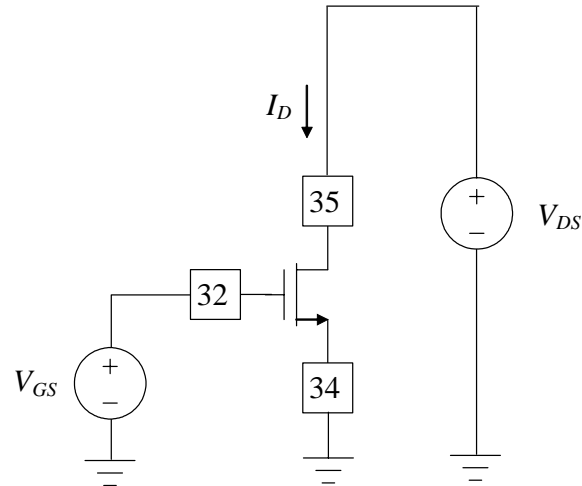
Plot your data in MATLAB, making sure to label your  $x$  and  $y$  axes (with units). **See the handout on plotting experimental data for examples of how data should be plotted in this class.**

Make two plots: one using the “plot” command and one using the “semilogy” command to create a logarithmic current axis. In both plots, plot the data using circles. For example:

```
plot(vgs, id, 'o');
semilogy(vgs, id, 'o');
```

In the first (linear) plot, you should observe the current increasing as the square of gate voltage, as described by equation 1.67 in Johns & Martin (and shown graphically on page 47 on the *Introduction to MOSFET Operation* supplementary notes). The second (semi-logarithmic) plot is useful for identifying the exponential current-voltage relationship that appears in the subthreshold region. In semilog plots, exponentials appear as straight lines. You should observe a straight line at very low current levels.

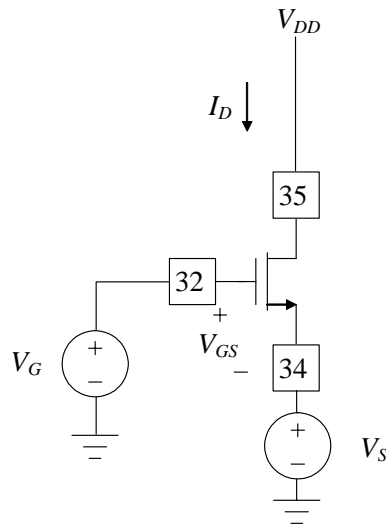
(b)  $I_D$  vs.  $V_{DS}$ . We will now measure the effect of drain voltage on drain current. The figure below shows our experimental configuration. In the 4200 KITE project tree, go to the next interactive test module (ITM), called “nMOS\_Vds\_sweep,” or something similar. You will modify this ITM to perform this experiment.



Using your data from part (a), note the gate voltage that gave a drain current of about 200  $\mu\text{A}$ . Set this gate voltage as a “bias voltage” using SMU2. We now wish to sweep the drain voltage from zero to +5.0 V while measuring drain current. Use SMU1 to generate the dc drain voltage.

Sweep  $V_{DS}$  from zero to 5.0 V in at least 100 steps. Record the drain current at each point. After observing the data on the 4200 graph, move the data into MATLAB and plot  $I_D$  vs.  $V_{DS}$  on linear axes (i.e., use ‘plot’). As before, label your axes with units. You should observe a curve similar to that in Figure 1.14 or 1.16 in Johns & Martin (and on page 49 on the *Introduction to MOSFET Operation* supplementary notes). Do you see a triode region and an active region? Does the transition from one region to the other occur where it should?

(c)  $I_D$  vs.  $V_S$ . We will now measure the effect of source voltage on drain current. Look at the next ITM for the general setup. Here is the configuration we will use:



First, you will need to take the GNDU connection from the 4200 off of pin 34, and connect SMU3 to pin 34, since we will change the source voltage of the transistor. Connect the GNDU line to the “ground” provided by the power supply.

Tie the drain to  $V_{DD} = 5.0$  V using a bias voltage on SMU1. Set the gate voltage to 3.0 V using SMU2, and tie the source (pin 34) to SMU3, which you will sweep.

Sweep the source voltage from 0 V ( $V_{GS} = 3$  V) to 3 V ( $V_{GS} = 0$  V), and then note the source voltage that gives a drain current around 200  $\mu$ A. Now repeat the test with a restricted range of source voltages that keep the current below 200  $\mu$ A.

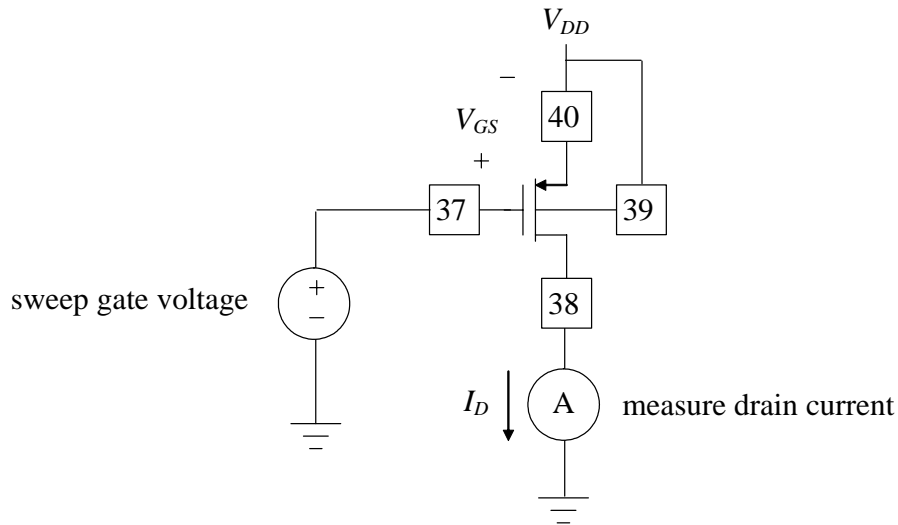
In MATLAB, plot  $I_D$  vs.  $V_{GS}$  ( $V_{GS} = 3.0$  V  $- V_S$ ) data from this experiment *and* the data from part (a) on the same graph using with linear axes (“plot”) and a logarithmic y axis (“semilogy”). How do the data differ? Why are they different?

### Experiment 2: Measuring I-V curves of a pFET

We will now repeat the measurements made in experiment 1 (a) and (b) on a pMOS transistor. When using pFETs, it is important to remember that the gate and drain should always be negative *with respect to the source*, which is often tied to  $V_{DD}$ . (This does *not* mean that the gate and drain voltages will be negative *with respect to ground*; this should not happen!) For all these experiments, you should connect GNDU to  $V_{DD}$ , and use only *negative* voltages on the 4200, but make sure to keep voltages in the range of 0 V to -5 V.

Drain currents will be negative for pMOS devices, but it is fine to plot everything with positive currents since only the direction of current flow has changed. It is important to remember the negative numbers cannot be plotted on a logarithmic axis, so to create semilog plots, you must plot the absolute value of current.

(a)  $I_D$  vs.  $V_{GS}$ . We will begin by measuring the effect of the gate-to-source voltage on drain current. The next ITM should be set up for this experiment. The experimental configuration is summarized below:



Please note that the diagram of the  $p$ FET on the Keithley 4200 is upside-down, with the source drawn at the bottom of the screen.

Wire the well of the  $p$ FET to  $V_{DD}$ . Set the source bias voltage (SMU3) to 0 V, which will put the source at 0 V relative to GNDU; in other words, the source will be at  $V_{DD}$ . Tie the drain (pin 38) to SMU1, which should be set to -5 V. This sets up  $V_{DS} = -5.0$  V. Set up SMU2 to supply the gate voltage to the  $p$ FET (pin 37). **You should keep the output of the SMUs between 0 and -5 V at all times.**

Now repeat the measurements of 1(a), using negative gate-to-source voltages. You should refine the find the upper current limit (200  $\mu$ A), as the  $p$ FET will have a different current-to-voltage relationship. Take a measurement of  $I_D$  vs.  $V_{GS}$  for currents up to 200  $\mu$ A. Make sure you have at least 100 data points.

(b)  $I_D$  vs.  $V_{DS}$ . We will now measure the effect of drain voltage on drain current. The next ITM is roughly set up to do this measurement.

Set the gate voltage so that a current of around 200  $\mu$ A appears in saturation (active) region. Repeat the measurements of 1(b) on the  $p$ FET, using negative drain-to-source voltages. (Sweep  $V_{DS}$  from 0 V to -5 V.)

## **REPORT**

Each lab group (two students) should submit a lab report that is separate from the lab notebook. (In this class, lab notebooks will not be turned in.) The report should be typed, not handwritten, although it is acceptable to add neat handwritten notes to figures

where appropriate (e.g., to label different curves). Lab reports are due in your lab section one week after a two-week lab ends.

Begin your lab report with a title page containing your names, email addresses, T.A., lab section, and the title of the lab. Next, write one or two paragraphs outlining the overall goal of the lab. Describe how you performed each experiment, listing any problems you encountered and how you overcame them. Figures are preferably included in line with the text. You should number the figures and refer to them from the text.

- Every sentence labeled with a “bullet” like this indicates either a figure you should include or an answer you should explicitly provide in your report.

The grading for Lab 1 will be as follows:

MATLAB Plots (21):	3 points each
Answers (14):	1 point each
Circuit parameter table:	3 points
Introduction and conclusion:	7 points
Format, flow, and coherency:	7 points
<u>Spelling, grammar, neatness:</u>	<u>6 points</u>
Total:	100 points

Extra credit: 5 points

Before beginning this report, you should perform the MATLAB curve fitting exercise available on the course website. This will teach you how to use the `polyfit` command to fit straight lines to data.

Your lab report should contain the following sections:

### Experiment 1: nFET characterization

Part (a):  $I_D$  vs.  $V_{GS}$

We will first determine the threshold voltage of the nFET using a simple technique. Since our  $V_{DS}$  was very high (5.0 V) in this experiment, we can assume that the transistor was in the active (saturation) region. In saturation, the drain current of a MOSFET is given by

$$I_D = \frac{1}{2} \mu_n C'_{ox} \frac{W}{L} (V_{GS} - V_T)^2 \quad (1)$$

for  $V_{GS} > V_T$ . For  $V_{GS} < V_T$ ,  $I_D = 0$ .

Taking the square root of both sides, we get

$$\sqrt{I_D} = \sqrt{\frac{1}{2} \mu_n C_{ox}' \frac{W}{L}} \cdot (V_{GS} - V_T) \quad (2)$$

This means that if we plot the square root of  $I_D$  vs.  $V_{GS}$ , we will get a straight line, and our  $x$  intercept will be the threshold voltage  $V_T$ .

Plot the square root of  $I_D$  vs.  $V_{GS}$  in MATLAB. For example:

```
idsqrt = sqrt(id);
plot(vgs, idsqrt, 'o');
```

You should observe that *part* of this curve (the part that is above threshold) is a straight line with a positive slope. Use `polyfit` to fit a straight line to the appropriate part of this curve. Do not use `polyfit` on the entire curve, since it deviates from straight-line behavior at near the threshold voltage. In many parts of this (and later) assignments, you will have you use your judgment to determine which subset of a dataset to use for a particular theoretical fit.

- Include a plot of the square root of  $I_D$  vs.  $V_{GS}$ , with a linear fit to the above threshold region. On the plot, label (by hand, if you wish) the threshold voltage; that is, the point where the linear fit crosses the  $x$  axis. Also label the slope. *Remember to label axes and plot measured data as discrete points and theoretical fits as continuous lines! Refer to the plotting handout to see what we expect in each plot!*

Now we have a good estimate of  $V_T$ . From the slope of this line, you should be able to calculate the electron mobility  $\mu_n$ . Remember, the  $W/L$  ratio of this transistor is given on the chip pin-out diagram, and the oxide thickness is also given in the Lab 1 Assignment. (You will first need to calculate the oxide capacitance per unit area  $C_{ox}'$ . Make sure to use the dielectric constant of silicon dioxide, *not* silicon.)

- What is the effective electron mobility in this process? Make sure you use units of  $\text{cm}^2/\text{V}\cdot\text{s}$ .
- An important parameter in circuit design is the product of mobility and oxide capacitance,  $\mu_n C_{ox}'$ , which has units usually expressed as  $\mu\text{A}/\text{V}^2$ . Compute this parameter for this CMOS process.

Now let's do away with the square root and just plot  $I_D$  vs.  $V_{GS}$ .

- Include a plot of  $I_D$  vs.  $V_{GS}$ , with the theoretical fit to equation (1) (for  $V_{GS} > V_T$  only).

Does the fit look good? You may need to adjust the fit parameters ( $V_T$  and  $\mu_n$ ) a bit to achieve the best fit. If you change these values for this plot, report the new values.

Now that we have determined parameters for the above threshold region of operation, we will explore the subthreshold current. You have noticed that the drain current does not go

exactly to zero below threshold. It turns out that in the subthreshold region, current decreases exponentially. The easiest way to identify exponentials is to plot them on a semilogarithmic graph. Use the `semilogy` command to plot  $I_D$  vs.  $V_{GS}$  with a logarithmic y axis. You should see a region at very low current levels where the data points fall in a straight line.

The drain current below threshold obeys the following equation:

$$I_D = I_0 \frac{W}{L} \exp\left(\frac{\kappa V_G - V_S}{U_T}\right) \quad (3)$$

where  $I_0$  is a process-dependant constant with units of current, and  $\kappa$  (kappa) is a unitless constant that typically ranges between 0.6 and 0.9 for different CMOS processes. Note that  $U_T$  is the thermal voltage  $kT/q$ , which is approximately 26 mV at room temperature.

- Include a `semilogy` plot of  $I_D$  vs.  $V_{GS}$ , with the theoretical fit to equation (3). This fit should appear as a straight line, and will probably only fit your first 5-8 data points, where subthreshold operation occurs.
- What values of  $I_0$  and  $\kappa$  do you get?
- Now repeat the previous `semilogy` plot with the fit to (3), but also include your fit to equation (1) using the parameters from the previous plots.

You should observe that the subthreshold (weak inversion) and above threshold (strong inversion) equations do a good job fitting the data in their respective regions, but a poor job of fitting in the other region. Also notice there is an intermediate region, corresponding to *moderate inversion*, that *neither* equation predicts with great precision.

In 1995, Enz, Krummenacher and Vittoz proposed a relatively simple MOSFET model valid in *all* regions of operation: weak, moderate, and strong inversion. This has come to be known as the EKV model. Their basic equation for drain current (in saturation) is given by

$$I_D = I_S \cdot \left[ \ln \left( 1 + \exp \left[ \frac{\kappa(V_G - V_T) - V_S}{2U_T} \right] \right) \right]^2 \quad (4)$$

where

$$I_S = \frac{2\mu_n C'_{ox} U_T^2}{\kappa} \cdot \frac{W}{L} \quad (5)$$

- Include a `semilogy` plot of  $I_D$  vs.  $V_{GS}$ , with a theoretical fit to the EKV model. In order to get a good fit, you may have to use different values of  $\kappa$ ,  $\mu_n$ , and  $V_T$  than the values used in previous plots. Report the values used in this plot.
- What is the value of  $I_S$  for this transistor? This is called that *moderate inversion characteristic current*, and is a good indication of the approximate boundary between

strong and weak inversion for a transistor having a particular  $W/L$  ratio. (Note: This parameter is unrelated to the  $I_S$  used in bipolar transistor equations.)

You should observe a very close fit to the measured data using the EKV model. For example, see the second figure in the plotting handout.

We will now investigate the transconductance  $g_m$  of this transistor. Transconductance is the most important small-signal parameter for MOSFETs, and its value often determines the gain or bandwidth of a circuit. Transconductance is defined as

$$g_m \equiv \frac{\partial I_D}{\partial V_{GS}} \quad (6)$$

We can approximate  $g_m$  as  $\Delta I_D / \Delta V_{GS}$  for small increments in gate voltage. The `diff` command in MATLAB (type “`help diff`” for more information) is useful for this type of analysis.

Use `diff` on your current measurement vector to create a  $\Delta I_D$  vector. Now divide this by the quantity  $\Delta V_{GS}$ , which is the voltage step you used to take your measurements. Now you have a vector with measured transconductance values.

In strong inversion (above threshold),  $g_m$  is given by

$$g_m = \sqrt{2\mu C'_{ox} \frac{W}{L} I_D} \quad (7)$$

- Plot your measured  $g_m$  vs.  $I_D$  using `semilogx` so the  $x$  axis ( $I_D$ ) is logarithmic. Make sure to label both axes with the appropriate units. Include a fit to equation (7).

In weak inversion (below threshold),  $g_m$  is

$$g_m = \frac{\kappa I_D}{U_T} \quad (8)$$

- Include another `semilogx` plot of your measured  $g_m$  vs.  $I_D$ , but this time include a fit (over the appropriate range) to equation (8).

An good expression for  $g_m$  valid in *all* regions of inversion has been proposed by Enz and colleagues, and is given by

$$g_m = \frac{\kappa I_D}{U_T} \cdot G'(I_D) \quad (9)$$

where

$$G'(I_D) = \frac{2}{1 + \sqrt{1 + 4(I_D/I_S)}} \quad (10)$$

[Remember,  $I_S$  comes from equation (5).]

- Include one more `semilogx` plot of your measured  $g_m$  vs.  $I_D$ , but this time include a fit to equation (10). Does this expression fit the entire range of  $g_m$  values from weak inversion to strong inversion?

Part (b):  $I_D$  vs.  $V_{DS}$

After plotting  $I_D$  vs.  $V_{DS}$  (both axes linear, not logarithmic), you should observe two regions: the triode region and the active (saturation) region where the transistor approximates a constant current source.

- What determines the boundary between these two regions? In your data, does the boundary occur in the position you expect?
- Include a plot of  $I_D$  vs.  $V_{DS}$ , and label the boundary between triode and active regions.

Drain current in the triode region is described by

$$I_D = \mu_n C'_{ox} \frac{W}{L} \left[ (V_{GS} - V_T) V_{DS} - \frac{1}{2} V_{DS}^2 \right] \quad (11)$$

Drain current in the active region is almost constant, but due to channel length modulation, the current increases slightly with  $V_{DS}$ . This compliance is described by

$$I_D = I_{Dsat} \cdot \left( 1 + \frac{V_{DS}}{V_A} \right) \quad (12)$$

where  $I_{Dsat}$  is the saturation current, and  $V_A$  is the Early voltage, which has units of volts. Typical values of Early voltage in MOSFETs range from 10 V to 200 V depending on the length of the device. Since long devices are less affected by channel-length modulation, they have higher Early voltages. (In an ideal MOSFET, the Early voltage would be infinite.) Note that the Johns and Martin textbook uses the channel length modulation coefficient  $\lambda$  instead, where  $\lambda = 1/V_A$ . In this lab, we will be talking in terms of Early voltage.

If we fit a straight line to the data in the active region, the Early voltage will be the negative of the  $x$  intercept.

- Include a another plot of  $I_D$  vs.  $V_{DS}$ , with fits to both the triode region using equation (11) and a straight-line fit to the active region.
- What is the Early voltage  $V_A$  of this transistor?

Part (c):  $I_D$  vs.  $V_S$

We will now investigate the body effect.

- Plot  $I_D$  vs.  $V_{GS}$  ( $V_{GS} = 3.0 \text{ V} - V_S$ ) data from this experiment *and* the data from part (a) on the same graph using with linear axes. You should notice that the effective threshold voltage is very different for the two data sets. Estimate the threshold voltage for the part (c) data and indicate it on the plot.
- What was the value of  $V_{SB}$  at this threshold? (Remember, the bulk is at ground.)

Take your threshold voltage from part (a) to be  $V_{T0}$ , and your threshold voltage from part (c) to be  $V_T$ .

- Given the following equation, calculate  $\gamma$  (gamma), assuming  $\Phi_F = 0.4 \text{ V}$  for this process.

$$V_T = V_{T0} + \gamma \left( \sqrt{|2\Phi_F| + V_{SB}} - \sqrt{|2\Phi_F|} \right) \quad (13)$$

Use the value of  $V_{SB}$  at the observed threshold.

## Experiment 2: pFET characterization

Repeat the plots, calculations, and analysis from Experiment 1 (a) and (b) for the pFET data. All your values for  $V_{GS}$  and  $V_{DS}$  in the pFET experiments should be *negative* voltages. However, to make things easier use the *absolute value* of  $V_{GS}$  and  $V_{DS}$  values so that your plots do not use negative axes. If you use positive numbers for  $V_{GS}$ ,  $V_{DS}$ , and  $I_D$  values, you should be able to repeat the fits using the same equations and MATLAB routines you used for the nFET experiments.

### Circuit Parameter Table

You have now extracted the most important first-order parameters of MOSFET operation in this 0.5- $\mu\text{m}$  CMOS process. At the end of your report, provide a table summarizing the results of your theoretical fits. If you got slightly different values for a parameter using different fits, you may chose to report all the values, an average, or the one you believe the most. Don't forget to include units in your table!

parameter	nMOS	pMOS
$V_{t0}$		
$\mu C_{ox}'$		
$\kappa$		
$\gamma$		(we didn't measure this)
$V_A$ for $L = 2 \mu\text{m}$		

### Extra Credit

For extra credit, you may repeat Experiment 1(c) for the pFET transistor, and use this data to estimate  $\gamma_p$  to complete your table above. Include the appropriate plot of your data.