UNIVERSITY OF UTAH
ELECTRICAL AND COMPUTER ENGINEERING DEPARTMENT

ANALOG INTEGRATED CIRCUITS LAB

LAB 4
Differential Pairs and Differential Amplifiers

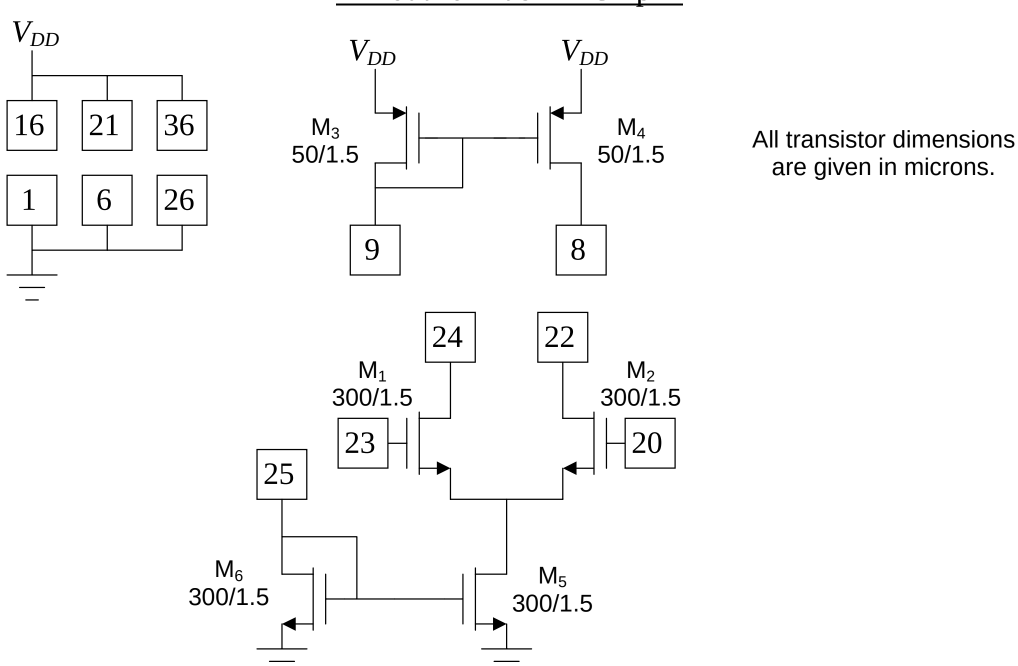
Objective: In this lab, you will characterize the differential pair and use this subcircuit to construct differential amplifiers. You should review section 3.8 in Johns & Martin.

Power: We will be using a single-polarity power supply for this lab. Connect pins 1, 6, and 26 to ground. Connect pins 16, 21, and 36 to V_{DD} = 5.0 V. (Use the +25V power supply for V_{DD}). Leave these power connections in place for all experiments.

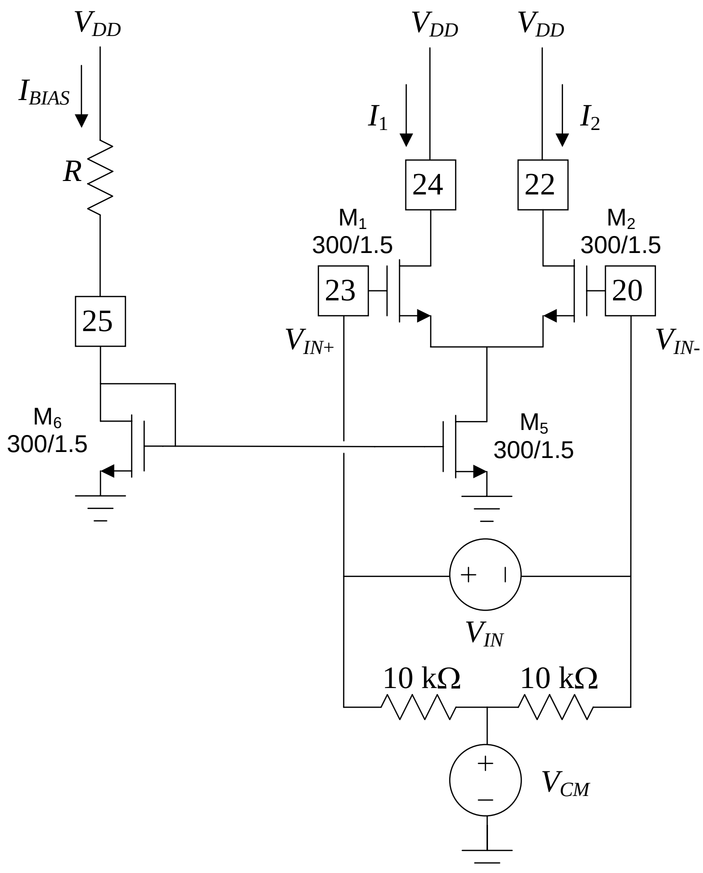
Experiment 1: The Differential Pair and Differential Amplifiers

The following figure shows the subcircuits on Chip A that we will use for this characterization of the differential pair. **Be sure to connect pins 1, 6, and 26 to ground, and pins 16, 21, and 36 to V_{DD} (5.0 V) for all the experiments in this assignment.**

Pin-out for Lab 4 – Chip A



(a) *I*-*V* characterization of *n*MOS differential pair. Connect the circuit shown below. Using the technique from the previous lab, find a value for *R* that results in a bias current I_{BIAS} of close to 200 μA. Record this value of V_{GS6} along with the exact value of I_{BIAS}. You should use the HP function generator for the differential voltage source V_{IN} (remember to set it to HIGH-Z load mode!) and the 6-V power supply for the common-mode voltage source V_{CM}.



We are using two 10-kΩ resistors in combination with the two voltage sources to create an input network that allows us to control differential input voltage $V_{IN} = V_{IN+} - V_{IN-}$ and common-mode input voltage $V_{CM} = (V_{IN+} + V_{IN-})/2$ independently.

- As an exercise, solve for V_{IN+} and V_{IN-} for the case where V_{CM} = 2.5 V and V_{IN} = +0.2 V. Show (in your lab report) that this network works as expected. Now set your voltage sources to these values and measure V_{IN+} and V_{IN-}. Does the input network behave properly?

Note that if we set V_{IN} too high (or too low if V_{IN} is negative) for a given V_{CM}, we can make the inputs go below ground or above V_{DD}. During this lab, take care not to do this, as this may damage the chip. Every time you plan a sweep of V_{IN}, calculate the extreme values of V_{IN+} and V_{IN-} (given your value of V_{CM}) to make sure they stay within the power supply rails.

Now, with V_{CM} = 2.5 V and I_{BIAS} = 200 μA, sweep V_{IN} from –0.3 V to +0.3V in 20 mV increments. Record I_1 and I_2 at each step. (You may wish to measure this currents using two separate sweeps if you don't have access to two ammeters.)

- On the same graph, plot I_1 vs. V_{IN} and I_2 vs. V_{IN}. Include fits to the following expressions for differential pair current:

$$I_1 = \frac{I_{BIAS}}{2} + \sqrt{\mu C_{ox}^{'} \frac{W}{L} I_{BIAS}} \cdot \left(\frac{V_{IN}}{2}\right) \cdot \sqrt{1 - \frac{(V_{IN}/2)^2}{\left(I_{BIAS} / \mu C_{ox}^{'}[W/L]\right)}}$$

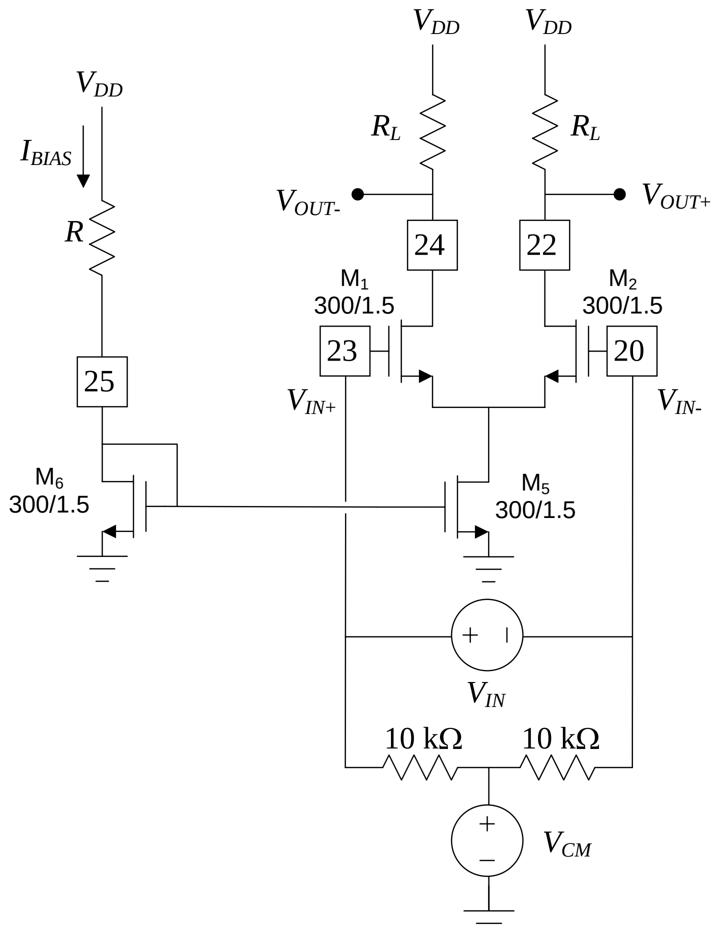
$$I_2 = \frac{I_{BIAS}}{2} - \sqrt{\mu C_{ox}^{'} \frac{W}{L} I_{BIAS}} \cdot \left(\frac{V_{IN}}{2}\right) \cdot \sqrt{1 - \frac{(V_{IN}/2)^2}{\left(I_{BIAS} / \mu C_{ox}^{'}[W/L]\right)}}$$

Now set V_{IN} = 0 and sweep V_{CM} from 1.0 V to 4.0 V in 0.5 V increments, measuring I_1 and I_2 at each step. "Ideally", the current should be completely independent of the common-mode voltage, but in practice this is not the case.

- What happens to I_1 and I_2 as V_{CM} increases? Why does this happen? Include a plot of this data in your report.

(b) Differential pair with resistive load. Add load resistors R_L = 10 kΩ to the differential pair as shown in the figure below. (I_{BIAS} should still be 200 µA.)

- Calculate the expected g_m of M_1 and M_2, and use this to calculate the expected gain of this circuit for the case where we measure the output differentially (i.e., $V_{OUT} = V_{OUT+} - V_{OUT-}$). (Include this calculation in your lab report.)



Now set V_{CM} to 2.5 V and V_{IN} to zero.

- In this case, what would you expect the dc level of V_{OUT+} and V_{OUT-} to be? Write an expression for this that uses V_{DD}, R_L, and I_{BIAS}. Now measure the voltages at the two outputs. Do they match your calculations?

Now sweep V_{IN} from –0.2 V to +0.2V in 10 mV increments. Record V_{OUT+} and V_{OUT-} at each step.

- Plot both of these output voltages vs. V_{IN} on the same graph. Fit lines to the linear part of the curves, and from the slope of these lines, extract the single-ended gain for each output.
- Now plot the differential output voltage V_{OUT} vs. V_{IN} on a separate graph. Include a fit to the linear region, and find the gain. Does this gain match the theoretical gain you calculated earlier? From your measured gain, calculate g_{m1}.

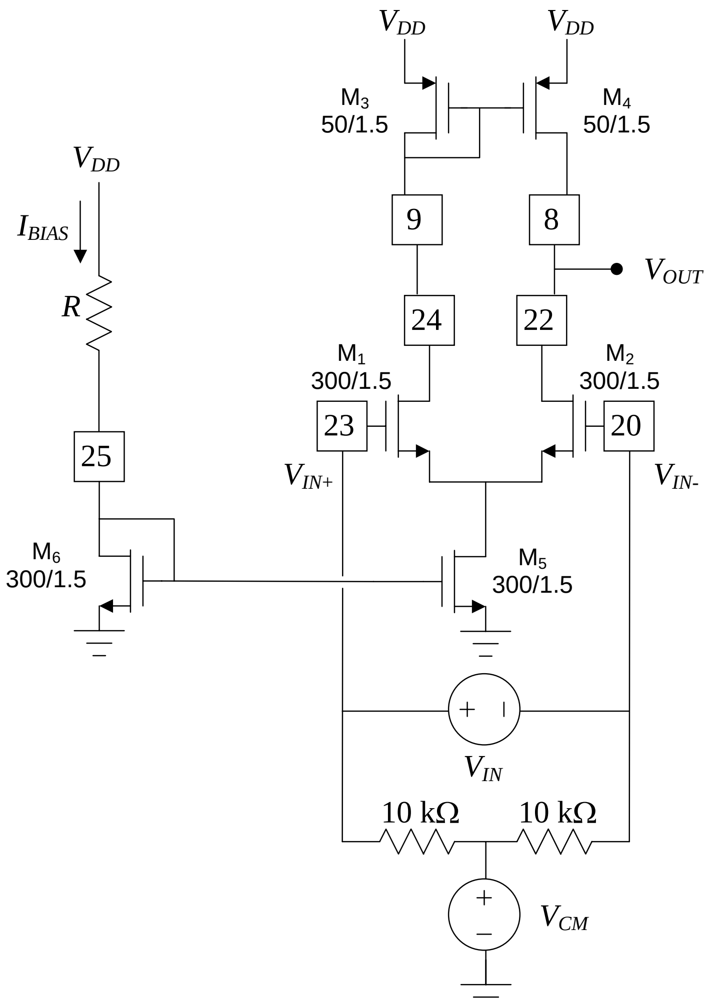
Now set V_{IN} = 0 and sweep V_{CM} from 1.0 V to 4.0 V in 0.25 V increments, measuring the differential output voltage $V_{OUT} = V_{OUT+} - V_{OUT-}$ at each step.

- Plot V_{OUT} vs. V_{CM}, and fit a straight line to the data. What is the common-mode gain? Note that ideally, the common-mode gain is zero. In this circuit, a non-zero common-mode gain is caused by mismatch between the two R_L resistors. Add a 1-kΩ resistor in series with *one* of your load resistors to create an effective R_L of 11 kΩ on one side of the circuit.
- Repeat the common-mode gain measurements. Is the common-mode gain you measured consistent with the imbalance in R_L?

Let's calculate the common-mode rejection ratio (CMRR) of this amplifier with mismatched load resistors. CMRR is defined as differential gain divided by common-mode gain, and is usually expressed in dB. Since we want common-mode gain to be as low as possible, a large CMRR is better than a small CMRR. Most "general purpose" amplifiers have a CMRR of greater than 60 dB.

- What is yours? How does the 10% mismatch in load resistors degrade CMRR?

(c) Differential pair with active load. We will now connect a *p*MOS current mirror as an active load for our *n*MOS current mirror as shown in the figure below.



Now set V_{CM} = 2.5 V and adjust V_{IN} until the output voltage V_{OUT} is close to 2.5 V. We will consider 2.5 V to be our "zero" output since it is halfway between the power supply rails.

- What value of V_{IN} is required to produce this output? This is the *input offset voltage* V_{OS} of the amplifier. Now change V_{IN} and see how high and how low V_{OUT} will go.
- What determines the minimum value of V_{OUT}? Change the common-mode voltage and describe what effect V_{CM} has on V_{OUTmin}.

Now make sure you set V_{CM} back to 2.5 V, and sweep V_{IN} from –0.15 V to + 0.15 V in increments of 10 mV while measuring V_{OUT}. You should observe a region of very high gain surrounded by two low-gain regions.

- Include a plot; no fit is necessary. Give estimates of V_{OUTmin} and V_{OUTmax} that define the high-gain region. What limits the high-gain region to this range?

Now we wish to "zoom in" on the high gain region, taking more data points so we can fit a line to estimate the gain reliably. Take 10-15 data points in this high-gain region. You should take enough data points to measure the gain accurately. You will probably have to vary V_{IN} in 1-mV steps since the output will change very rapidly.

- Plot V_{OUT} vs. V_{IN} and fit a straight line to the data. What is the measured gain?
- Write an expression for the theoretical gain of this amplifier. Assuming M_2 and M_4 have the same Early voltage V_A, calculate the Early voltage from your measured gain and your previously-measured value of g_{m1}. Based on your previous experience with this CMOS process, does your value for V_A seem reasonable for devices having a length of 1.5 μm?

Now set V_{IN} to some value that puts the output in the high-gain region. Sweep V_{CM} from 2.0 to 3.0 V in increments of 0.1 V and measure the output voltage to derive the common-mode gain.

- Include a plot of V_{OUT} vs. V_{CM} with a fit for the gain. What is the CMRR of this amplifier?

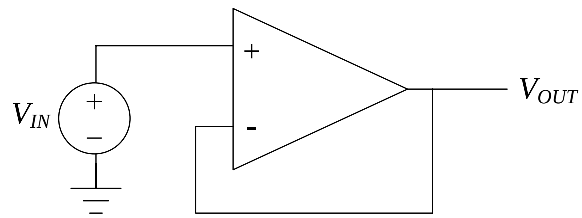
(d) Comparison. Suppose we wanted to build a differential pair with resistive load [as in part (b)] having the same gain as the active-load amplifier from part (c).

- What value of R_L would we need to use to get this gain? Using I_{BIAS} = 200 μA, what would the dc level of V_{OUT+} and V_{OUT-} be in this case? Would the amplifier work properly? What changes could we make to achieve this gain with a resistive load? Discuss the advantages of using an active load.

Experiment 2: Single-Stage Op-Amp

In this experiment, we will continue to use the differential pair with active load from Experiment 1(c) as a single-stage op-amp. Make sure you use a bias current of 200 μA. Disconnect the input network that we used to set V_{IN} and V_{CM}.

(a) Unity-gain buffer. Connect the single-stage op-amp as a unity-gain buffer as shown in the figure below.



Sweep V_{IN} from 0 to 5 V in increments of 0.1 V and measure V_{OUT}.

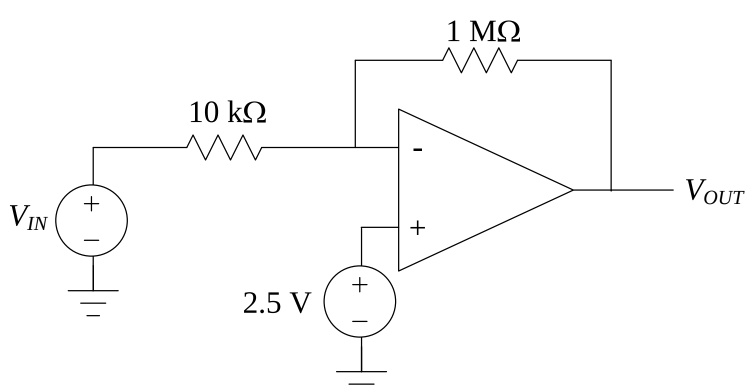
- Does the circuit act as a unity-gain amplifier? Over what range? Include a plot with a fit to the appropriate region. What is the gain over this region? The ideal gain A_f of this circuit is:

$$A_f = \frac{A}{1 + A\beta}$$

The feedback network gain β in this circuit is one, because the output is directly fed back to the input. You measured A in Experiment 1, part (c). How does your measured gain compare with the gain predicted by this equation.

- Does a single-stage op-amp make a good unity-gain buffer? Why or why not?

(b) Inverting amplifier. Connect the single-stage op-amp as an inverting amplifier as shown in the figure below.



We will be using a 2.5-V voltage source as a “virtual ground” halfway between our power supply rails. We will refer all voltages to this level.

- What is the gain of this circuit if we use an ideal op-amp? For this circuit, $\beta = 0.01$. What do you expect the closed-loop gain A_f to be given the gain A of our single-stage op-amp?

Sweep V_{IN} from 2.48 V to 2.52 V in 1-mV increments, and measure V_{OUT}. Note that we are sweeping the input voltage from –0.02 V to +0.02 V relative to our virtual ground.

- Plot V_{OUT} (referred to virtual ground) vs. V_{IN} (referred to virtual ground) and include a fit. What is the gain of this amplifier? How does this compare with your predictions? Does a single-stage op-amp make a good "gain-of-100" amplifier? Why or why not?

EXTRA CREDIT

For extra credit, reduce the bias current I_{BIAS} to 100 μA and repeat the differential gain measurements (V_{OUT} vs. V_{IN}) on the amplifiers from parts 1(b) and 1(c). (You don't have to measure the common-mode gain.) Theoretically, how should the gain change in each circuit if the bias current is reduced by a factor of two? How do the measurements match theory?

REPORT

Each lab group (two students) should submit a lab report that is separate from the lab notebook. (In this class, lab notebooks will not be turned in). The report should be typed, not handwritten, although it is acceptable to add neat handwritten notes to figures where appropriate (e.g., to label different curves). Lab reports are due in your lab section one week after a two-week lab ends.

Begin your lab report with a title page containing your names, email addresses, T.A., lab section, and the title of the lab. Next, write one or two paragraphs outlining the overall goal of the lab. Describe how you performed each experiment, listing any problems you encountered and how you overcame them. Figures are preferably included in line with the text. You should number the figures and refer to them from the text.

- Every sentence labeled with a "bullet" like this indicates either a figure you should include or an answer you should explicitly provide in your report.

The grading for Lab 4 will be as follows:

MATLAB Plots (10):	5 points each
Answers (11):	3 points each
Introduction and conclusion:	4 points
Format and style:	3 points
Total:	90 points
Extra credit:	10 points

Your lab report should contain a description of all experiments performed, data plots (with fits) requested throughout this assignment, and a discussion of how the measured data (and fit parameters) compare with circuit theory.