

UNIVERSITY OF UTAH
ELECTRICAL AND COMPUTER ENGINEERING DEPARTMENT

ANALOG INTEGRATED CIRCUITS LAB

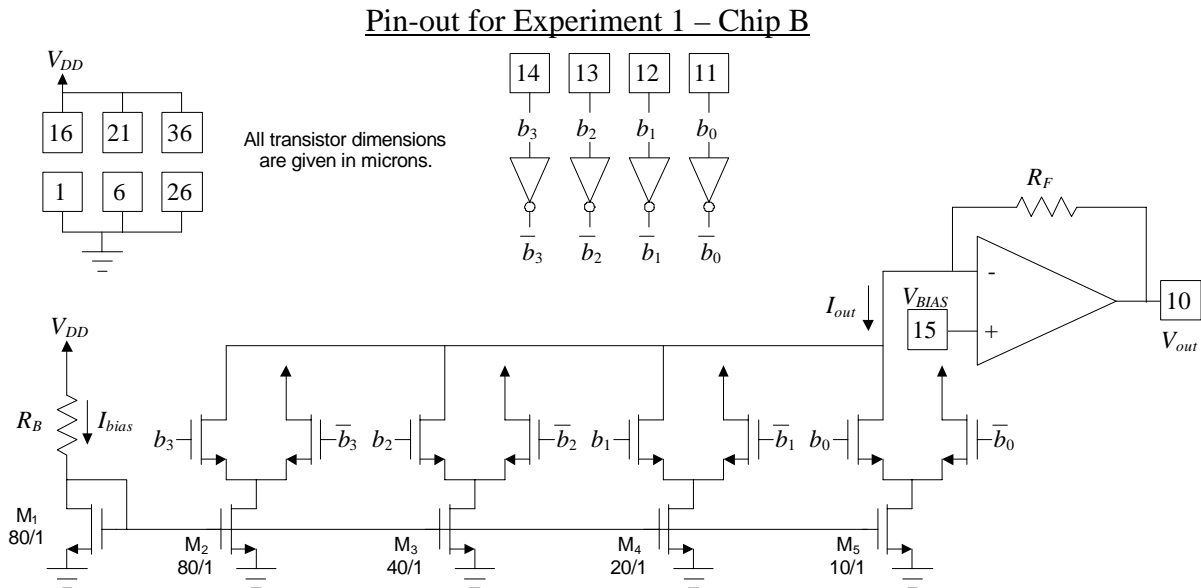
LAB 6
Data Converters

Objective: In this lab, you will characterize a 4-bit binary-weighted current-mode digital-to-analog converter (DAC) and a 3-bit flash analog-to-digital converter (ADC). You should read sections 11.1-11.5, 12.2 (with emphasis on Figure 12.13), and 13.4 in Johns & Martin.

Power: We will be using a single-polarity power supply for this lab. Connect pins 1, 6, and 26 of Chip B to ground. Connect pins 16, 21, and 36 of Chip B to $V_{DD} = 5.0$ V. (Use the +25V power supply for V_{DD}). Leave these power connections in place for all experiments.

Experiment 1: 4-Bit Binary-Weighted Current-Mode DAC

The following figure shows the circuit on Chip B that we will use for this characterization of the current-mode DAC. **Be sure to connect pins 1, 6, and 26 to ground, and pins 16, 21, and 36 to V_{DD} (+5.0 V) for all the experiments in this assignment.**



Set V_{BIAS} to +1.0 V. What do you expect the voltage to be at the negative input of the op-amp?

The resistors R_B and R_F are p^+ diffusion resistors – basically long thin strips of the highly-doped regions used in p MOS drains and sources. The resistance of p^+ diffusion in this process is approximately $103 \Omega/\text{square}$. R_B is $820 \mu\text{m}$ long and $4 \mu\text{m}$ wide. R_F is $204 \mu\text{m}$ long and $4 \mu\text{m}$ wide.

- Calculate the expected resistance of each resistor.
- Using the following process parameters, estimate the expected current through M_1 . Solving for the exact value is very difficult, so use the following technique to get an approximate answer: Choose a “reasonable” value for the gate voltage of M_1 (an educated guess), then calculate the current through the resistor given by this voltage. Now calculate the actual gate voltage M_1 would need to source this amount of current. Iterate these steps a few times until you get a reasonable estimate for I_{D1} . Use the process data given in the table below.

nMOS

$$V_{t0} = 0.62 \text{ V}$$

$$\mu_n C_{ox} = 40 \mu\text{A}/\text{V}^2$$

- Now calculate the expected drain currents for M_2 - M_5 . What will I_{out} and V_{out} be when b_0 - b_3 are tied to V_{DD} ? What will I_{out} and V_{out} be when b_0 - b_3 are tied to ground?

Now sweep the digital input from $B_{in} = 0000$ to $B_{in} = 1111$. Record V_{out} for all possible inputs.

- Plot V_{out} vs. B_{in} (which will vary from zero to 15), making sure to use discrete data points in your plot. How does the measured output range of the DAC compare to your calculated values?

Use the function generator to provide a zero-to-5 V square wave into the LSB digital input (b_0), and set b_1 - b_3 to zero. (*Before* connecting the function generator to the chip, observe its output on the scope to make sure your waveform does not go below 0 V or exceed 5 V.) Observe this digital signal on one scope channel and the DAC output on the other channel. Increase the frequency of the square wave until you can clearly see and measure (using the cursors) the settling time of the DAC.

- Include a screen shot of the scope showing this settling behavior.

Now connect the square wave to *all four* binary inputs so that we switch between inputs of 0000 and 1111. Observe the two signals on the scope, varying the square wave frequency. Adjust this frequency until you clearly observe the slew rate limitations of the DAC op-amp.

- Include a screen shot of the scope showing this slewing behavior. Use the cursors to measure the positive and negative slew rates. How long does the DAC take to slew from minimum to maximum (and maximum to minimum) output?
- Based on these experiments, what is the maximum frequency you would recommend for this DAC’s operation? Is this DAC sufficient to use in audio

applications requiring 44,000 conversions per second in order to reproduce sounds up to 22 kHz?

We will now explore the output range limitations of this DAC. Increase V_{BIAS} to 2.0 V. Recalculate the expected minimum and maximum output voltages. Now sweep the binary input from 0000 to 1111, recording V_{out} at each step.

- Plot the DAC transfer function as before. Do you see any problem with the DAC operation? What is the cause of the problem? (Note that the op-amp in this DAC has the same design as the one you studied in Lab 5.)

Now decrease V_{BIAS} to 0.1 V. Recalculate the expected minimum and maximum output voltages. Now sweep the binary input from 0000 to 1111, recording V_{out} at each step.

- Plot the DAC transfer function as before. Do you see any problem with the DAC operation? What is the cause of the problem? (Hint: This time, the problem is not with the op-amp.)

Experiment 2: 3-Bit Flash ADC

A 3-bit flash ADC is shown on the next page. Although the triangular-shaped objects may look like op-amps, they are *comparators*, which are (to oversimplify things a bit) uncompensated op-amps (since they are never used with feedback and need to be very fast) with digital outputs.

The digital logic shown as a “black box” in the schematic has the following truth table:

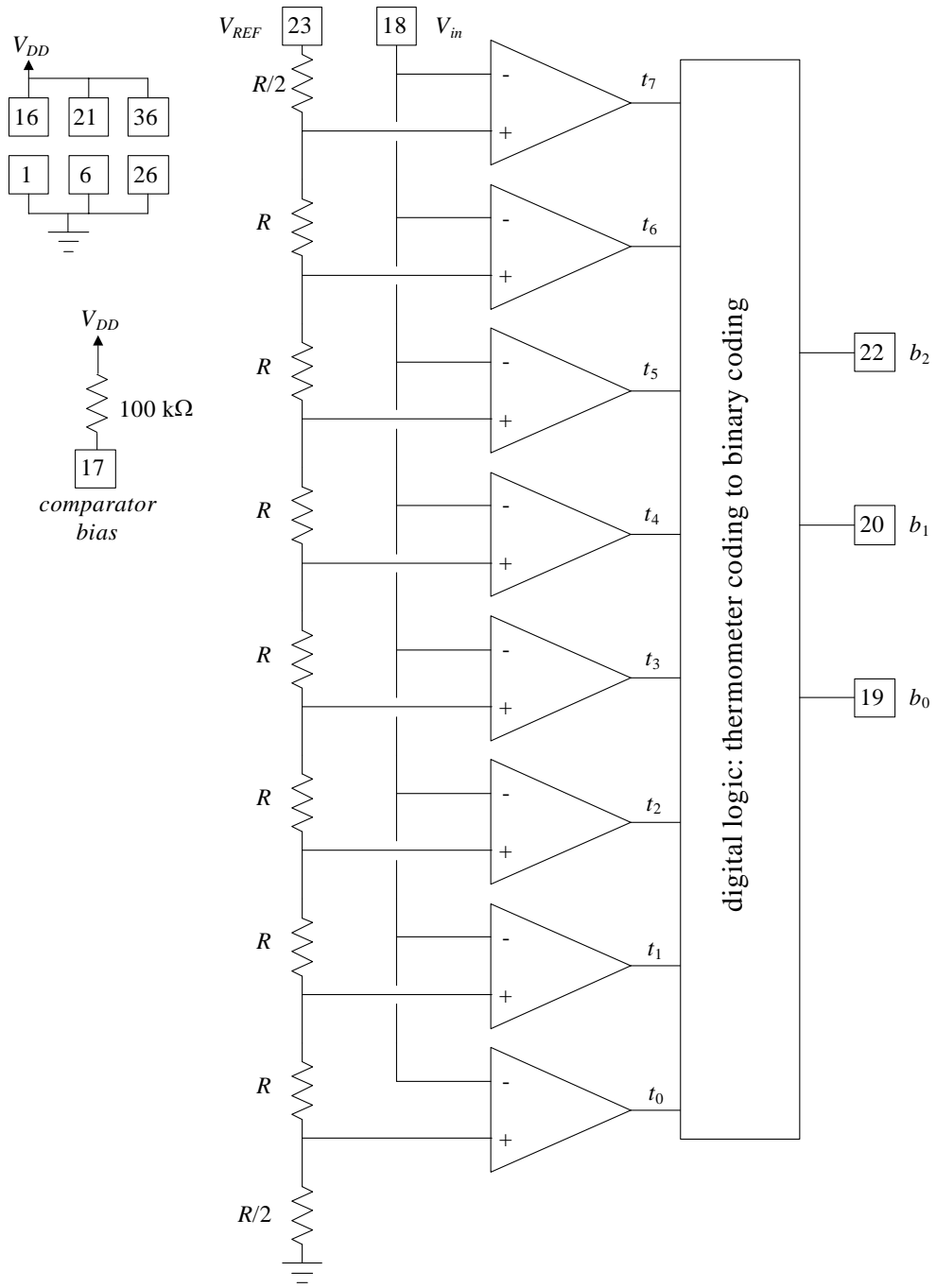
t_7	t_6	t_5	t_4	t_3	t_2	t_1	t_0	b_2	b_1	b_0
1	1	1	1	1	1	1	1	0	0	0
1	1	1	1	1	1	1	0	0	0	1
1	1	1	1	1	1	0	0	0	1	0
1	1	1	1	1	0	0	0	0	1	1
1	1	1	1	0	0	0	0	1	0	0
1	1	1	0	0	0	0	0	1	0	1
1	1	0	0	0	0	0	0	1	1	0
1	0	0	0	0	0	0	0	1	1	1
0	0	0	0	0	0	0	0	0	0	0

Note that the last entry in this table may produce an undesired output.

Each resistor R is made from a strip of p^+ diffusion that is 200 μm long and 1 μm wide. The $R/2$ resistors are 100 μm long and 1 μm wide.

- Calculate the expected total resistance of the resistor chain. Using an ohmmeter, measure the resistance between pin 23 and ground. What is the value of R based on this measurement? Tie V_{REF} to V_{DD} .
- How much power is the resistor chain dissipating? Derive the voltage at each point on the resistor chain, and write this on the schematic.

Pin-out for Experiment 2 – Chip B



Tie a 100 k Ω resistor between pin 17 and V_{DD} . This will set up a current of approximately 40 μ A into pin 17. This current is mirrored on chip to bias the comparators.

Now sweep V_{in} from zero to V_{DD} and record the points where the binary output transitions from one code B_{out} to the next. During this experiment, make sure only to *increase* the input voltage; don't turn it up and down. If you miss a transition, turn V_{in} back to zero and then move up again until you find it.

- Plot B_{out} (which will vary from zero to seven) vs. V_{in} as a “stair-step” plot similar to Fig. 11.4 in Johns & Martin. For example, if the ADC transitioned between 000 and 001 at 0.25 V and transitioned between 001 and 010 at 0.50 V, you should begin your plot as

```
plot([0 0.25 0.25 0.5 0.5], [0 0 1 1 2], 'o-');
```

to create a stair-step appearance that clearly shows the boundaries between codes.

- Do you observe a problem at the top end of the input voltage range? Consult the logic truth table shown previously and explain what happens.

Now sweep V_{in} down from V_{DD} to zero and record the points where the binary output transitions from one code B_{out} to the next. During this experiment, make sure only to *decrease* the input voltage; don't turn it up and down. If you miss a transition, turn V_{in} back to V_{DD} and then move down again until you find it.

- Plot B_{out} vs. V_{in} as a “stair-step” plot superimposed on the previous plot. Do you see a difference in the transition points? Read pp. 318-319 in Johns & Martin and comment on the presence and effect of *hysteresis* in comparators in the ADC. Do our comparators exhibit hysteresis?

We will now observe this hysteresis in another experiment. Using the function generator, apply a 100-kHz triangle wave to the input of the ADC. This triangle wave should vary from 1.0 V to 4.0 V at its minimum and maximum. Observe the waveform on the scope before you connect it to your chip to make sure it is correct. Using your scope, observe the input waveform on one channel and the MSB output (b_2) on the other channel. Superimpose the two waveforms on the screen. Use the two horizontal cursors to measure the voltage difference between the MSB trip point on the increasing and decreasing portions of the triangle wave.

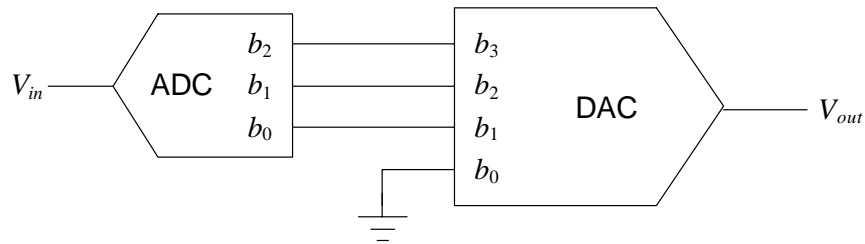
- Include a screen shot of the scope with the two cursors set appropriately. What is the magnitude (in volts) of the hysteresis? How does this voltage compare with the voltage difference between two digital output codes? Express the hysteresis in terms of LSB, where one LSB is the voltage difference between adjacent code words.
- Do you also observe small glitches in the MSB waveform? What is the source of these glitches?

Now apply 1.0 V to 4.0 V square wave to the input while still observing the MSB. Increase the frequency until you can measure the “conversion time” of the ADC. What is

its conversion time? What is the maximum frequency at which this ADC should be used? Would this ADC be adequate for audio applications required 40,000 samples per second?

Experiment 3: Analog-Digital-Analog System

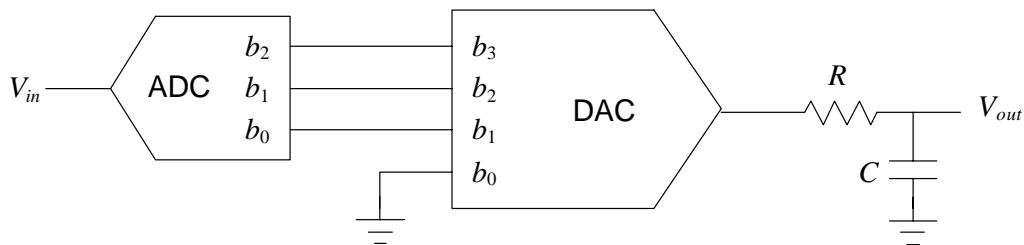
We will now have a bit of fun and build the following system:



Set V_{BIAS} back to 1.0 V. Apply a 10-kHz sine wave to the input. Observe V_{in} and V_{out} on the scope. Adjust the amplitude and offset of the input sine wave so that the output has all eight steps visible, but avoids the erroneous “zero” output at the top of the ADC’s range.

- Include a screen shot of the scope.

Now let’s add a single-pole low-pass “smoothing” filter at the output to eliminate the high-frequency quantization noise:



Use $R = 1 \text{ k}\Omega$.

- Calculate the necessary value of C to give a cutoff frequency of around 40 kHz. This is sufficiently high to avoid attenuating our 10-kHz signal, but low enough to eliminate most of the quantization noise. Use the “RC-box” at your lab station to set the appropriate capacitance.
- Observe the input and output in the scope, and include a screen shot. Feel free to play around with this system, adjusting the input signal or filter cutoff frequency.

EXTRA CREDIT

Read section 11.5 in Johns & Martin. Calculate worst-case INL and DNL errors for both the DAC and ADC. In your report, include plots with linear fits (like Figure 11.10) and plots of INL and DNL errors for each code. Express INL and DNL errors both in volts, and also in equivalent LSB.

REPORT

Each lab group (two students) should submit a lab report that is separate from the lab notebook. (In this class, lab notebooks will not be turned in). The report should be typed, not handwritten, although it is acceptable to add neat handwritten notes to figures where appropriate (e.g., to label different curves). Lab reports are due in your lab section one week after a two-week lab ends.

Begin your lab report with a title page containing your names, email addresses, T.A., lab section, and the title of the lab. Next, write one or two paragraphs outlining the overall goal of the lab. Describe how you performed each experiment, listing any problems you encountered and how you overcame them. Figures are preferably included in line with the text. You should number the figures and refer to them from the text.

- Every sentence labeled with a “bullet” like this indicates either a figure you should include or an answer you should explicitly provide in your report.

The grading for lab 6 will be as follows:

Screenshots, Plots (10):	4 points each
Answers (9):	2 points each
Introduction and conclusion:	4 points
<u>Format and style:</u>	<u>3 points</u>
Total:	65 points

Extra credit: 10 points

Your lab report should contain a description of all experiments performed, data plots (with fits) requested throughout this assignment, and a discussion of how the measured data (and fit parameters) compare with circuit theory.