

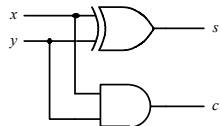
$+y$	$+0$	$+1$	$+0$	$+1$
$c\ s$	$0\ 0$	$0\ 1$	$0\ 1$	$1\ 0$

Carry \uparrow \uparrow Sum

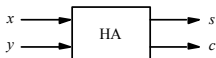
(a) The four possible cases

x	y	Carry c	Sum s
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

(b) Truth table



(c) Circuit

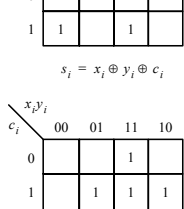


(d) Graphical symbol

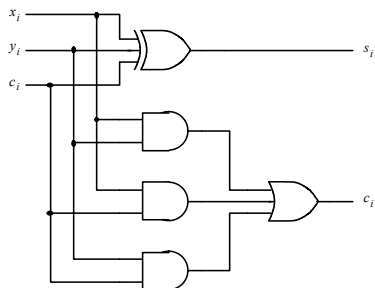
Figure 5.2. Half-adder.

c_i	x_i	y_i	c_{i+1}	s_i
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

(a) Truth table

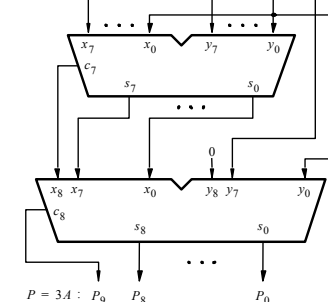


(b) Karnaugh maps

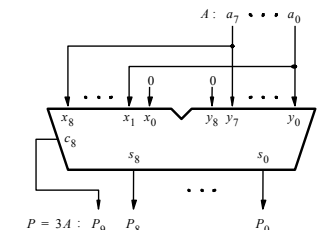


(c) Circuit

Figure 5.4. Full-adder.



(a) Naive approach



(b) Efficient design

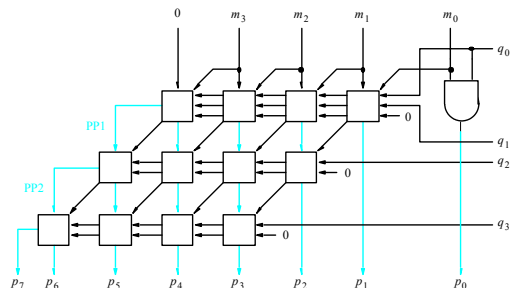
Figure 5.7. Circuit that multiplies an 8-bit unsigned number by 3.

Multiplicand M	(14)	1110
Multiplier Q	(11)	$\times 1011$
		<hr/>
		1110
		1110
		0000
		1110
		<hr/>
Product P	(154)	10011010

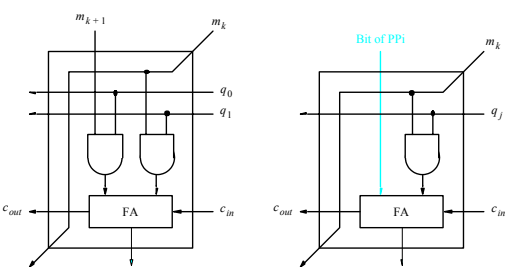
(a) Multiplication by hand

Multiplicand M	(11)	1110
Multiplier Q	(14)	$\times 1011$
		<hr/>
Partial product 0		1110
		+ 1110
		<hr/>
Partial product 1		10101
		+ 0000
		<hr/>
Partial product 2		01010
		+ 1110
		<hr/>
Product P	(154)	10011010

(b) Multiplication for implementation in hardware



(a) Structure of the circuit



(b) A block in the top row (b) A block in the bottom two rows

Multiplicand M	(+14)	01110
Multiplier Q	(+11)	$\times 01011$
		<hr/>
Partial product 0		001110
		+ 011110
		<hr/>
Partial product 1		010101
		+ 000000
		<hr/>
Partial product 2		001010
		+ 011110
		<hr/>
Partial product 3		010011
		+ 000000
		<hr/>
Product P	(+154)	0010011010

(a) Positive multiplicand

Multiplicand M	(-14)	10010
Multiplier Q	(+11)	$\times 01011$
		<hr/>
Partial product 0		1110010
		+ 110010
		<hr/>
Partial product 1		1101011
		+ 000000
		<hr/>
Partial product 2		1110101
		+ 110010
		<hr/>
Partial product 3		1101100
		+ 000000
		<hr/>
Product P	(-154)	1101100110

(b) Negative multiplicand

Bit positions	Bit positions 054							
	000	001	010	011	100	101	110	111
3210								
0000	NUL	DLE	SPACE	0	@	P	'	p
0001	SOH	DC1	!	1	A	Q	a	q
0010	STX	DC2	"	2	B	R	b	r
0011	ETX	DC3	#	3	C	S	c	s
0100	EOT	DC4	\$	4	D	T	d	t
0101	ENQ	NAK	%	5	E	U	e	u
0110	ACK	SYN	&	6	F	V	f	v
0111	BEL	ETB	'	7	G	W	g	w
1000	BS	CAN	(8	H	X	h	x
1001	HT	EM)	9	I	Y	i	y
1010	LF	SUB	*	:	J	Z	j	z
1011	VT	ESC	+	;	K	[k	{
1100	FF	FS	,	<	L	\	l	
1101	CR	GS	-	=	M]	m	}
1110	SO	RS	.	>	N	^	n	~
1111	SI	US	/	?	O	_	o	DEL
NUL	Null/Idle	SI						Shift in
SOH	Start of header	DLE						Data link escape
STX	Start of text	DC1-DC4						Device control
ETX	End of text	NAK						Negative acknowledgement
EOT	End of transmission	SYN						Synchronous idle
ENQ	Enquiry	ETB						End of transmitted block
ACK	Acknowledgement	CAN						Canoe! (error in data)
BEL	Audible signal	EM						End of medium
BS	Back space	SUB						Special sequence
HT	Horizontal tab	ESC						Escape
LF	Line feed	FS						File separator
VT	Vertical tab	GS						Group separator
FF	Form feed	RS						Record separator
CR	Carriage return	US						Unit separator
SO	Shift out	DEL						Delete/Idle

Bit positions of code format =

6	5	4	3	2	1	0
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Table 5.4. The seven-bit ASCII code.