Fundamentals of Digital Logic Design
ECE 3700
Practise Exam for the Mid-term 2
Spring 2009

Note: Time yourself for 1 hr 20 min. Closed book, closed notes, open minds. Do not panic. Good luck.

1. (4 points) Consider two 4-bit numbers $A = \{a_3, a_2, a_1, a_0\}$ and $B = \{b_3, b_2, b_1, b_0\}$, given in **two's complement form**. You are asked to design a circuit that takes these two numbers and produces an output s, such that $s = 1$ if and only if $A > B$. Otherwise $s = 0$ when $A \leq B$. For example:

- If $A = -2$ and $B = -3$, $A > B$.
- If $A = -2$ and $B = 0$, $A < B$.
- If $A = 5$ and $B = -1$, $A > B$.
- If $A = 5$ and $B = 7$, $A < B$.

Clearly, a truth table-based approach (2^8 minterms) is out of the question. Design the above circuit assuming that you have access to pre-designed 4-bit ADD/SUB unit, MUXes, Decoders, AND/OR/NOT/XOR/XNOR gates but *unfortunately, you don't have access to any magnitude comparators*.

2. (2 points) Design a circuit that takes as input *four* n-bit vectors, $A[n-1:0], B[n-1:0], C[n-1:0], D[n-1:0]$ given as *unsigned* integers. The circuit selects the minimum, or the smallest amongst them, and outputs the vector. Design the circuit efficiently, using a minimum number of comparators and MUXes.

3. (3 points) Let f be a Boolean function and x be one of the variables in its support. We know that f can be decomposed using the Shannon's expansion w.r.t. variable x as $f = x \cdot f(x = 1) + \overline{x} \cdot f(x = 0)$. Note that it is customary to use the notation $f_x = f(x = 1)$ and $f_{\overline{x}} = f(x = 0)$. So, the Shannon's expansion reads $f = x \cdot f_x + \overline{x} \cdot f_{\overline{x}}$. This is in fact a sum-of-product representation of the Shannon's expansion of f w.r.t. x.

(a) (1 point) Let $f(x, y, z) = xy + yz + xz$. Compute $f_x = f(x = 1)$, then compute $f_{\overline{x}} = f(x = 0)$. Now compute $f_x \cdot f_{\overline{x}}$; i.e. compute the product (or Boolean AND) of f_x and $f_{\overline{x}}$.

(b) (2 points) Now you are asked to prove that the **product of sum** representation of the Shannon's expansion is $f = (x + f_{\overline{x}}) \cdot (\overline{x} + f_x)$. In other words, prove that $(x + f_{\overline{x}}) \cdot (\overline{x} + f_x) = x \cdot f_x + \overline{x} \cdot f_{\overline{x}}$. (There's a hint in the exercise above).

4. (3 points) Design a modulo-6 synchronous down counter using TFFs. Assume that each TFF has a *T, Clk* and *Reset*

input and Q output. You can use any logic gates that you need. (Note: Modulo 6 counter counts from 0 to 5 and goes back to 0 and repeats).

5. (3 points) Solve problem 7.22 from the textbook.