1. (4 points) [Design of two's complement comparators] Consider two 4-bit numbers $A = \{a_3, a_2, a_1, a_0\}$ and $B = \{b_3, b_2, b_1, b_0\}$, given in two's complement form. You are asked to design a circuit that takes these two numbers and produces an output $s$, such that $s = 1$ if and only if $A > B$. Otherwise $s = 0$ when $A \leq B$. For example:

- If $A = -2$ and $B = -3$, $A > B$.
- If $A = -2$ and $B = 0$, $A < B$.
- If $A = 5$ and $B = -1$, $A > B$.
- If $A = 5$ and $B = 7$, $A < B$.

Clearly, a truth table-based approach ($2^8$ minterms) is out of the question. Design the above circuit assuming that you have access to pre-designed 4-bit unsigned adders, MUXes, Decoders, AND/OR/NOT/XOR/XNOR gates but unfortunately, you don’t have access to any magnitude comparators.

2. (2 points) Design a circuit that takes as input four $n$-bit vectors, $A[n-1 : 0], B[n-1 : 0], C[n-1 : 0], D[n-1 : 0]$ given as unsigned integers. The circuit selects the minimum, or the smallest amongst them, and outputs the vector. Design the circuit efficiently, using a minimum number of unsigned comparators and MUXes.

3. (3 points) Let $f$ be a Boolean function and $x$ be one of the variables in its support. We know that $f$ can be decomposed using the Shannon’s expansion w.r.t. variable $x$ as $f = x \cdot f(x = 1) + \overline{x} \cdot f(x = 0)$. Note that it is customary to use the notation $f_x = f(x = 1)$ and $f_{\overline{x}} = f(x = 0)$. So, the Shannon’s expansion reads $f = x \cdot f_x + \overline{x} \cdot f_{\overline{x}}$. This is in fact a sum-of-product representation of the Shannon’s expansion of $f$ w.r.t. $x$.

   (a) (1 point) Let $f(x, y, z) = xy + yz + xz$. Compute $f_x = f(x = 1)$, then compute $f_{\overline{x}} = f(x = 0)$. Now compute $f_x \cdot f_{\overline{x}}$, i.e. compute the product (or Boolean AND) of $f_x$ and $f_{\overline{x}}$.

   (b) (2 points) Now you are asked to prove that the product of sum representation of the Shannon’s expansion is $f = (x + f_{\overline{x}}) \cdot (\overline{x} + f_x)$. In other words, prove that $(x + f_{\overline{x}}) \cdot (\overline{x} + f_x) = x \cdot f_x + \overline{x} \cdot f_{\overline{x}}$. (There’s a hint in the exercise above). [A more tricky version of this question is given in textbook problem 6.10, pp. 376].

4. (3 points) You are given a pre-designed 4-bit ripple carry adder that takes inputs $A[3 : 0], B[3 : 0], C_{in}$ and
produces output $S[4 : 0]$. Using this pre-designed block, and any number of AND/OR/XOR/NOT gates, design a two’s complement adder and subtractor unit. Unfortunately, the 4-bit ripple carry adder is given as a black-box. You cannot access any internal signals. Why is this a problem? Overflow. [Hint, see Sec 5.5, particularly 5.5.6]

5. (3 points) Solve problem 6.11 from the textbook. Note that this problem can be solved by repeated application of Shannon’s expansion. [See textbook, 330 - 335, and the solved problems in Sec 6.8].