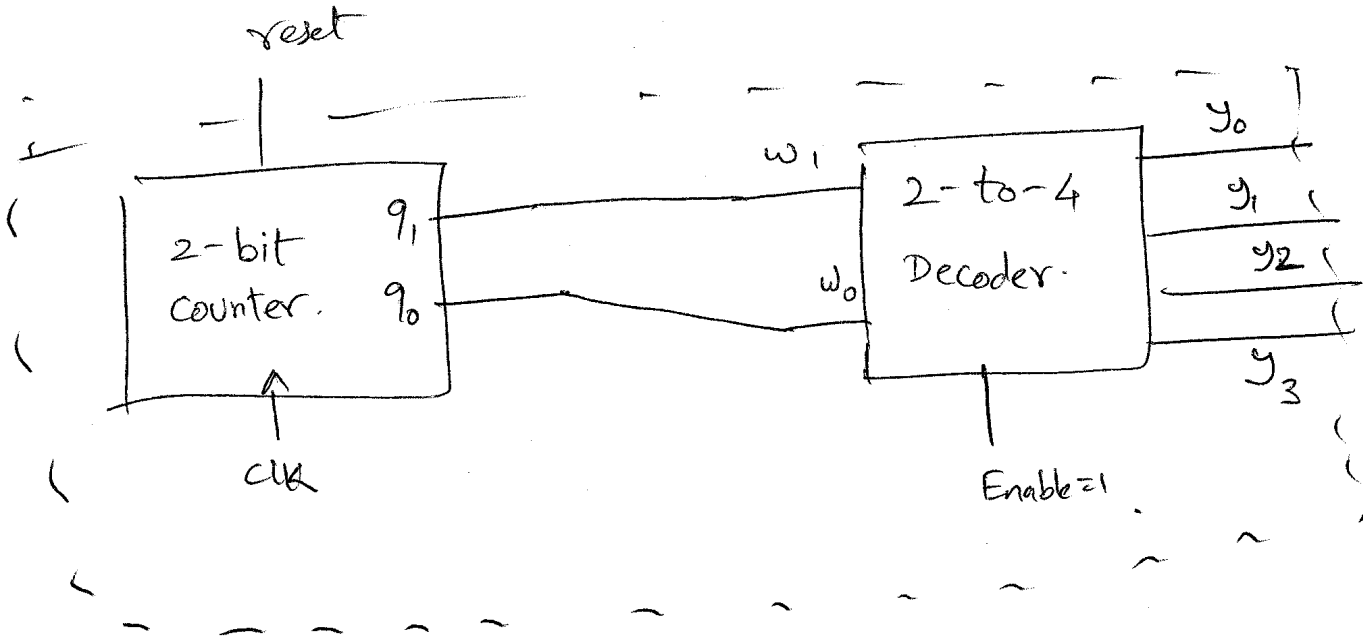


# HW4 Solutions

Q1



$q_1, q_0$

00

$y_0 = 1, y_1 = y_2 = y_3 = 0$

01

$y_1 = 1$  others 0

10

$y_2 = 1$

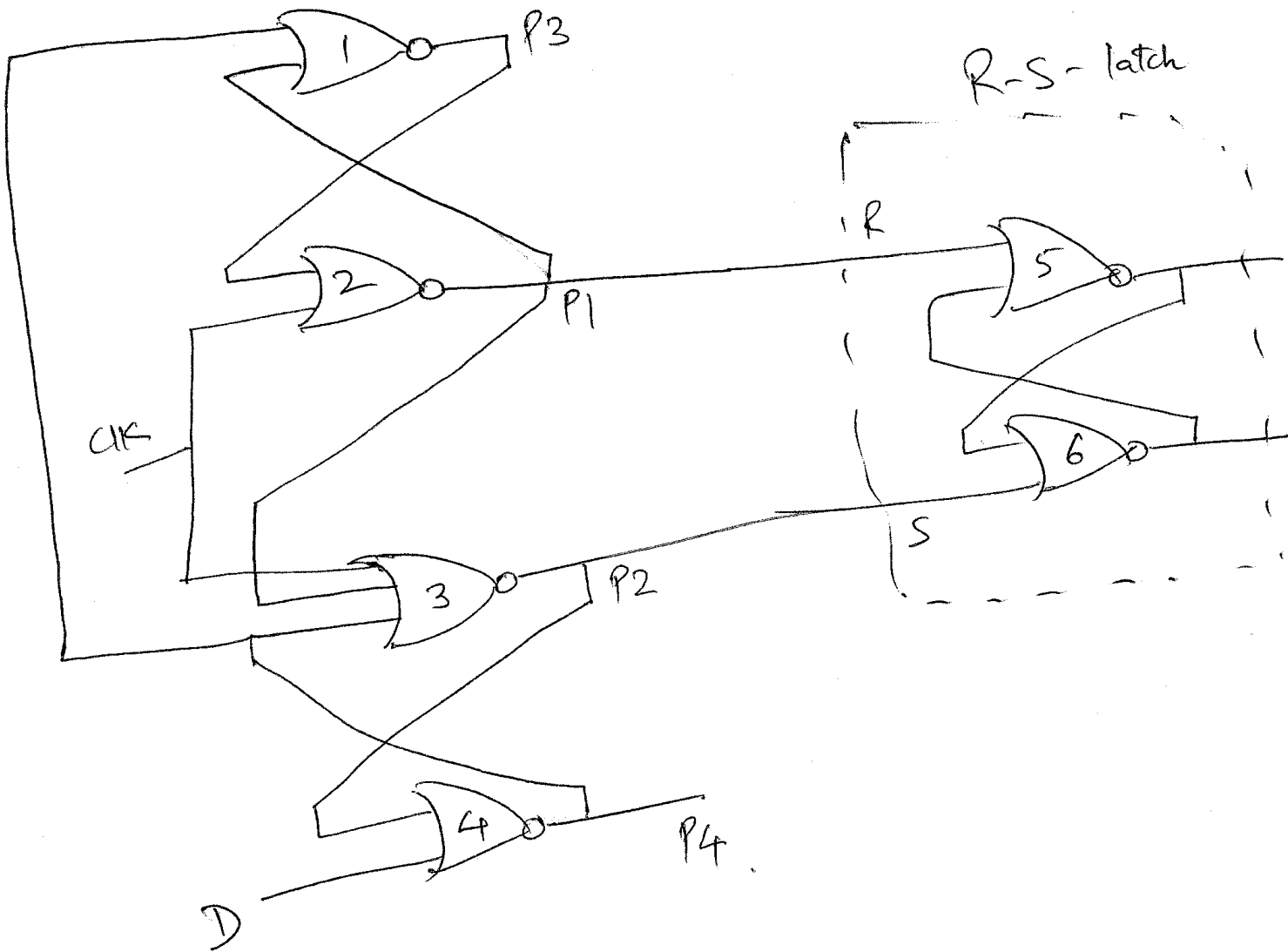
11

$y_3 = 1$

00

$y_0 = 1$

Q2



①  $CLK=1, P1=P2=0 \Rightarrow R-S-latch = \text{cross-coupled NOR gates}$   
 act as a chain of inverters and remember the previous value.

② Setup D:  $\rightarrow P2=0, D$  input applied:

$$\underline{P4 = \overline{D}}, P1=0, \underline{P3 = D}.$$

$D$  &  $\overline{D}$  sitting pretty @ Gates 2 & 4.

③ Apply CLK trigger.  $\downarrow$  CLK=0.

$P1 = \bar{D}$   
 $P2 = D$   $\Rightarrow$  R-S latch gets updated.

$Q = D$

(this proves Q updates during  $\downarrow$  CLK).

④ Once  $Q = D$  & CLK=0.

chang D input  $\rightarrow$  no change in FF.

Say  $D = 1$

$P2 = D = 1$

D-input @ Gate 4 = blocked.

So no change propagates

through G4.

Say  $D = 0$

$P1 = \bar{D} = 1$

$\Rightarrow P2 = 0$  (stable)

$P1 = 1 \Rightarrow P3 = 0$   
 $CLK = 0$  }  $\Rightarrow P1 = 1$  stable.

So  $P1$  &  $P2$  are stable & no change in latch takes place.

$\therefore$  Device is insensitive to changes in D after  $\downarrow$  CLK.

Q3



# Synchronous down counter using TFFs

↳ all TFFs synchronized w.r.t clock

Down counting

$Q_3$	$Q_2$	$Q_1$	$Q_0$
1	1	1	1
1	1	1	0
1	1	0	1
1	1	0	0
1	0	1	1
1	0	1	0
1	0	0	1
1	0	0	0
0	1	1	1
⋮			

\*  $T_0 = 1$

\*  $Q_1$  toggles when  $Q_0 = 0$  in previous state.

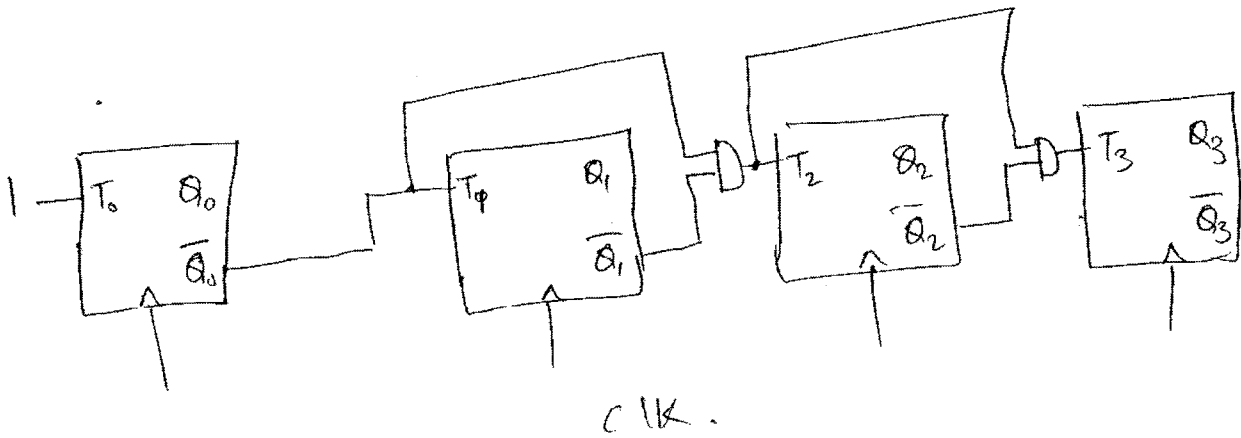
$$T_1 = \overline{Q_0}$$

\*  $Q_2$  Toggles when  $Q_1 = 0$  &  $Q_0 = 0$

$$\Rightarrow T_2 = \overline{Q_1} \cdot \overline{Q_0}$$

\*  $Q_3$  toggles when

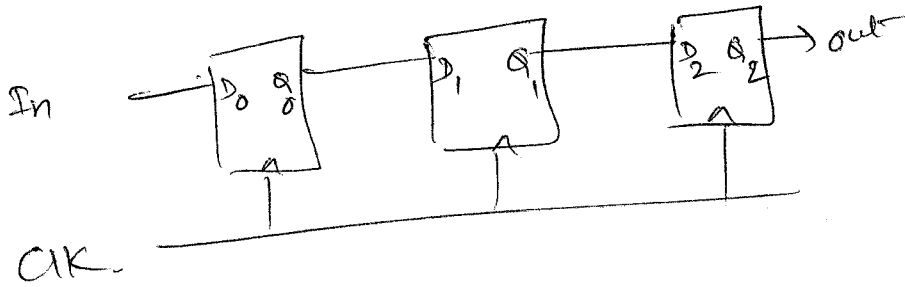
$$\overline{Q_2} \cdot \overline{Q_1} \cdot \overline{Q_0}$$



Q4 Lets take a 3-bit register.

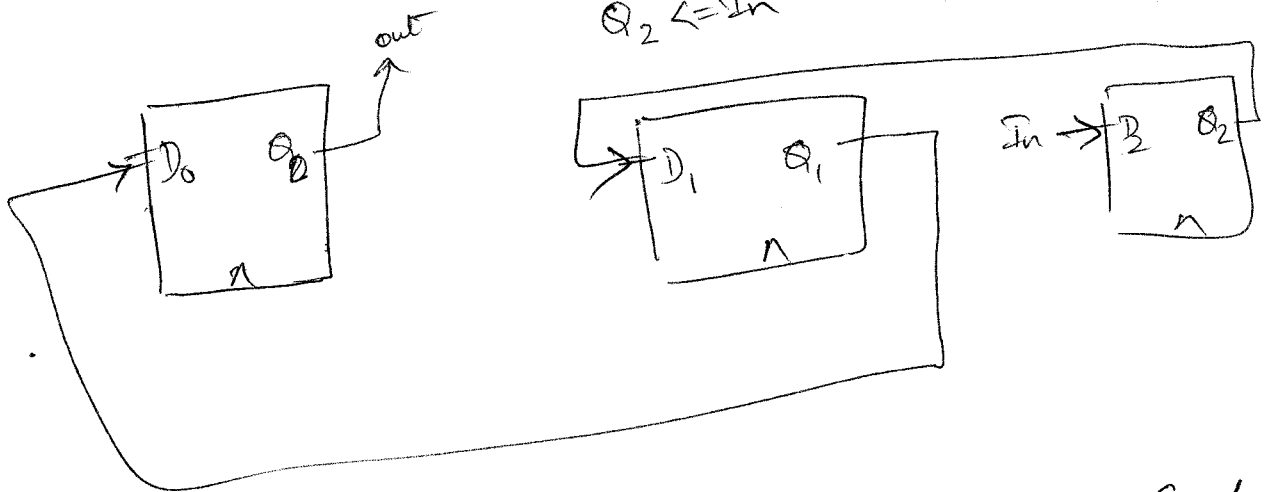


Shift right.  
 $Q_0 \leftarrow In$   
 $Q_1 \leftarrow Q_0$   
 $Q_2 \leftarrow Q_1$

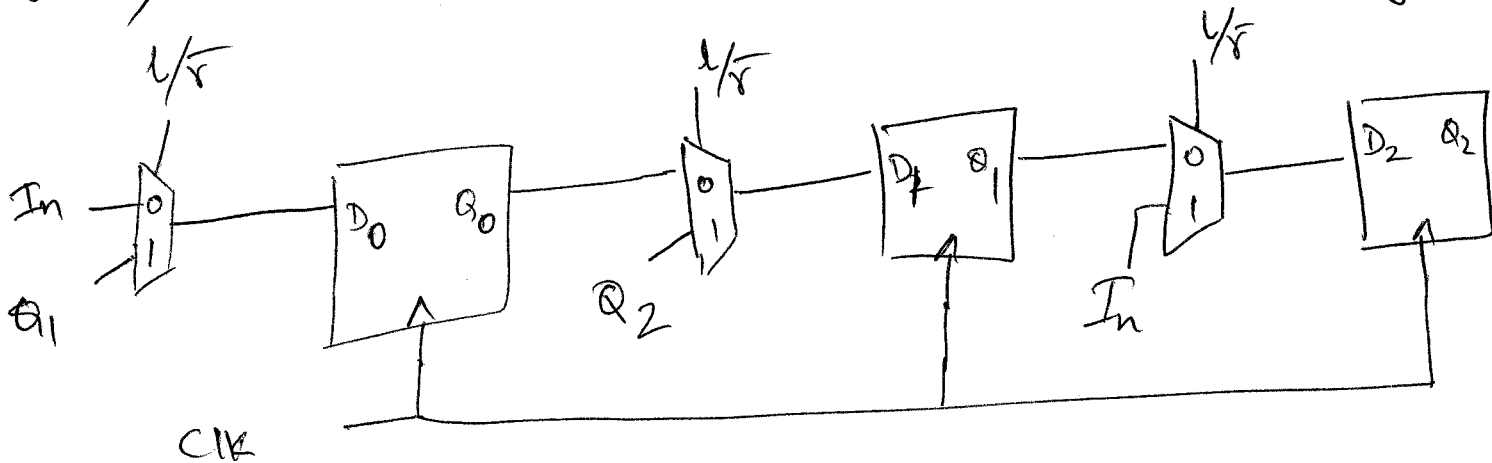


Shift Left.

$Q_1 \leftarrow Q_2$   
 $Q_0 \leftarrow Q_1$   
 $Q_2 \leftarrow In$

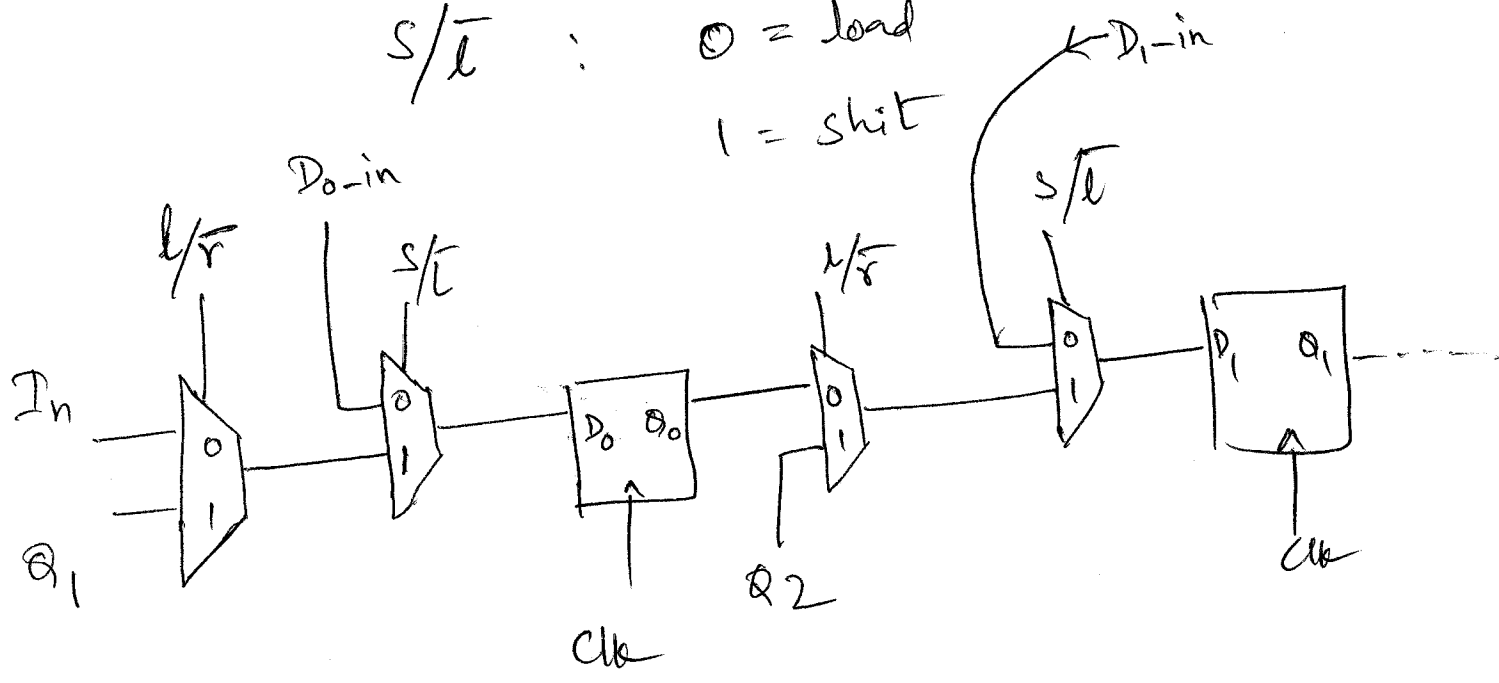


Left/Right } Use a mux controlled by left/right (l/r)  
 Shift } to choose what goes into  $D_i$   
 1 = left shift  
 0 = right shift



Now you can introduce an extra mux to choose between shift or load capability.

$S/\bar{L}$  : 0 = load  
1 = shift

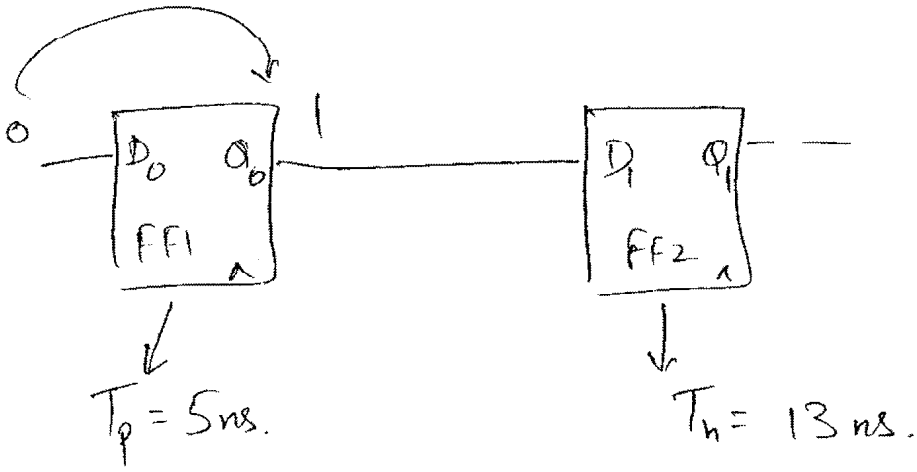


MUXes are Awesome!

Q4

Setup & hold time for -ve edge triggered DFFs.

See fig 7.9 in text book.



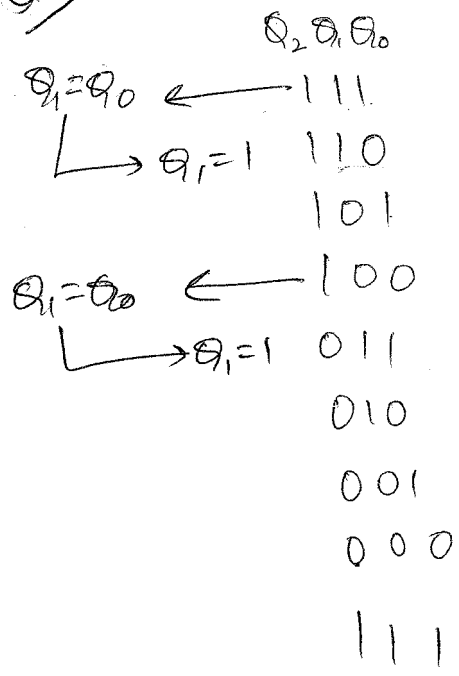
Say clk arrives @ both FFs at  $t=0$ .

$Q_0$  changes from  $1 \rightarrow 0$  @  $t=5$ .

But  $Q_0$  should be stable ~~for~~ until  $t=13$ .

hold time failure @ FF2.

Q6 Down counter



$D_0 = \overline{Q_0}$  (1st bit changes every clock cycle)

$D_1 = ?$  To answer this, reconsider  $D_0$ .

$$D_0 = \overline{Q_0} = 1 \oplus Q_0 = 0 \oplus \overline{Q_0} = \underline{\underline{0 \oplus \overline{Q_0}}}$$

$D_1 = 1$ , whenever  $Q_1 = Q_0$  in the previous cycle!

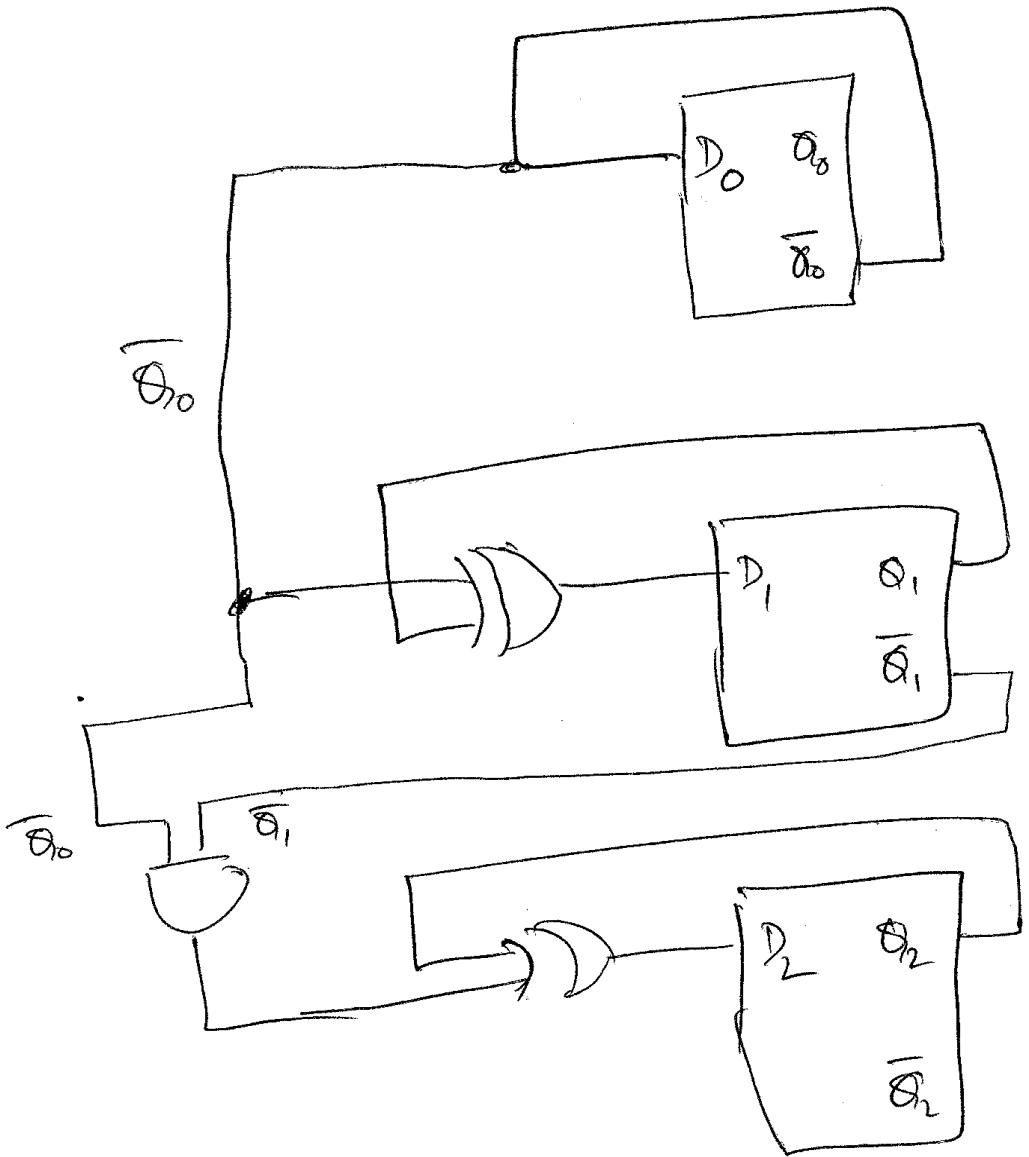
$$\therefore D_1 = Q_1 \oplus \overline{Q_0} = Q_1 \oplus \overline{Q_0}$$

Similarly  $D_2 = 1$  when.

$$Q_2 \oplus \overline{Q_1} \cdot \overline{Q_0}$$

Similarly  $D_3 = Q_3 \oplus \overline{Q_2} \cdot \overline{Q_1} \cdot \overline{Q_0}$

Do you see the similarity with equations on pp. 411-413 (and Table 7.1)



and so on