Lab Assignment for Extra Credit

ECE/CS 3700
Spring 2011

Assigned Thu (April 21) onwards, circuit demo on: i) 4/27, 3pm - 5pm; or ii) 4/29, 12pm - 2pm. Paymon or Priyank would be available in the lab.

This lab is for extra credit. You will perform Verilog Design, Simulation, Synthesis, Implementation and Testing of a music/tone generator. You do not have to submit any written reports. If your circuit generates the music alright, then I will give you 6 extra points, out of the total 100, for the class.

I. THE MUSIC/TONE GENERATOR

If we generate a square/sine-wave of some frequency (between 20Hz to 20KHz) and connect it to a speaker, you’ll hear a tone. Musical notes (A, B, C, C#, etc.) can be generated by designing a clock corresponding to that frequency. If I give you a document that lists the frequency of all musical notes, then you should be able to design a rudimentary tone-generator. Of course, the quality of the sound depends upon amplification, filtering, signal processing, etc., but for this project, the main idea behind such a circuit is generating the clocks at different frequencies. Select different clocks at different intervals, and what you’ll hear is going to be “music to your ears”. So how is this different from the stop-watch? Well, the assignment is described below; refer to Fig. 1 too.

Your design will operate as follows:
• Using the switches S0, S1, S2 (on the FPGA) you can play each of the 7 notes (as in a trumpet?). We will generate only major notes.

![Fig. 1. Block Diagram of the Music/Tone Generator](image-url)
• When \( S3 \) is 0, your design should play the notes corresponding to the switches \((S0, S1, S2)\) pressed. When \( S3 = 1 \), you’ll ignore \( S0, S1, S2 \) and play a pre-recorded song. The pre-recorded song is an FSM design.

• First, let us consider the case when \( S3 = 0 \) - in which case \( S0, S1, S2 \) act like your keyboard.

• When none of the switches are pressed, you will not play any note. When you press \( S0 \), you’ll play note \( A \). When you press \( S1 \), you can play \( B \). When you press all three switches together you’ll play the last note \( G \). Therefore, by pressing a combination of these switches, you can create “music” (or “noise”, depending on your tastes).

• When \( S3 = 1 \), you’ll play a tune called Habanera from Carmen, an opera by Bizet. The composition (the notes, the frequency, and the duration of each note) is available as another document on the class web-page. Using the table, you’ll build a state-machine that generates a clock at a particular frequency, for a particular duration (corresponding to the note being played). Looks kind of tedious at first glance, but the design consists of a bunch of counters selected by a “selector FSM”!

• A midi file corresponding to the tune is also uploaded on the class webpage so you can hear the tune.

• Design your machine such that it keeps on repeating the tune - i.e., keeps on looping through (when \( S3 = 1 \)). The moment \( S3 = 0 \), the machine should get into the input polling mode.

• You can implement \( S3 \) using a DIP switch, and \( S0, S1, S2 \) using the push-button switches.

• Speakers are going to be available in the lab with Paymon or Travis.

• For the “Note to Frequency” translation, refer to the site:

http://www.phy.mtu.edu/~suits/notefreqs.html

**The Assignment:** Verilog Design + Simulation + Synthesis + Mapping + Demo + Project report = the usual.

**Efficiency of Design:** Remember, you have to generate square waves of different frequencies, depending upon the musical note to be played. You could design \( n \) different counters and a huge MUX that would select the desired frequency. Of course, this is a massively redundant design. All the counters (D-FFs) are counting, but only one is being used. What a waste of power. How would you make the design efficient? You could run one (fast) counter, and depending on the note pressed, **activate** the musical-note-generating counter.

**A. Lab Report Submissions + Deadlines**

No Lab reports!

**Deadlines:** Paymon and/or I (Priyank) will be available in the lab on i) wednesday, 4/27, 3pm - 5pm; and ii) friday, 4/29, 12pm - 2pm. You can demo your circuit to either of us.

Have fun!