

Lab Assignment 4

ECE/CS 3700

Spring 2009

Assigned the week of 3/2 onwards, Due date: your respective lab sessions during the week 3/9-3/13, before spring break.

This is a short 1-week long lab in which the objective is to learn about 7-segment decoder displays and Verilog design using 'always' statements.

In the previous lab, you designed a 4-bit adder and connected the output 'Sum' signal to the bar-LEDs on the board. In this lab, you will:

- Study the 7-segment display given in textbook, pp 343-344.
- Implement it using always statements
- Hook it up to your adder design (in Verilog)
- Synthesize the whole thing, download the design to the FPGA and show that by applying the stimulus (using switches) you can display the correct answer on the 7-segment display.

And that is it for this week! The TAs will tell you about the 7-segment displays in the lab, and we are also going to cover Verilog design styles using always blocks in the class. Have fun!