Fundamentals of Digital Logic Design
ECE 3700
Practise Exam - I
Spring 2009

Note: Time yourself for 1 hour and 20 minutes. Closed book, closed notes, open minds, Do not panic. Good luck.

1. (3 points) Let $A = \{a_1, a_0\}$ and $B = \{b_1, b_0\}$ be two 2-bit numbers. You are asked to design a single-output circuit that takes these two numbers and outputs a **1** if and only if $A \geq B$. When it comes to implementation, you are allowed to use only single-bit multiplexers (MUXes). The equation for the MUX is given as $z = x \cdot c + y \cdot \overline{c}$. Design the above circuit using only MUXes. (Note that you don't really need knowledge of Ch 5 for this question!)

2. (2 points) Find all the primes of the function: $f(a, b, c, d) = \sum m(0, 4, 8, 10, 11, 12, 13, 15)$. Use any method you deem fit for this computation.

3. **(3 points)** Consider two unsigned 2-bit numbers $D = \{d_1, d_0\}$ and $C = \{c_1, c_0\}$. Design a combinational circuit that takes these two numbers as inputs and produces a 2-bit output $R = \{r_1, r_0\}$. The output R should be the remainder after dividing D by C. For example, when $d_1, d_0 = 11$ and $c_1, c_0 = 10$, then the output $r_1, r_0 = 01$ (as $D = 3$ divided by $C = 2$ results in remainder $R = 1$). Note that since *divide by zero* is not defined, $c_1, c_0 = 00$ will never occur.

(a) Write the truth table for the circuit with D, C and inputs and R as outputs.

(b) Fill in the Karnaugh map and write simplified Boolean expressions for r_1 and r_0.

(c) Draw a schematic that implements the circuit. Assume that the signals d_1, d_0, c_1, c_0 are available only in TRUE form.

4. (3 points) A Salt Lake City based company (called "Intractable Logistics") employs 6 (six) sales persons, referred to as $S_1, S_2, \cdots, S_6$. The company has business interests in London (L), Paris (P), New York (N), Tokyo (T), Moab (M) and Zurich (Z); and it wants these cities to be visited by its sales persons. Unfortunately:

(a) Sales person S_1 can only visit cities L, N, and M.

(b) S_2 can only visit T and M.

(c) S_3 can only visit P, N, and Z.

(d) S_4 can only visit N, T, and Z.

(e) S_5 can only visit L, T, and M.

(f) S_6 can only visit L, P, and Z.

Select a minimum number of sales persons required to cover all the cities.

5. **(2 points)** Design a two-bit XOR circuit using only NAND gates. Use minimum number of NAND gates.

6. **(2 points)** Given the Pull-down network of a CMOS gate shown in Fig. 1, derive its corresponding pull-up network and write a Boolean expression for the function.

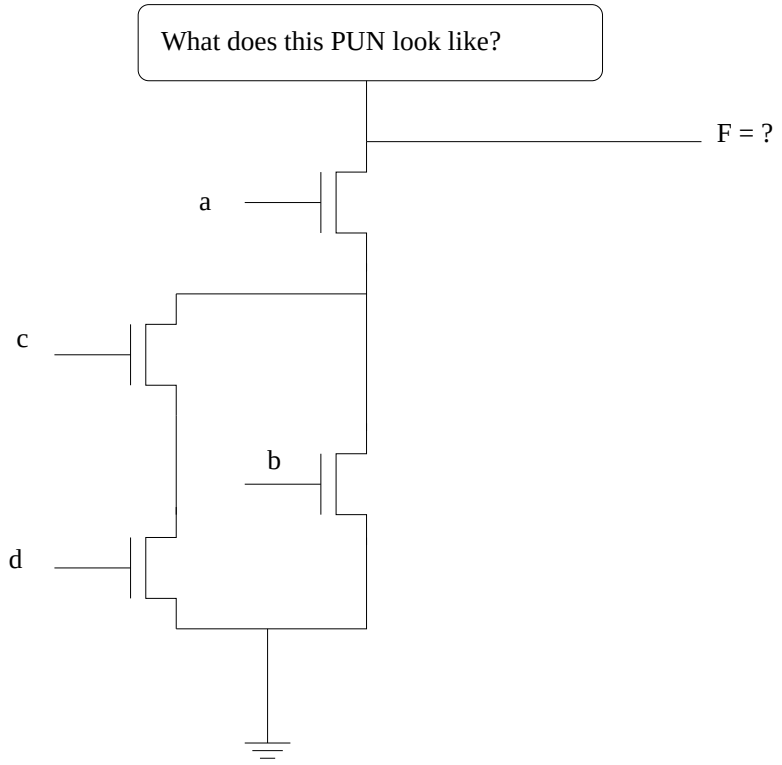

Fig. 1. Pull-down network of the gate is shown. Draw its corresponding pull-up network.