Q 7. Let us examine the signal propagations in the circuit between two positive edge clock triggers. When the first clock trigger arrives, let us assume that the D-input is stable enough so that there are no setup time violations. In that case, the signal-value at the D-input will appear at the Q output after 1-propagation delay, which is 1ns, subject to the fact that there are no hold-time violations too. Assume that there is no hold time violation at the first posedge clk trigger (we will prove this is true by analyzing the signal propagation through the circuit).

So, D appears at Q after 1ns (propagation delay). Then the change in Q value appears at the OR gate at 1ns, + 1ns + 1ns (OR-AND gate delay). To at t = 3ns, the D-value changes. Note that this does not violate the hold time, as D should be stable for 1ns hold-time after the posedge clock -- and D changes only after 3 ns (> 1ns).

We cannot now fire the next posedge trigger because we have to wait for setup time = 2ns. So, we can clock the circuit with total time delay of:
Prop. delay of DFF = 1ns +
Logic delay = 1 + 1 = 2ns +
Setup time = 2ns.

Total = 5ns time delay needed between two posedge triggers. If you clock the circuit faster, you will have setup-time violation!