Appendix B

Implementation Technology

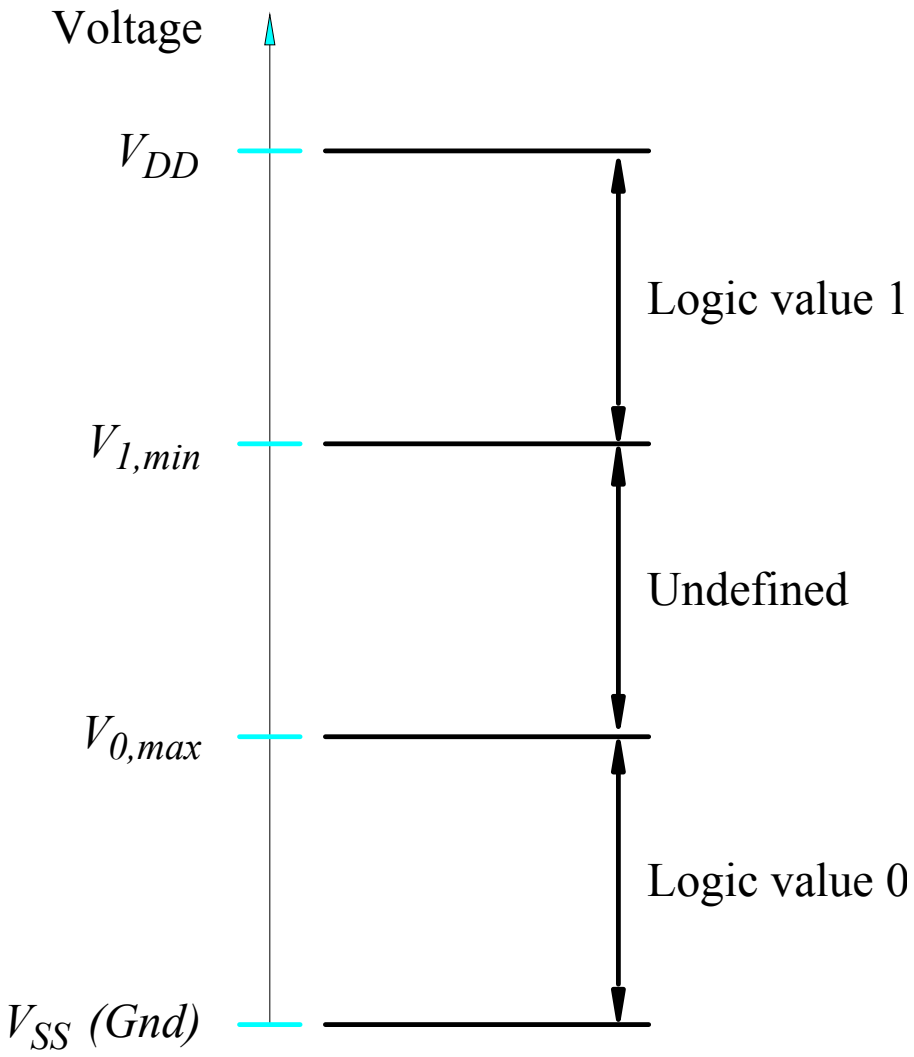
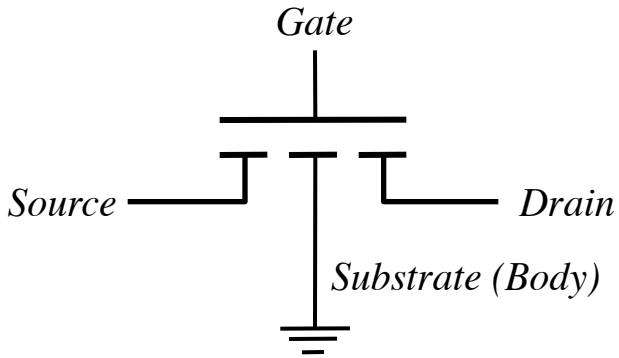
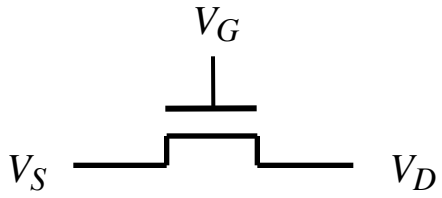


Figure B.1. Logic values as voltage levels.

(a) A simple switch controlled by the input *x*



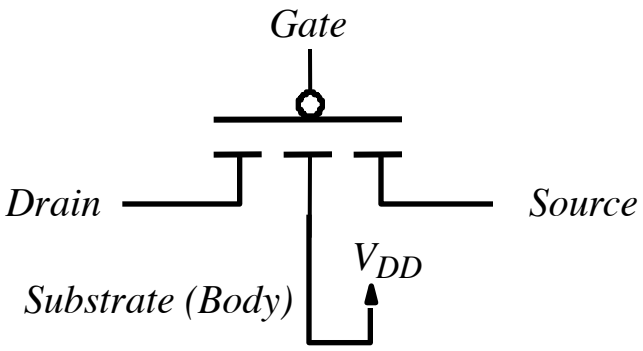
(b) NMOS transistor



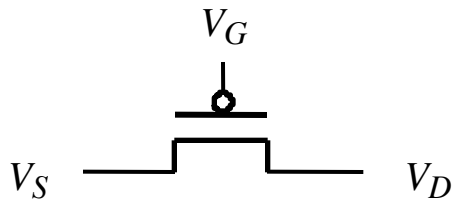
(c) Simplified symbol for an NMOS transistor

Figure B.2. NMOS transistor as a switch.

(a) A switch with the opposite behavior of Figure 3.2 *a*



(b) PMOS transistor



(c) Simplified symbol for a PMOS transistor

Figure B.3. PMOS transistor as a switch.

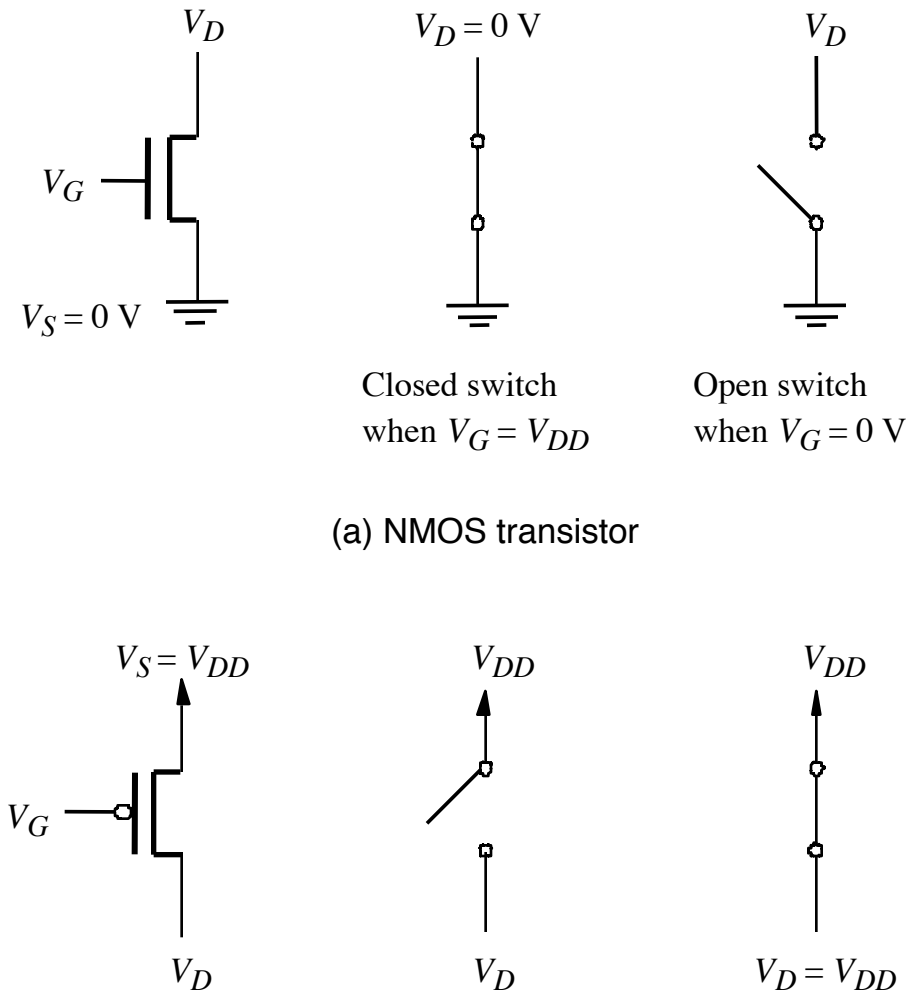
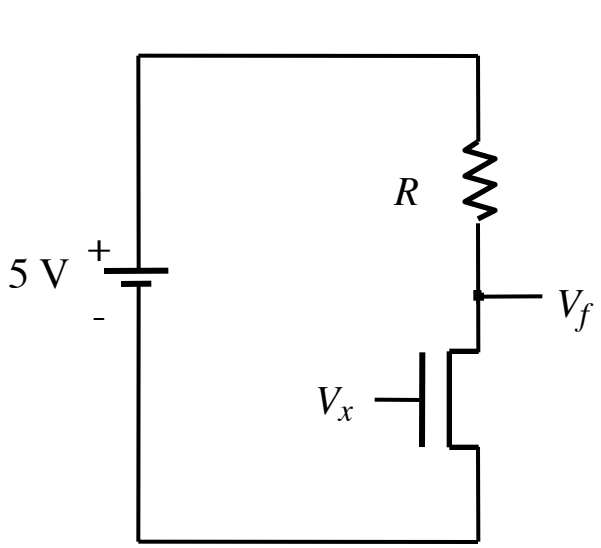
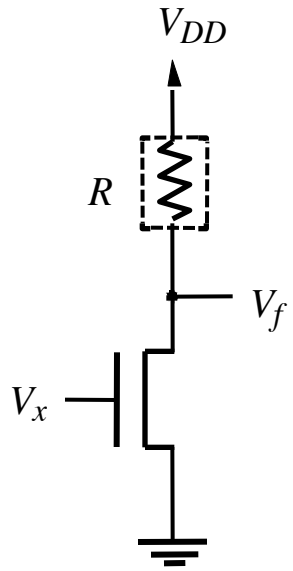


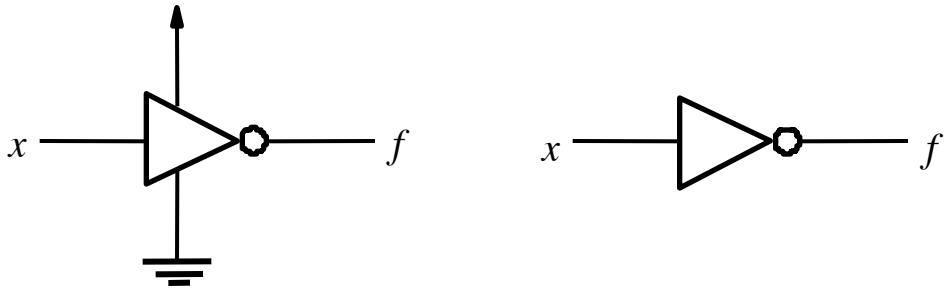
Figure B.4. NMOS and PMOS transistors in logic circuits.



(a) Circuit diagram

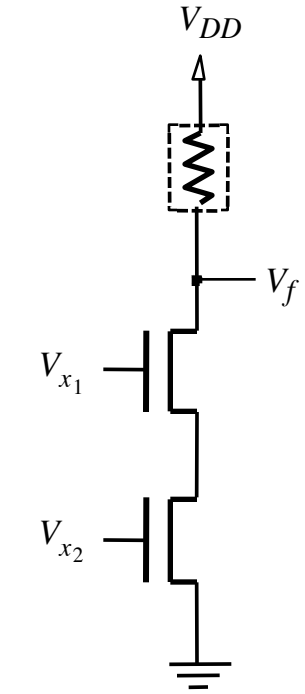


(b) Simplified circuit diagram



(c) Graphical symbols

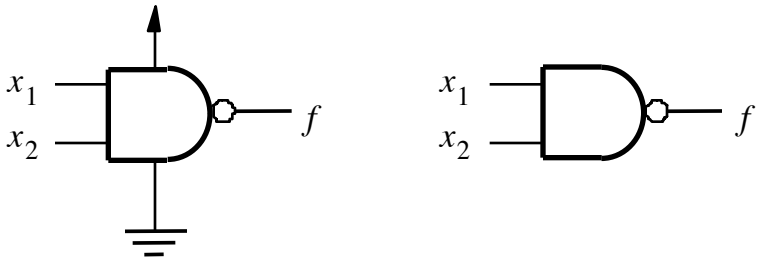
Figure B.5. A NOT gate built using NMOS technology.



(a) Circuit

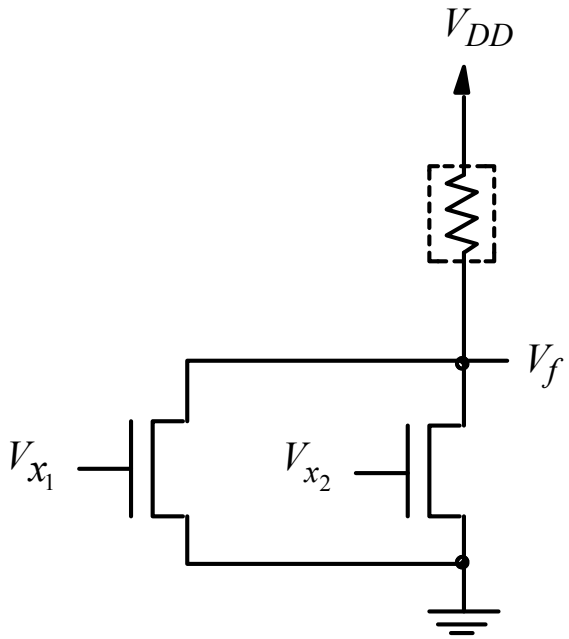
x_1	x_2	f
0	0	1
0	1	1
1	0	1
1	1	0

(b) Truth table



(c) Graphical symbols

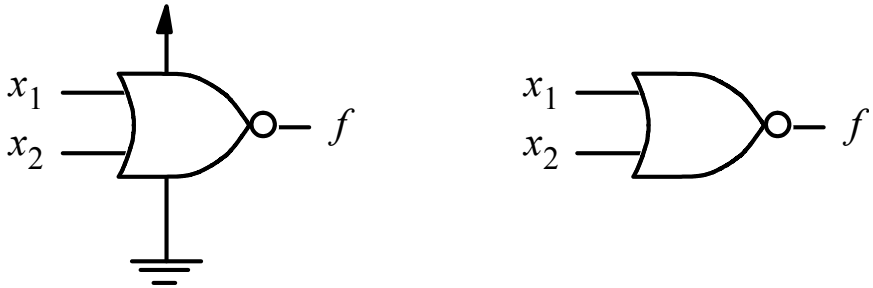
Figure B.6. NMOS realization of a NAND gate.



(a) Circuit

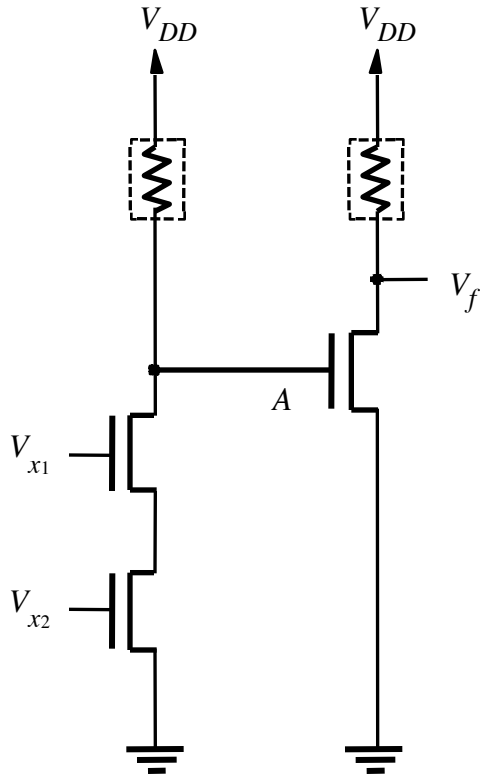
x_1	x_2	f
0	0	1
0	1	0
1	0	0
1	1	0

(b) Truth table



(c) Graphical symbols

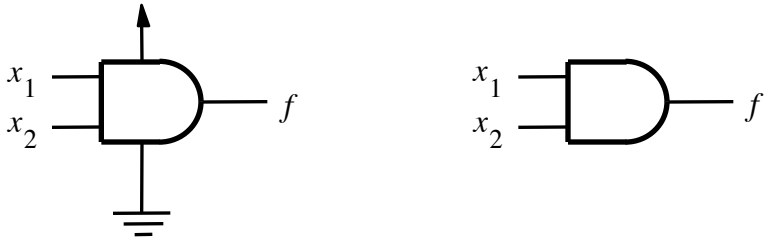
Figure B.7. NMOS realization of a NOR gate.



(a) Circuit

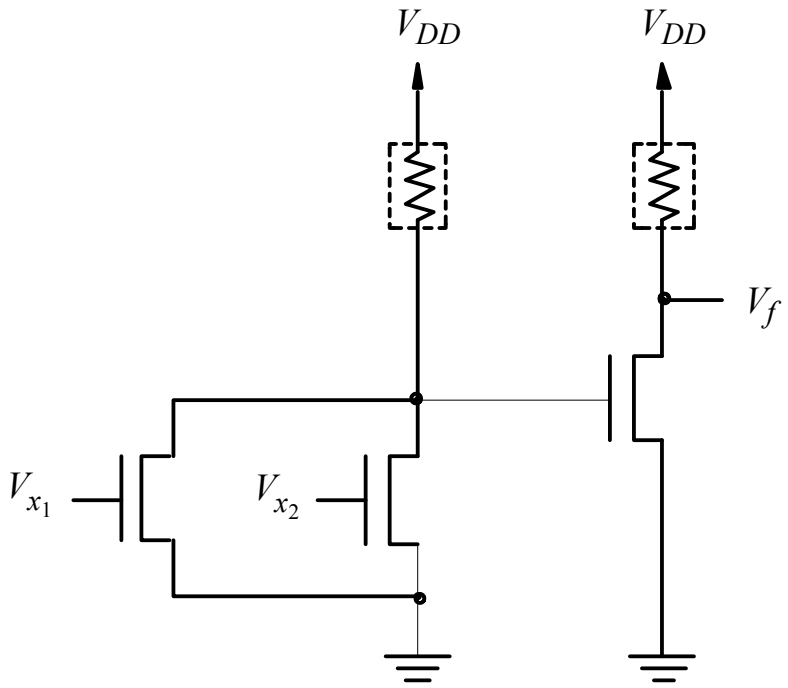
x_1	x_2	f
0	0	0
0	1	0
1	0	0
1	1	1

(b) Truth table



(c) Graphical symbols

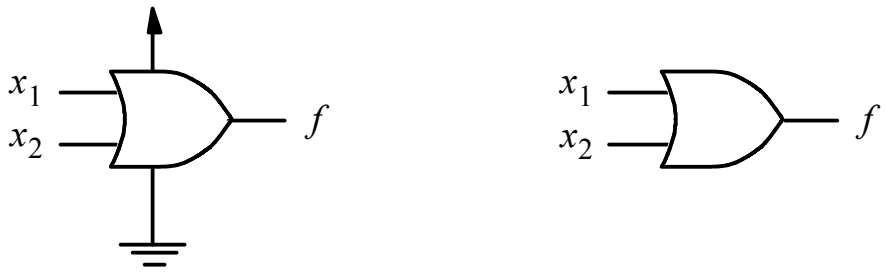
Figure B.8. NMOS realization of an AND gate.



(a) Circuit

x_1	x_2	f
0	0	0
0	1	1
1	0	1
1	1	1

(b) Truth table



(c) Graphical symbols

Figure B.9. NMOS realization of an OR gate.

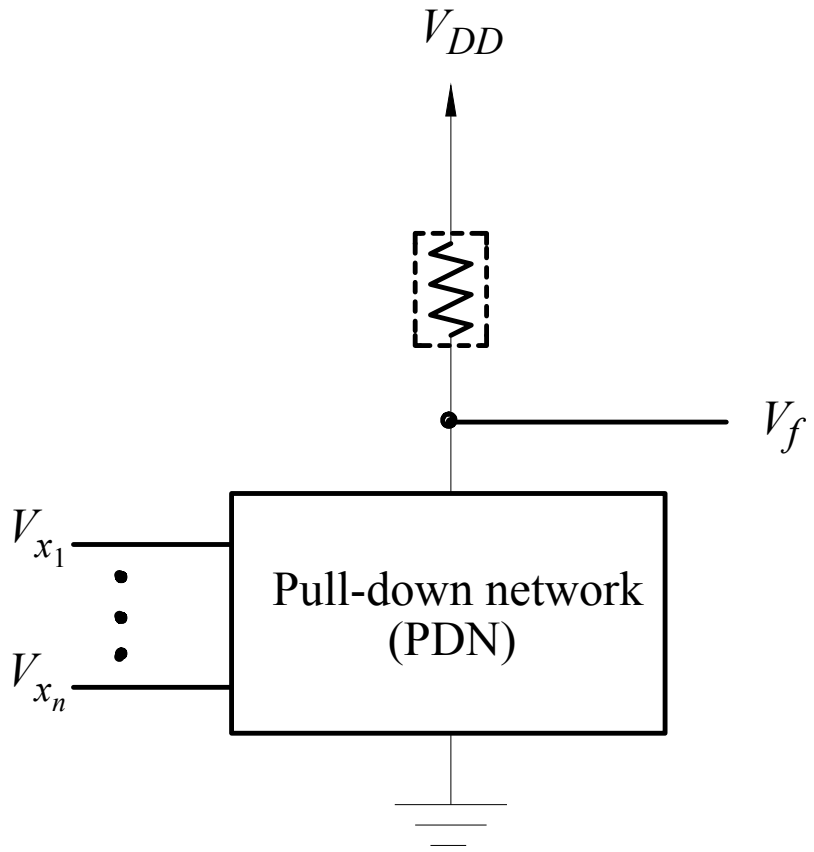


Figure B.10. Structure of an NMOS circuit.

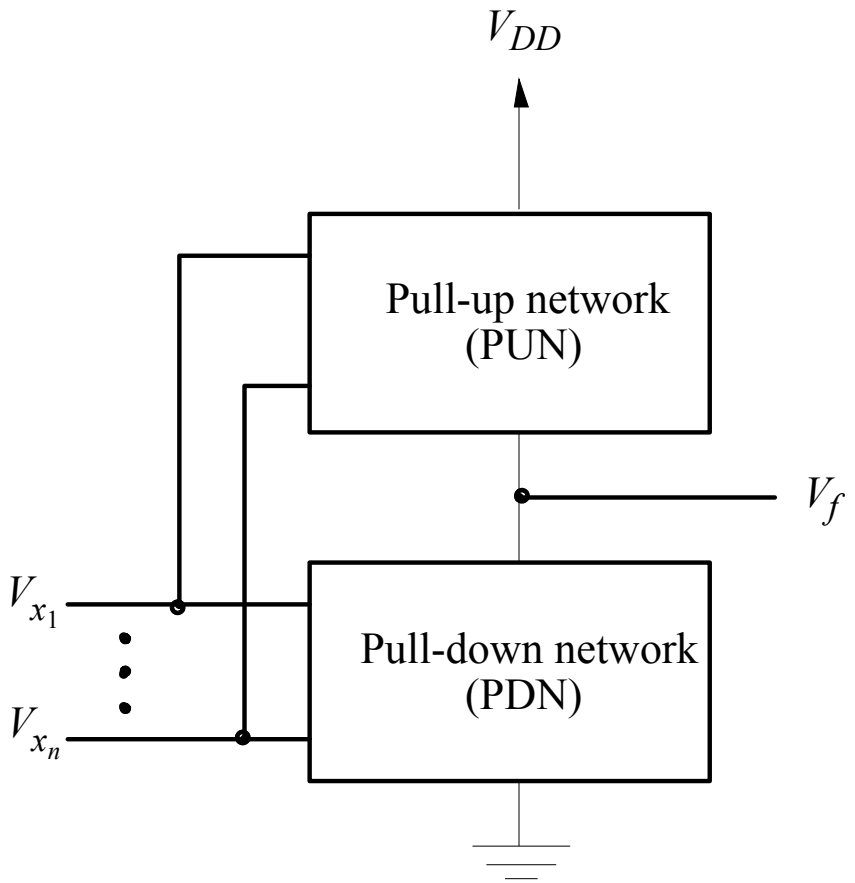
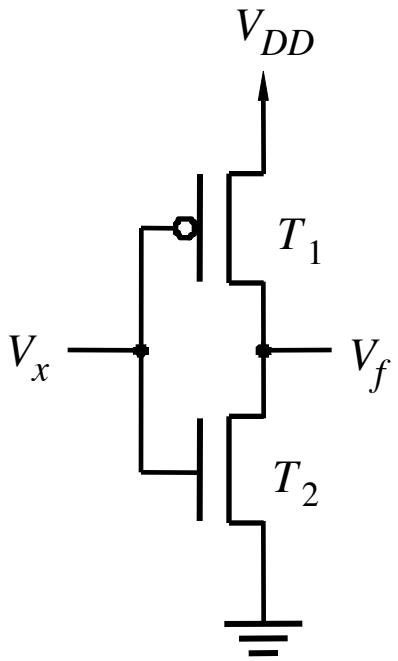


Figure B.11. Structure of a CMOS circuit.

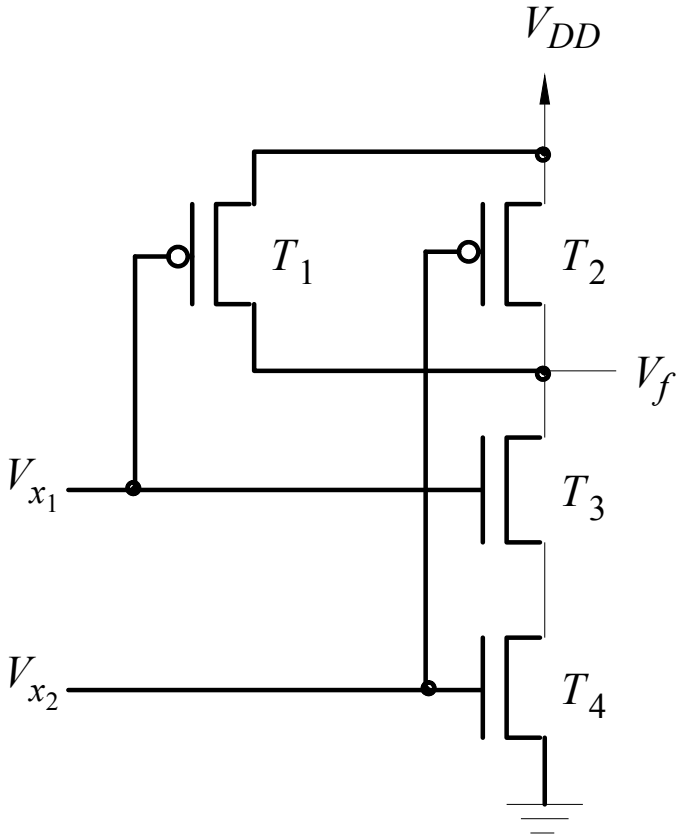


(a) Circuit

x	T_1	T_2	f
0	on	off	1
1	off	on	0

(b) Truth table and transistor states

Figure B.12. CMOS realization of a NOT gate.

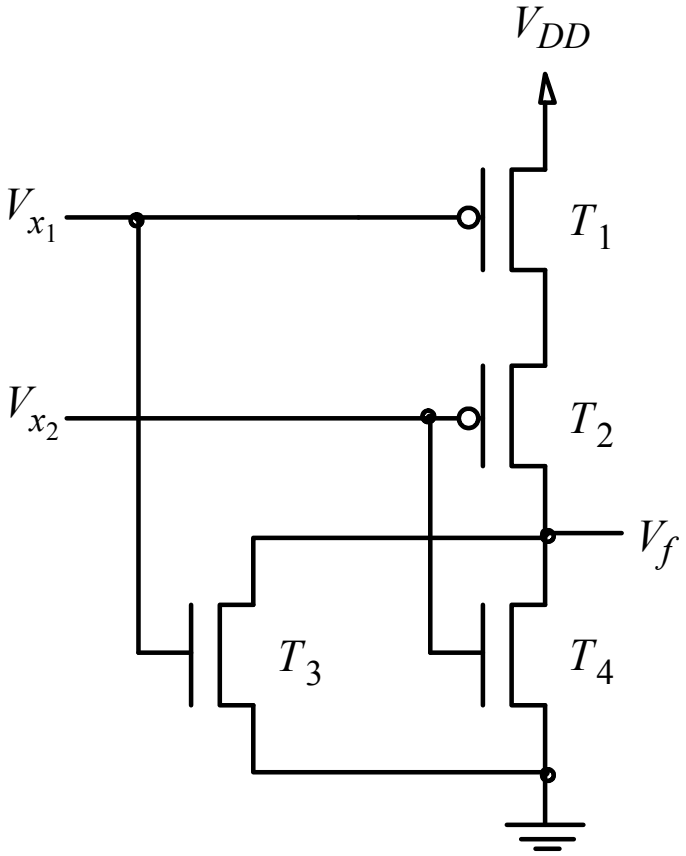


(a) Circuit

x_1	x_2	T_1	T_2	T_3	T_4	f
0	0	on	on	off	off	1
0	1	on	off	off	on	1
1	0	off	on	on	off	1
1	1	off	off	on	on	0

(b) Truth table and transistor state

Figure B.13. CMOS realization of a NAND gate.



(a) Circuit

x_1	x_2	T_1	T_2	T_3	T_4	f
0	0	on	on	off	off	1
0	1	on	off	off	on	0
1	0	off	on	on	off	0
1	1	off	off	on	on	0

(b) Truth table and transistor state

Figure B.14. CMOS realization of a NOR gate.

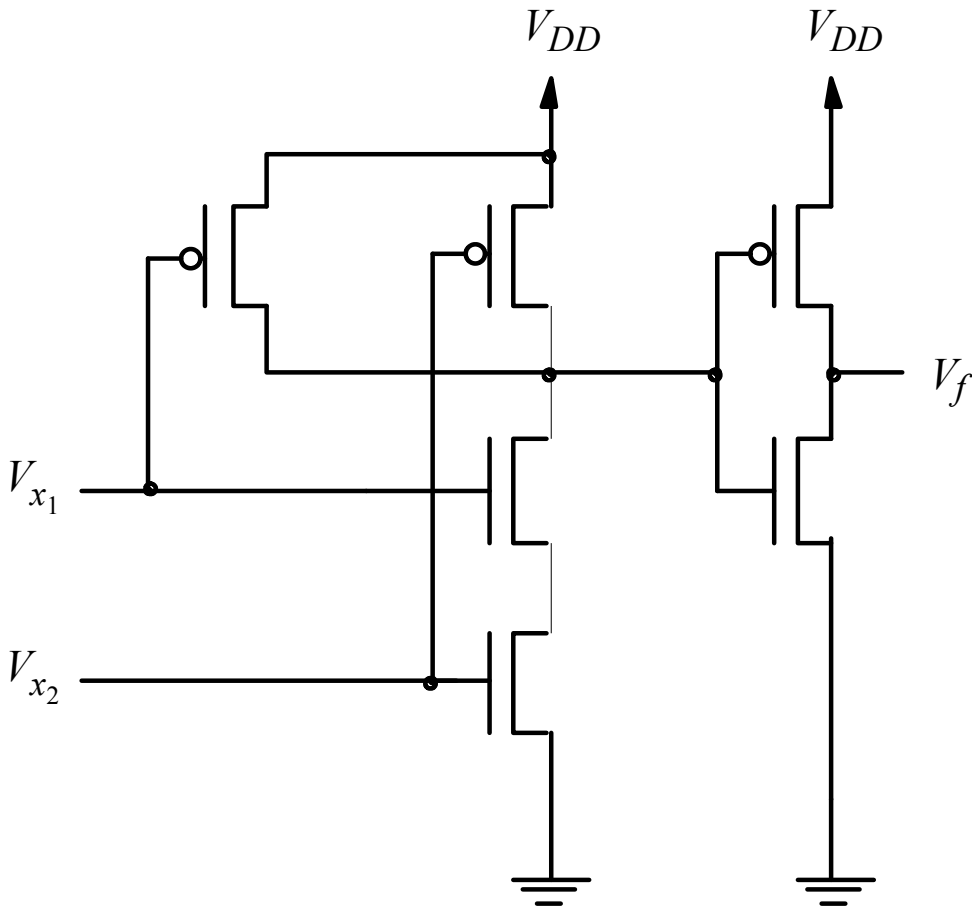


Figure B.15. CMOS realization of an AND gate.

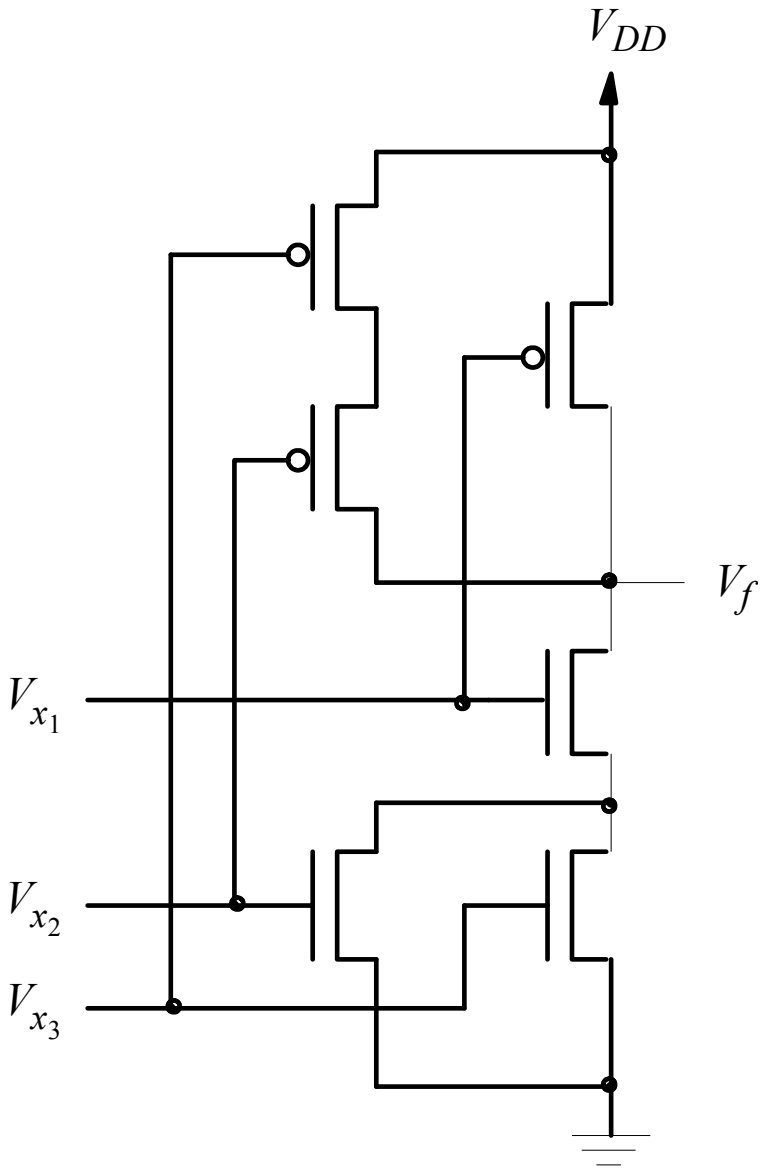


Figure B.16. The circuit for Example B.1.

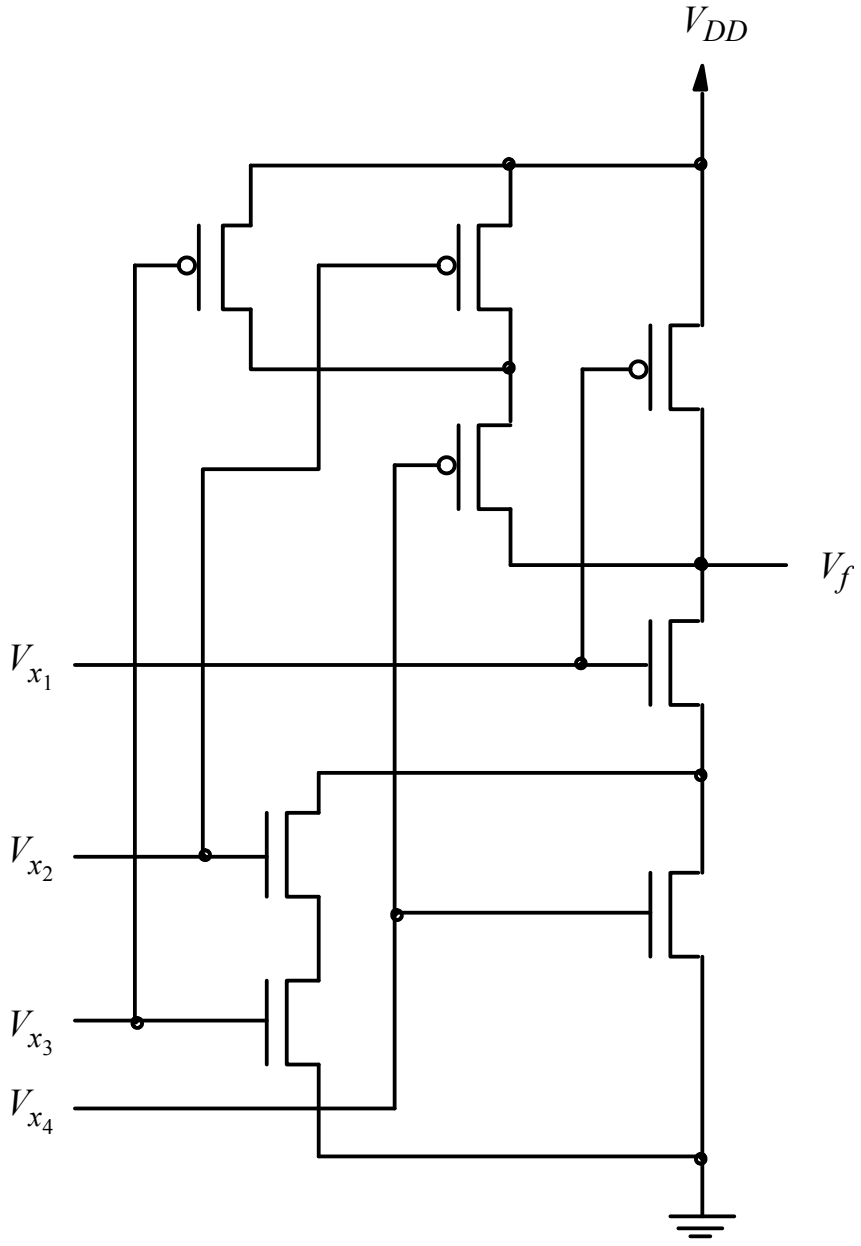
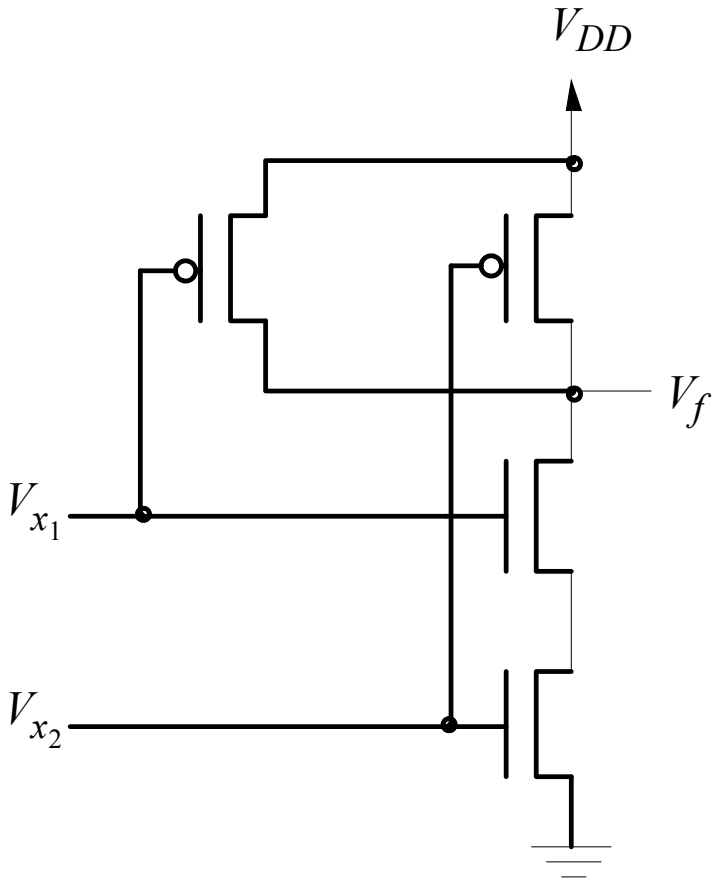


Figure B.17. The circuit for Example B.2.



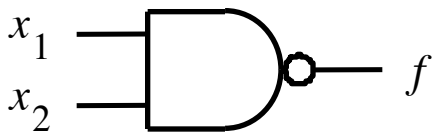
(a) Circuit

V_{x_1}	V_{x_2}	V_f
L	L	H
L	H	H
H	L	H
H	H	L

(b) Voltage levels

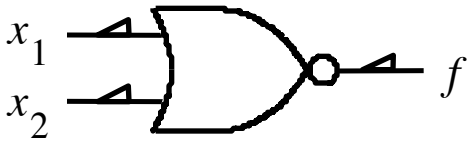
Figure B.18. Voltage levels in the circuit in Figure B.13.

x_1	x_2	f
0	0	1
0	1	1
1	0	1
1	1	0



(a) Positive logic truth table and gate symbol

x_1	x_2	f
1	1	0
1	0	0
0	1	0
0	0	1

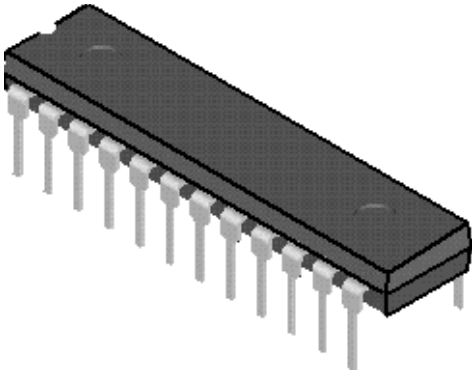


(b) Negative logic truth table and gate symbol

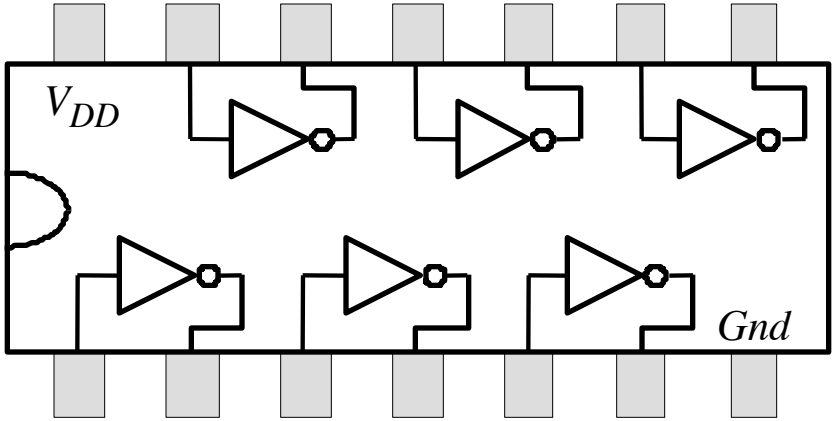
Figure B.19. Interpretation of the circuit in Figure B.18.

Please see “portrait orientation” PowerPoint file for Chapter B

Figure B.20. Interpretation of voltage levels.



(a) Dual-inline package



(b) Structure of 7404 chip

Figure B.21. A 7400-series chip.

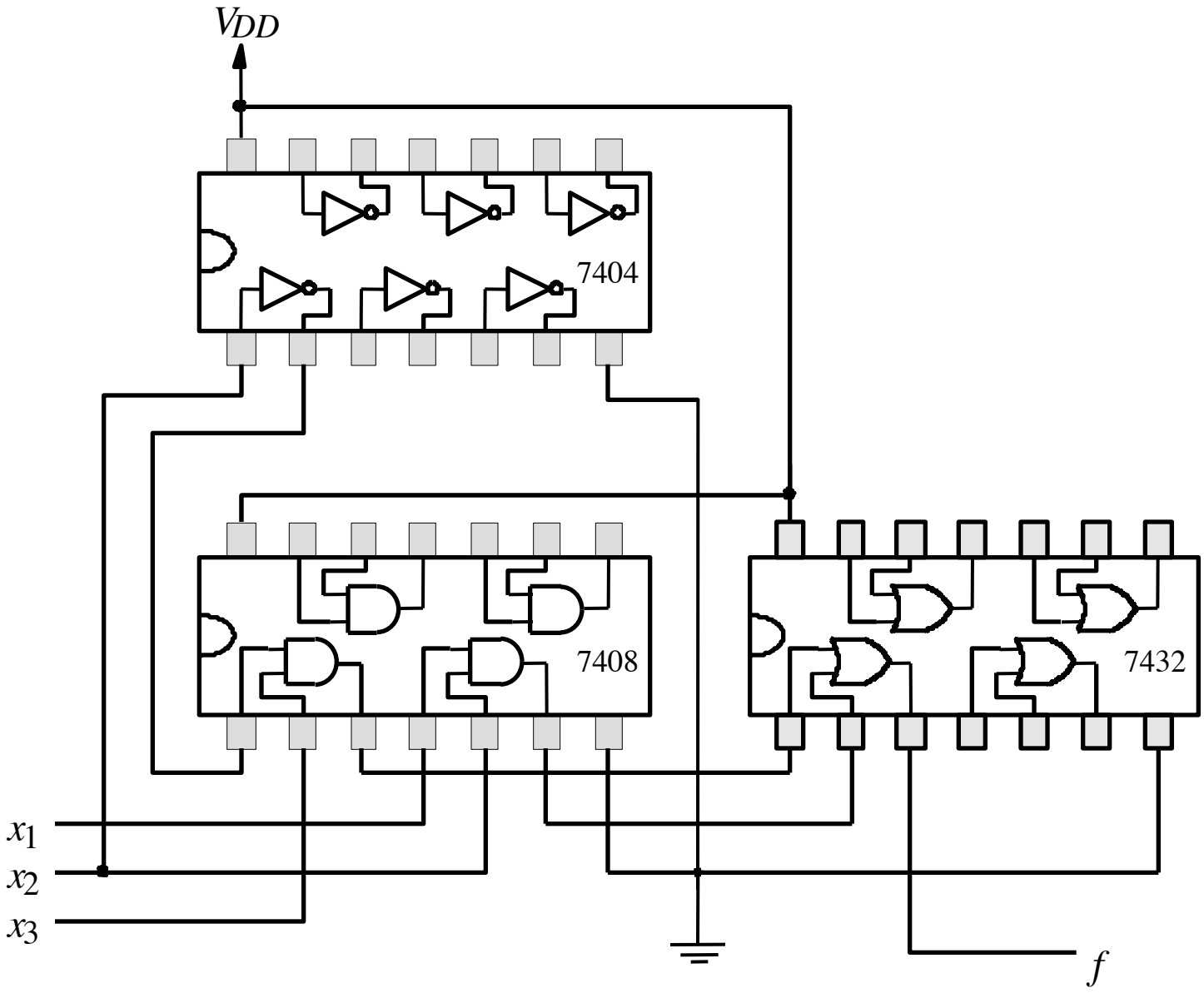


Figure B.22. An implementation of $f = x_1x_2 + \bar{x}_2x_3$.

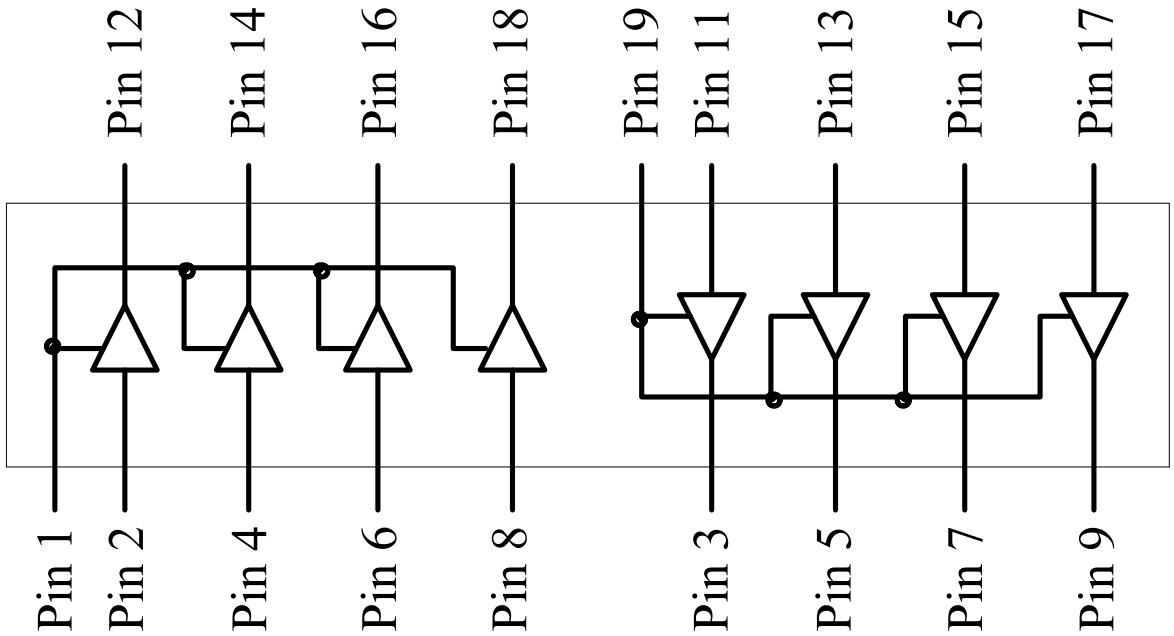


Figure B.23. The 74244 buffer chip.

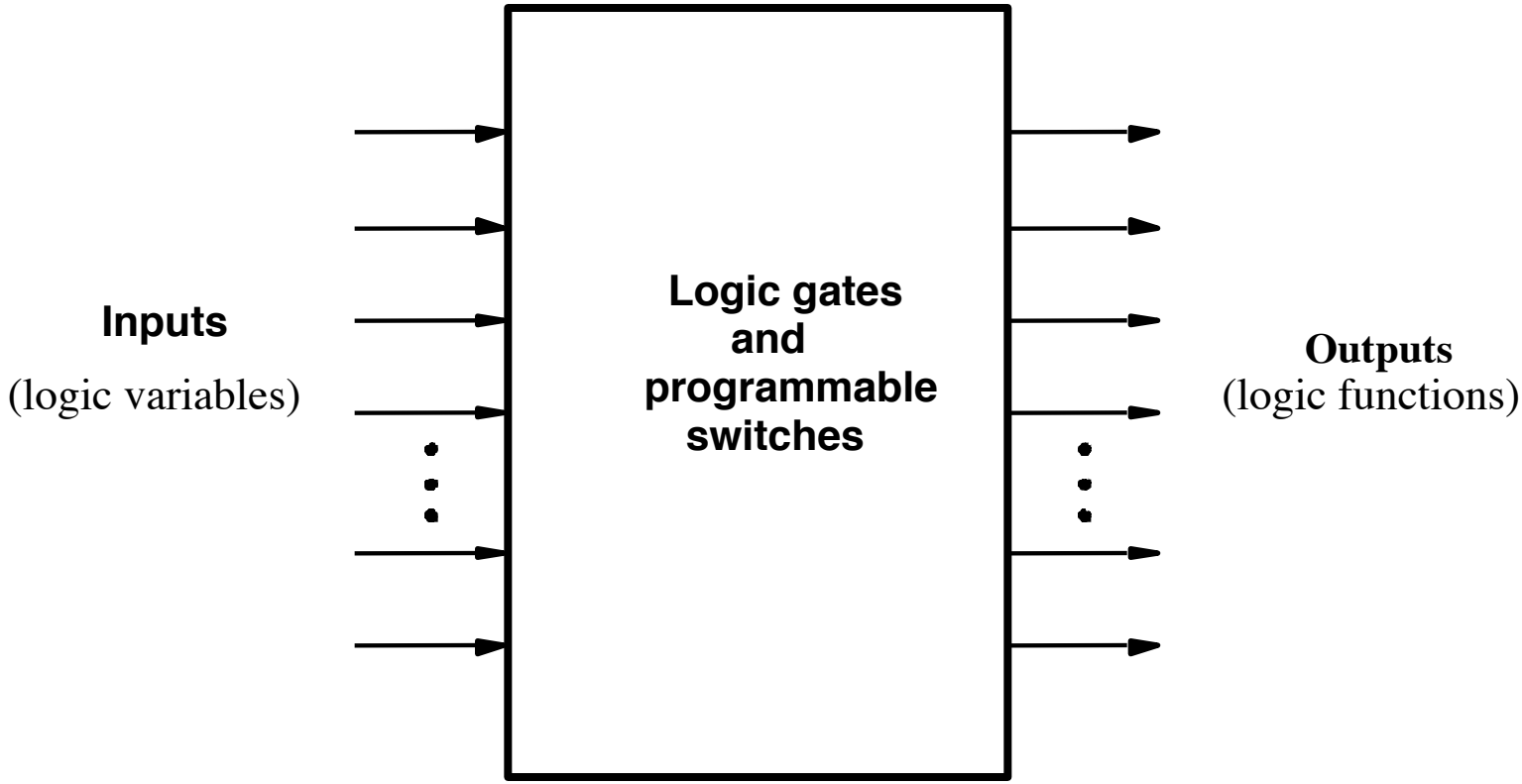


Figure B.24. Programmable logic device as a black box.

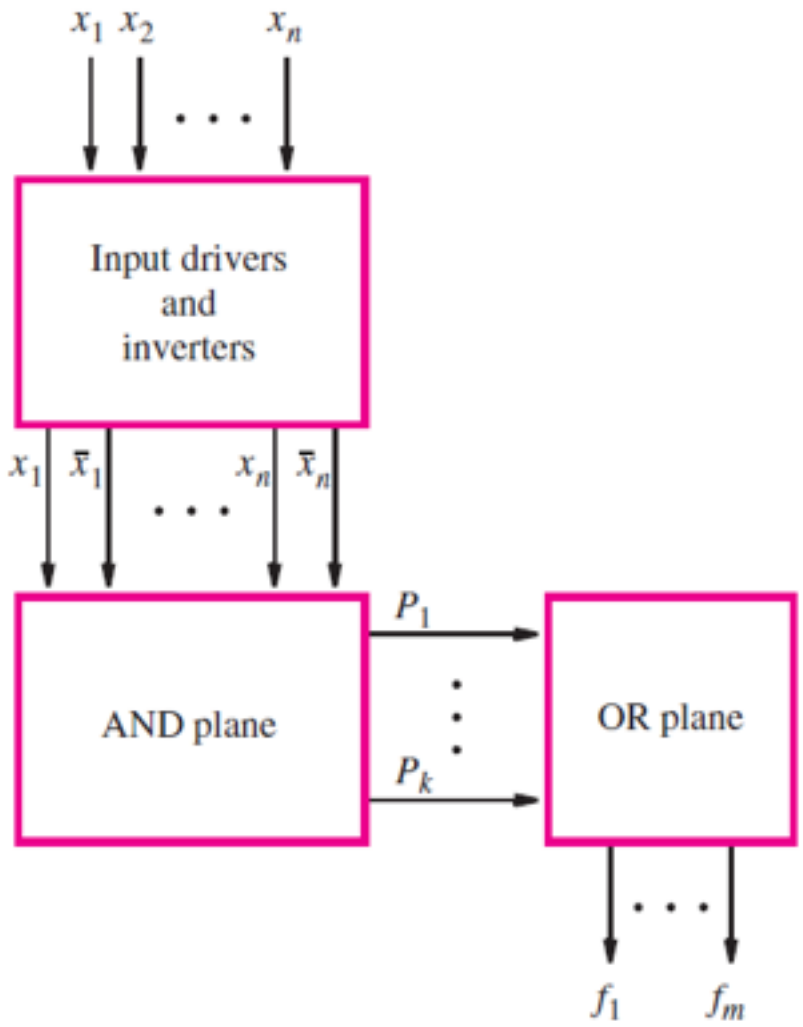


Figure B.25. General structure of a PLA.

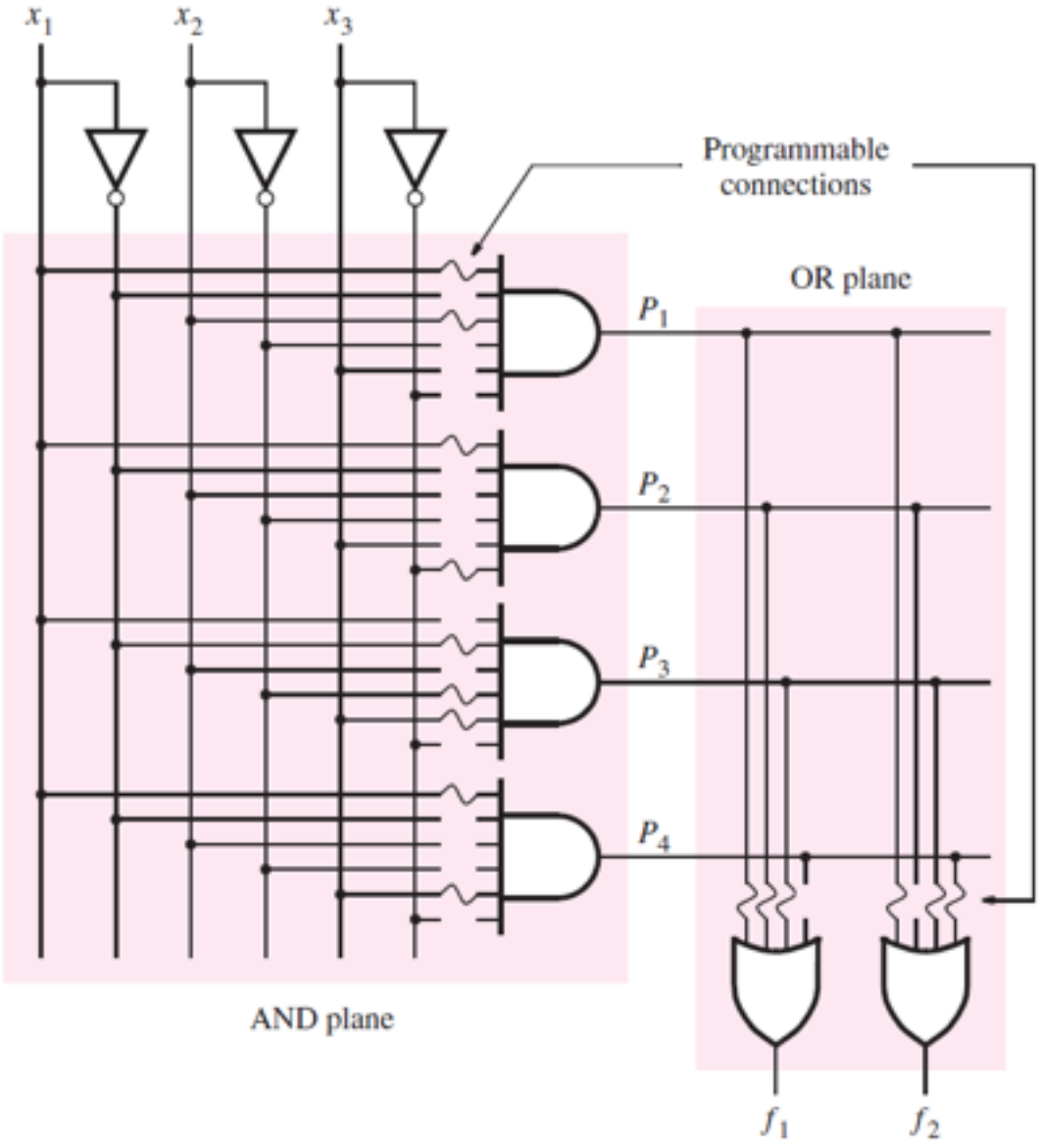


Figure B.26. Gate-level diagram of a PLA.

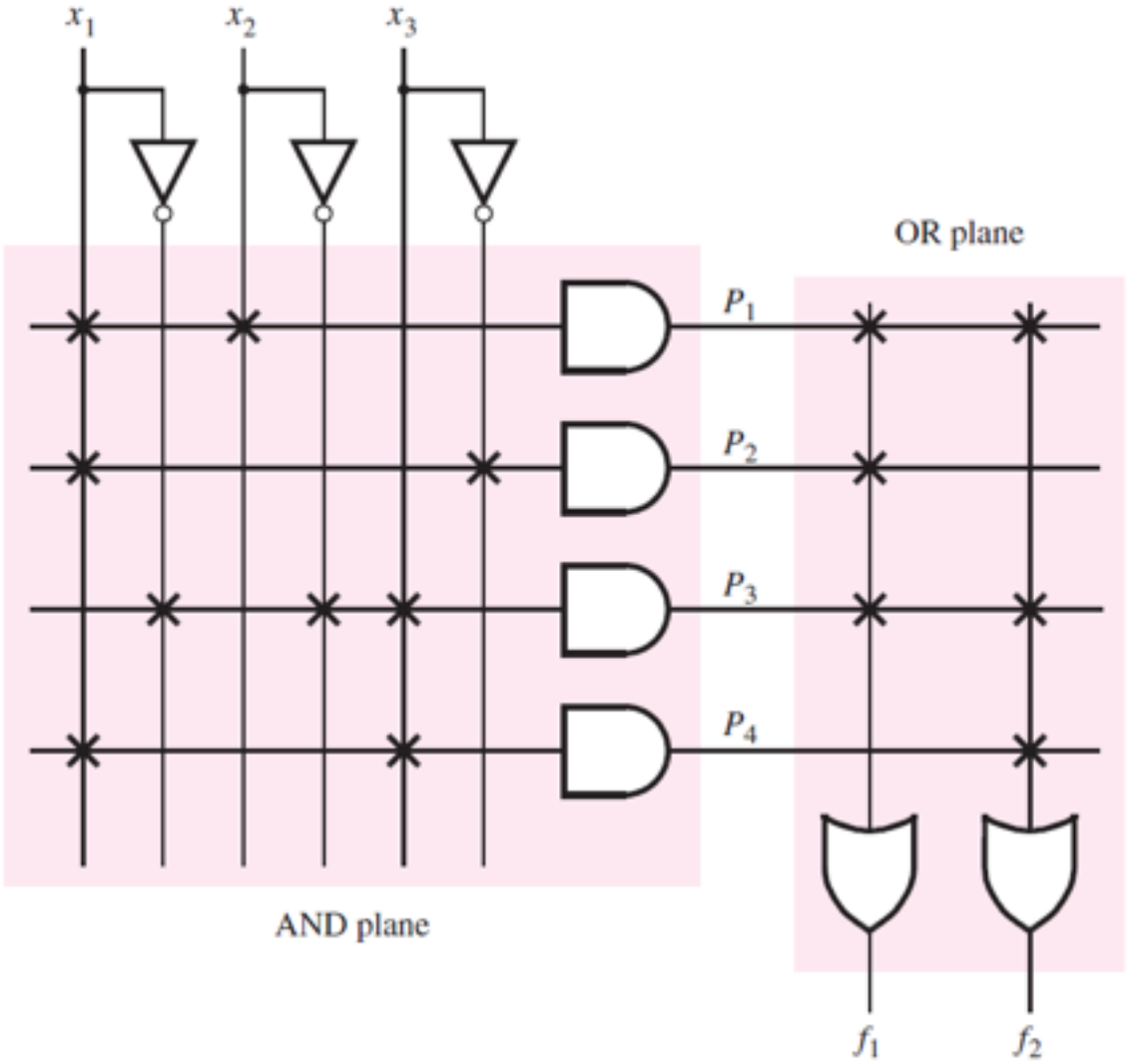


Figure B.27. Customary schematic for the PLA in Figure B.26.

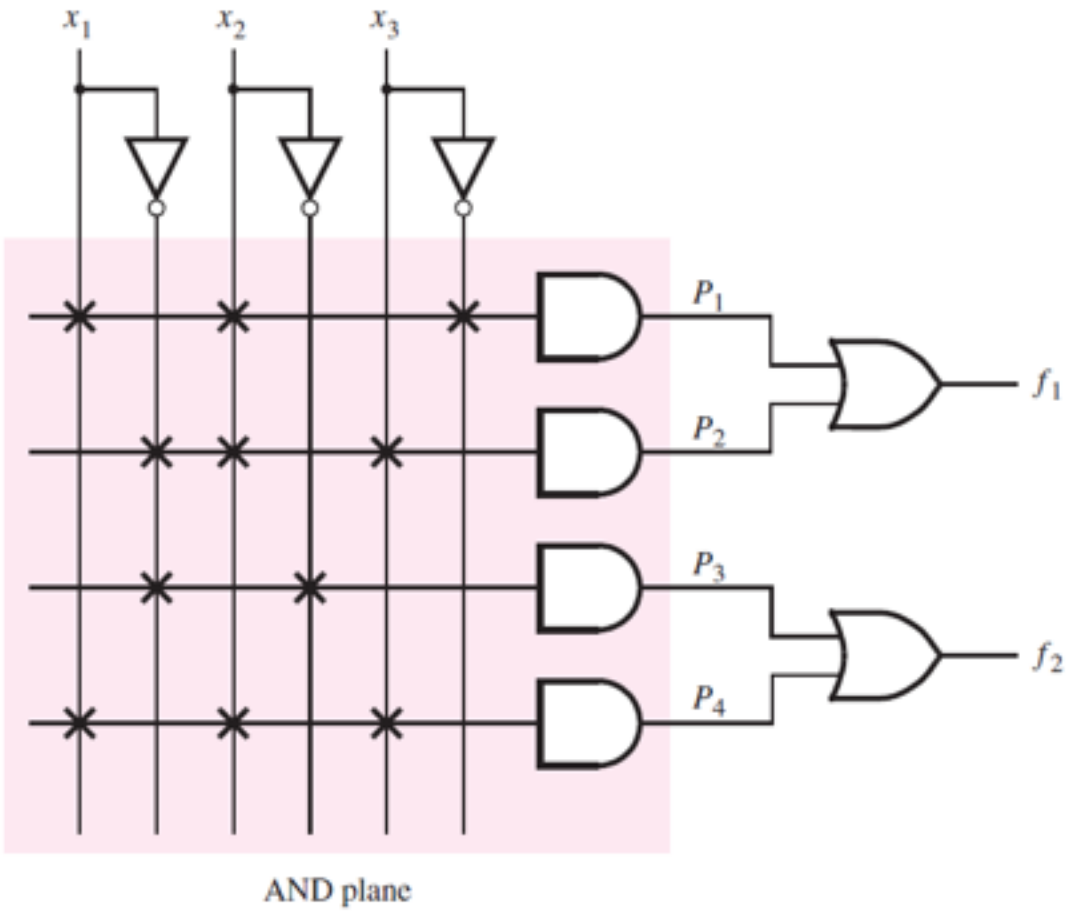


Figure B.28. An example of a PLA.

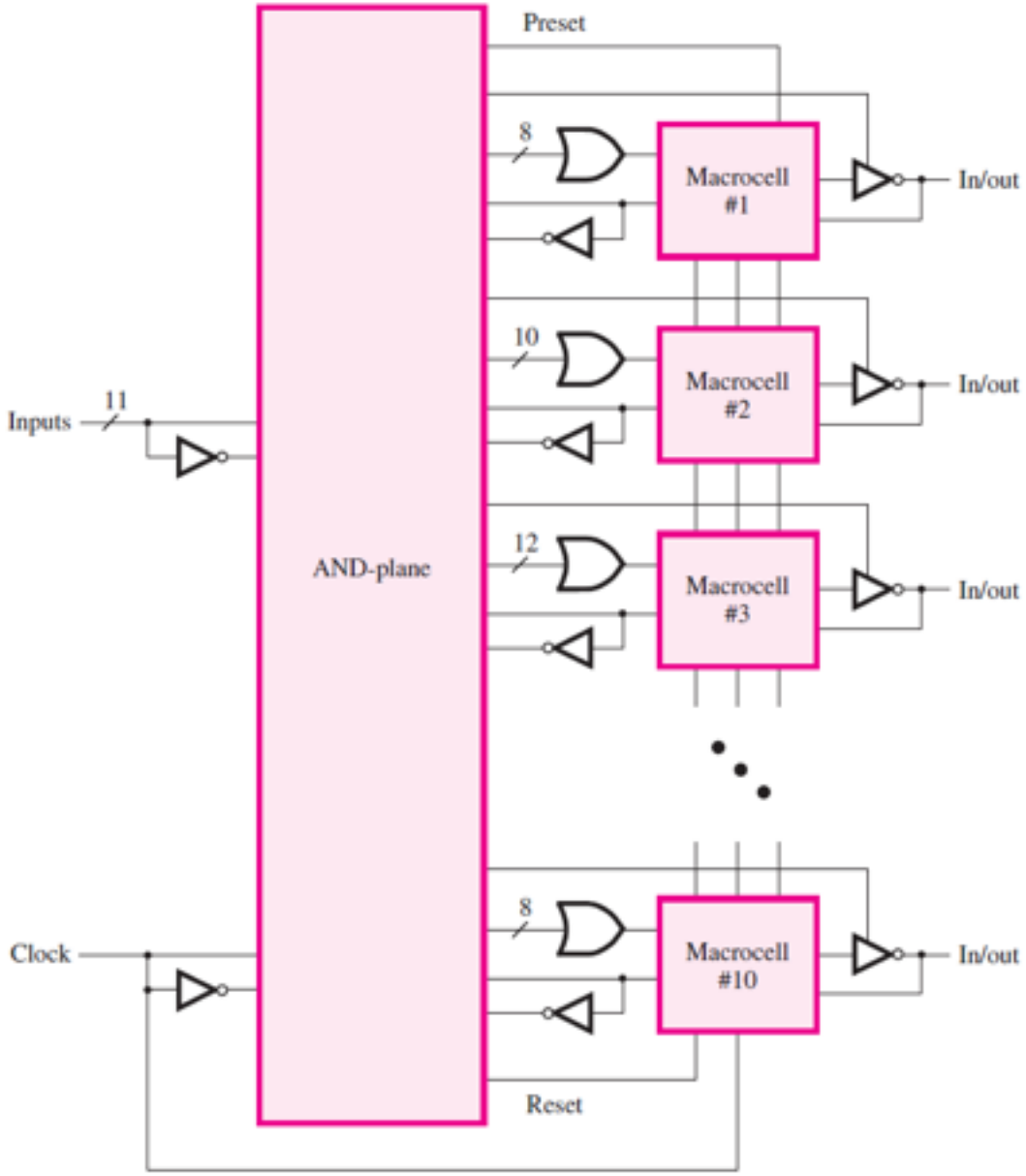


Figure B.29. The 22V10 PAL device.

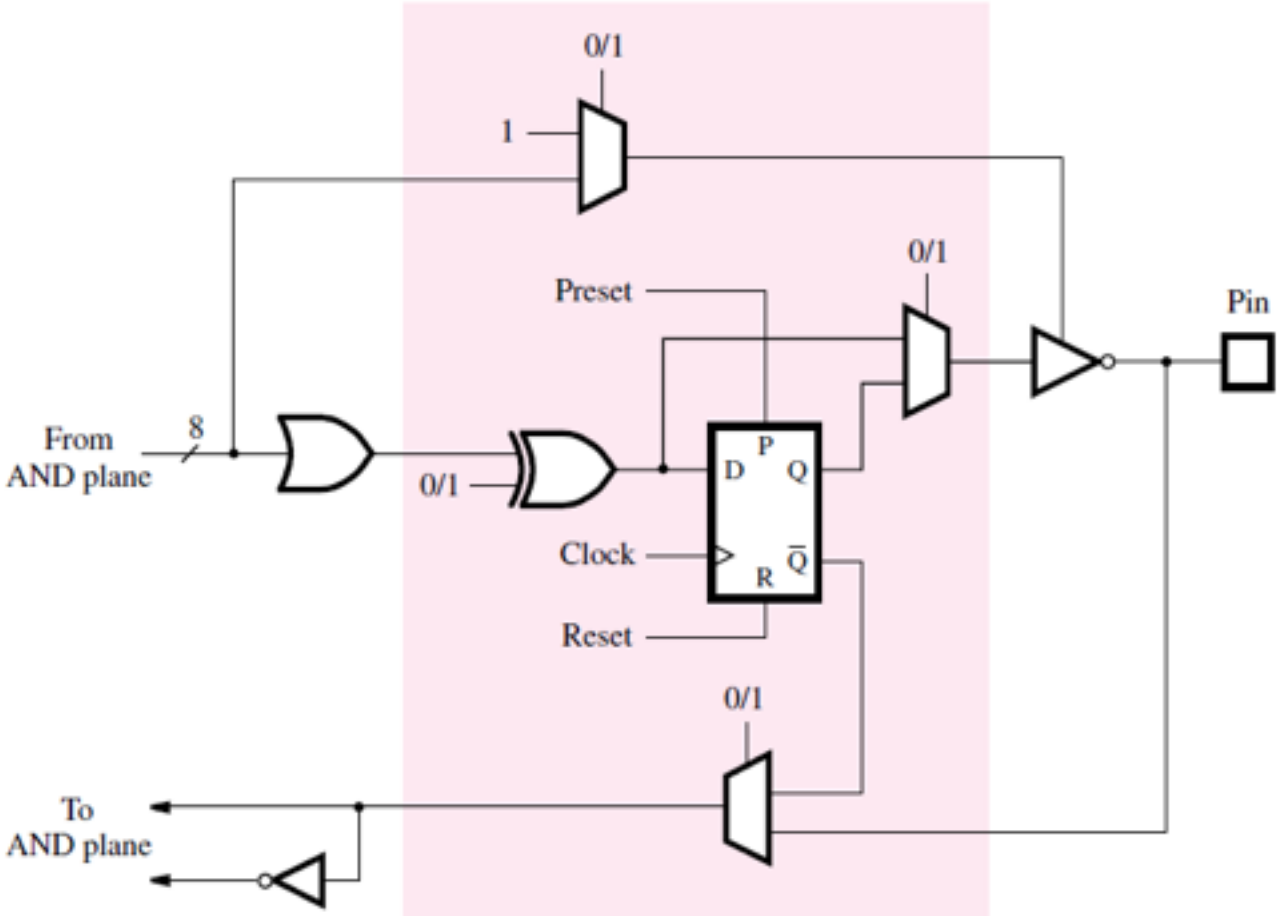


Figure B.30. The 22V10 macrocell.

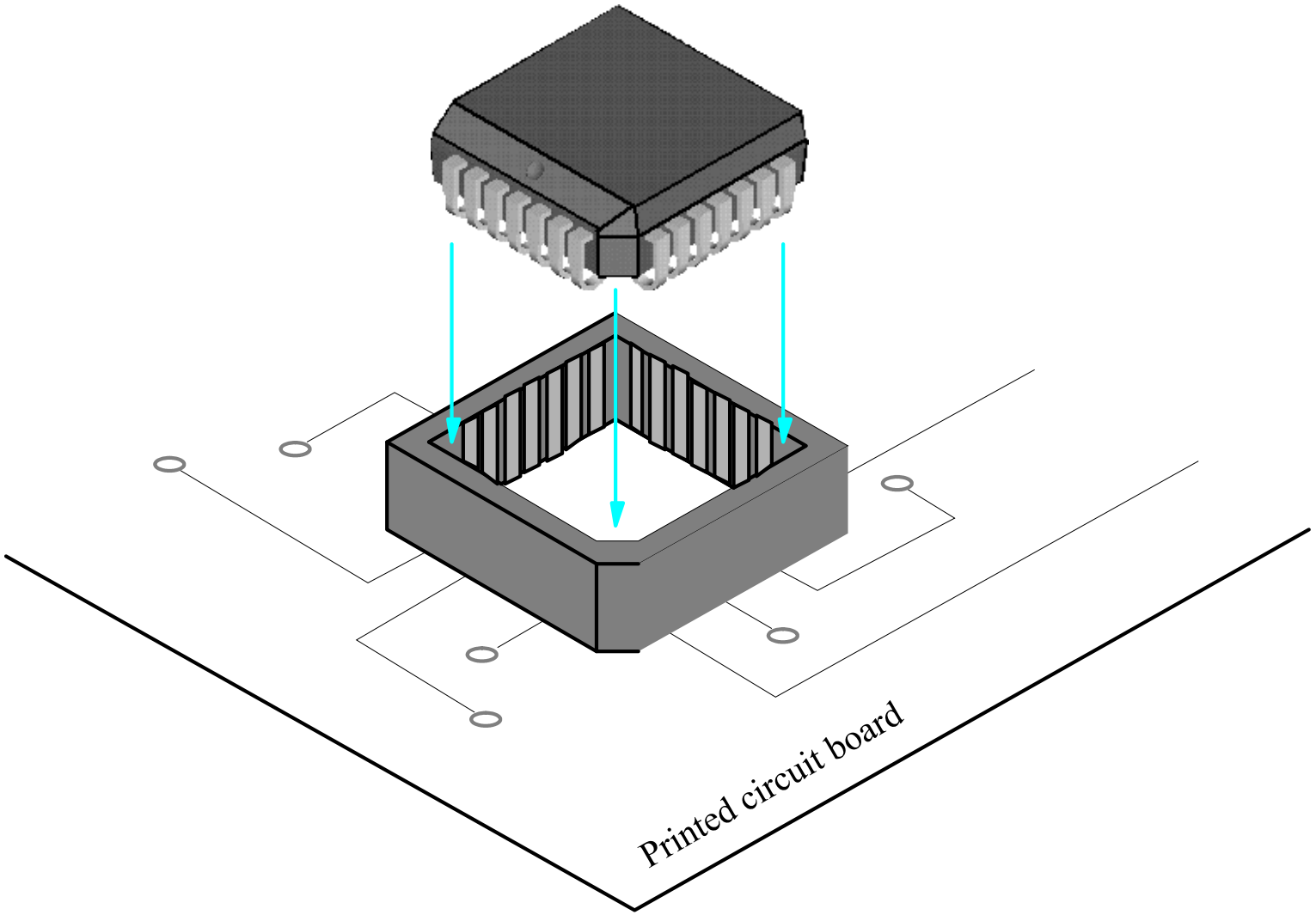


Figure B.31. A PLCC package with socket.

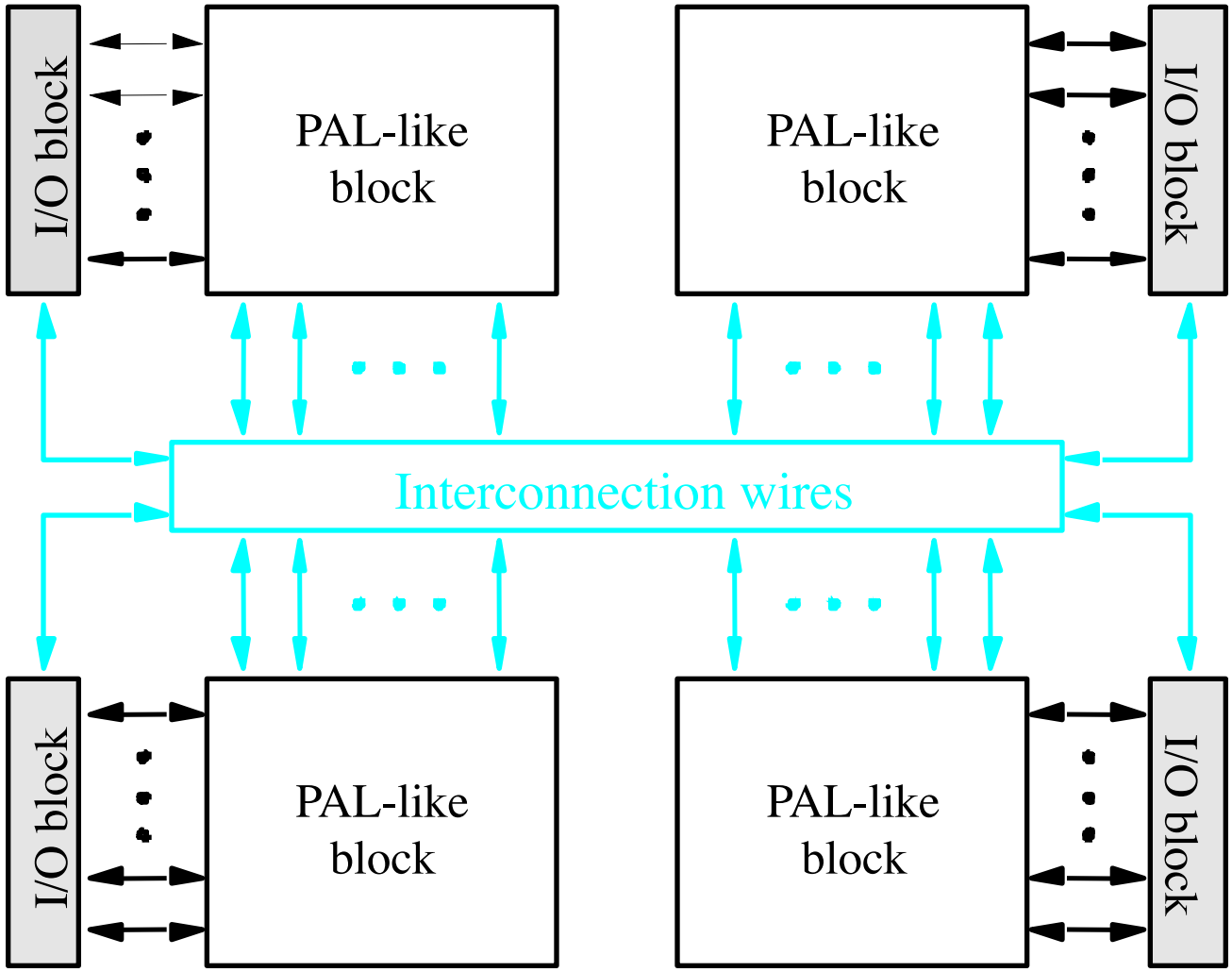


Figure B.32. Structure of a complex programmable logic device (CPLD).

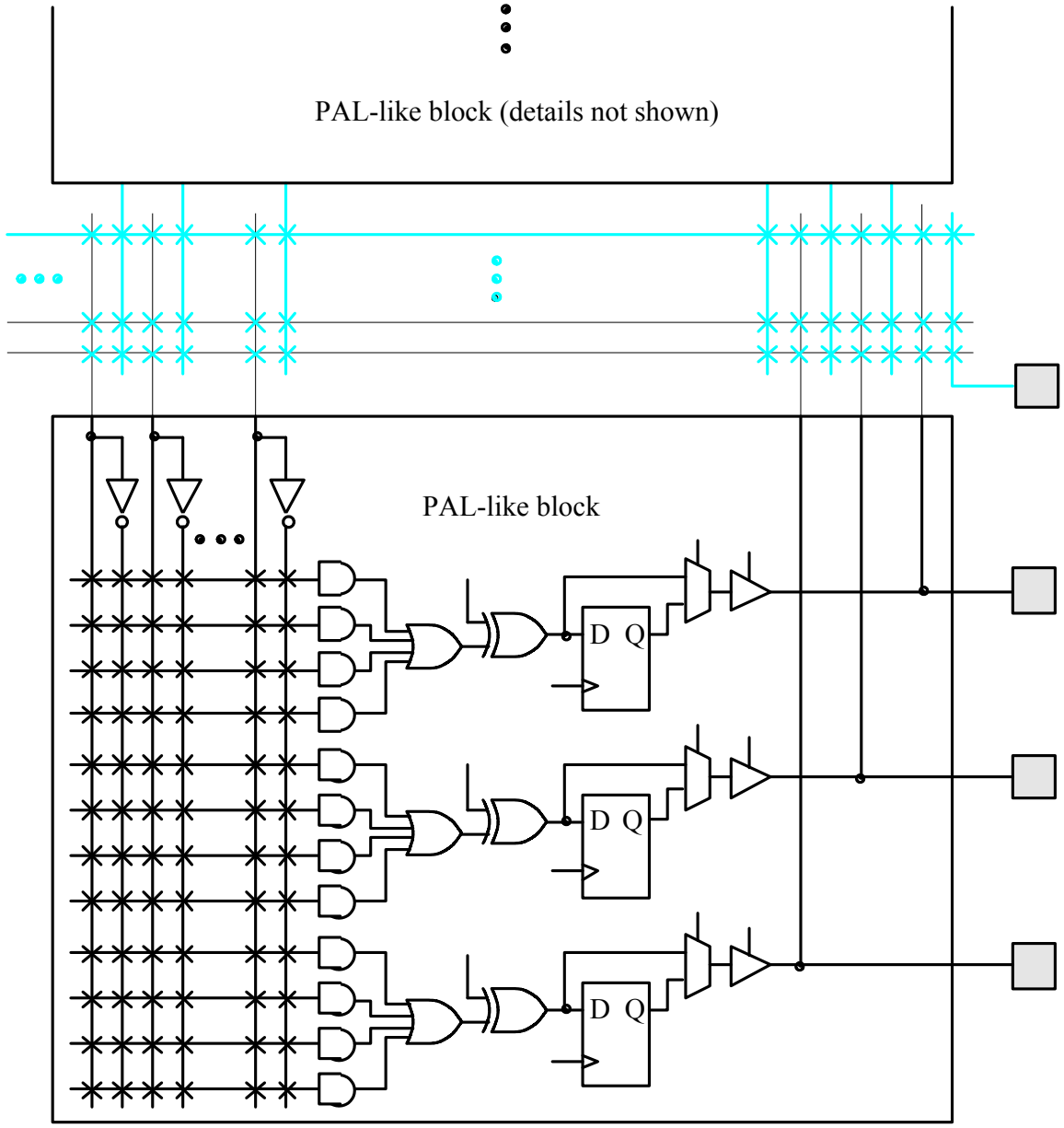
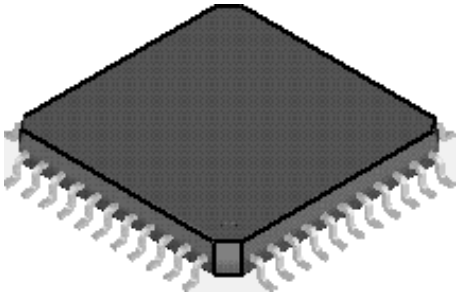
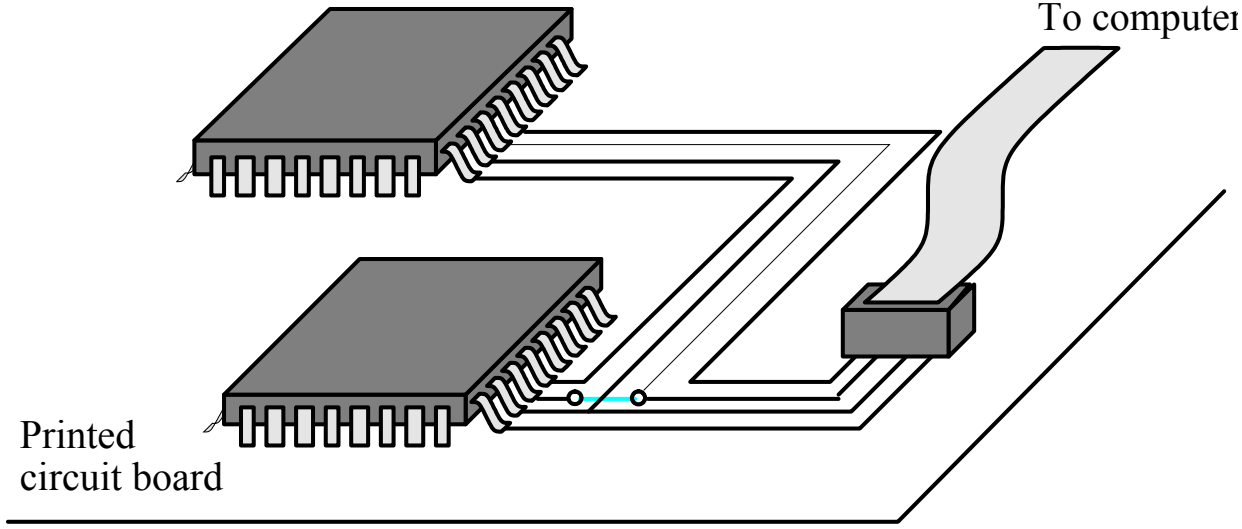


Figure B.33. A section of the CPLD in Figure B.32.



(a) CPLD in a Quad Flat Pack (QFP) package



(b) JTAG programming

Figure B.34. CPLD packaging and programming.

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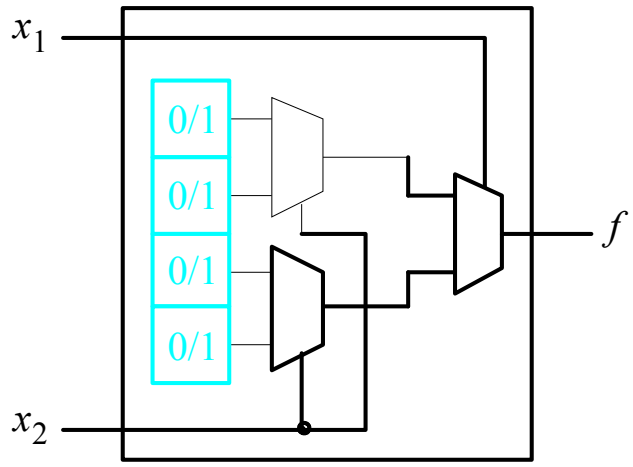
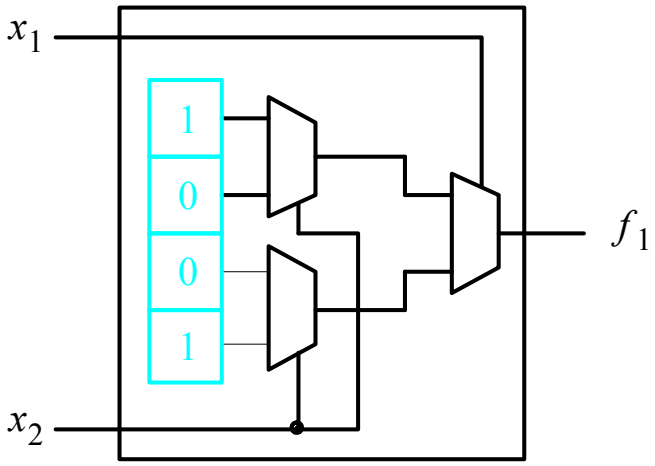
Figure B.35. A field-programmable gate array (FPGA).



(a) Circuit for a two-input LUT

x_1	x_2	f_1
0	0	1
0	1	0
1	0	0
1	1	1

(b) $f_1 = \bar{x}_1\bar{x}_2 + x_1x_2$



(c) Storage cell contents in the LUT

Figure B.36. A two-input lookup table (LUT).

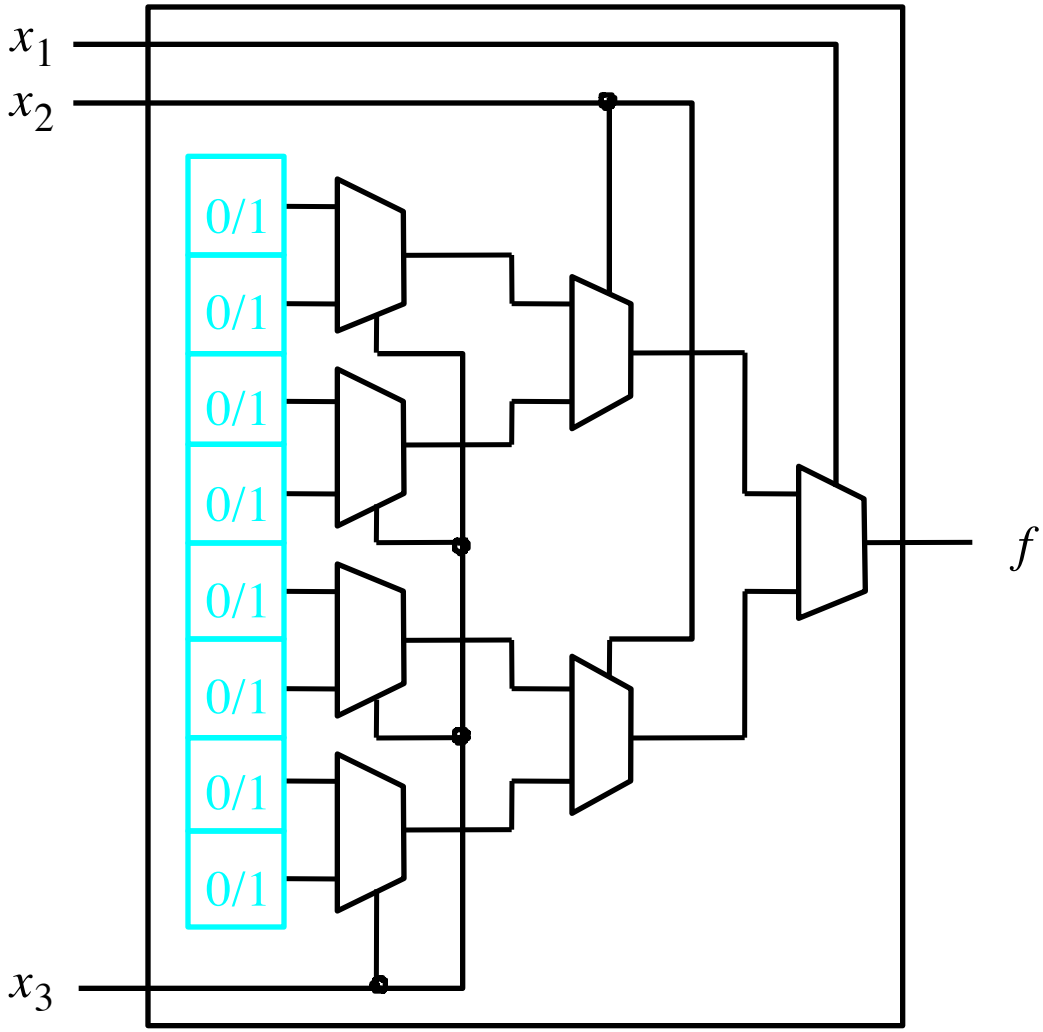


Figure B.37. A three-input LUT.

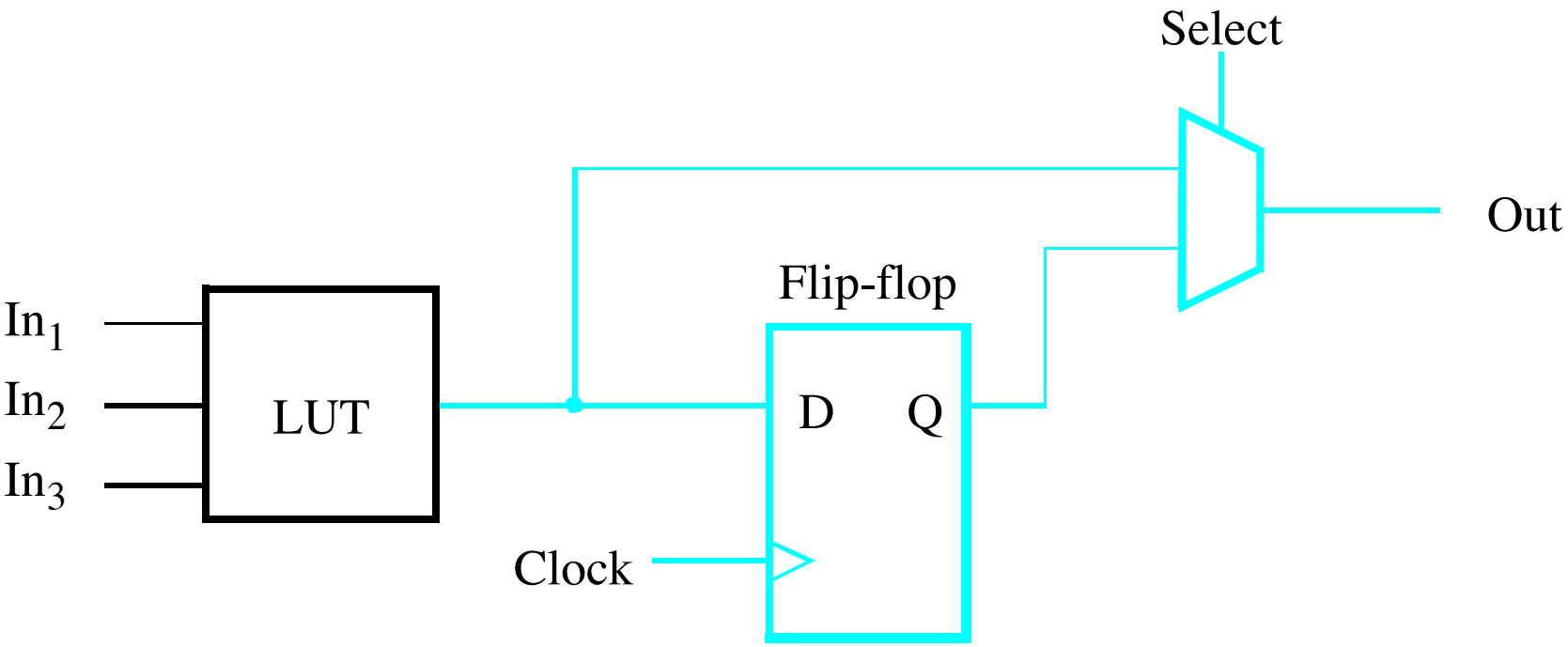


Figure B.38. Inclusion of a flip-flop in an FPGA logic block.

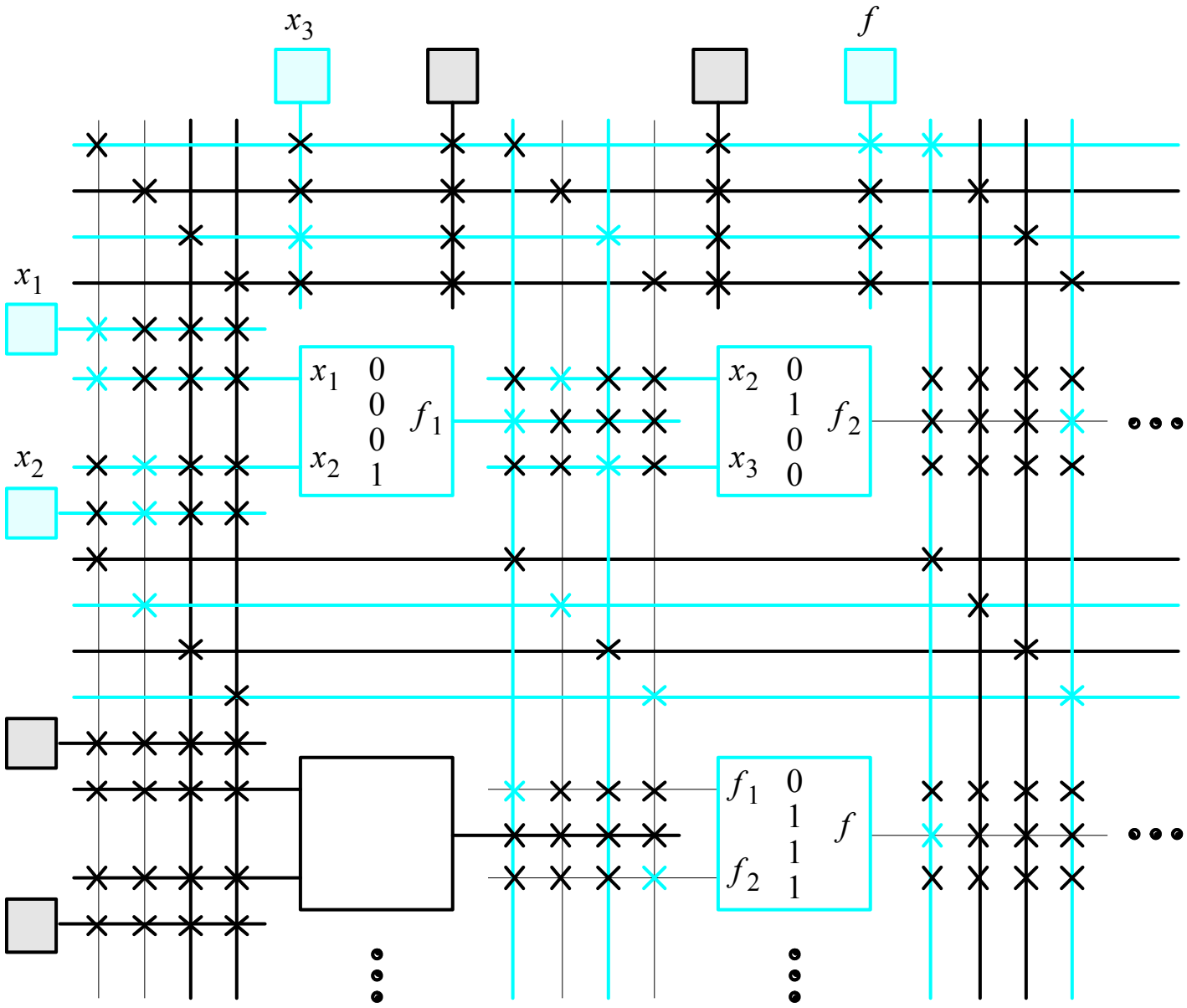


Figure B.39. A section of a programmed FPGA.

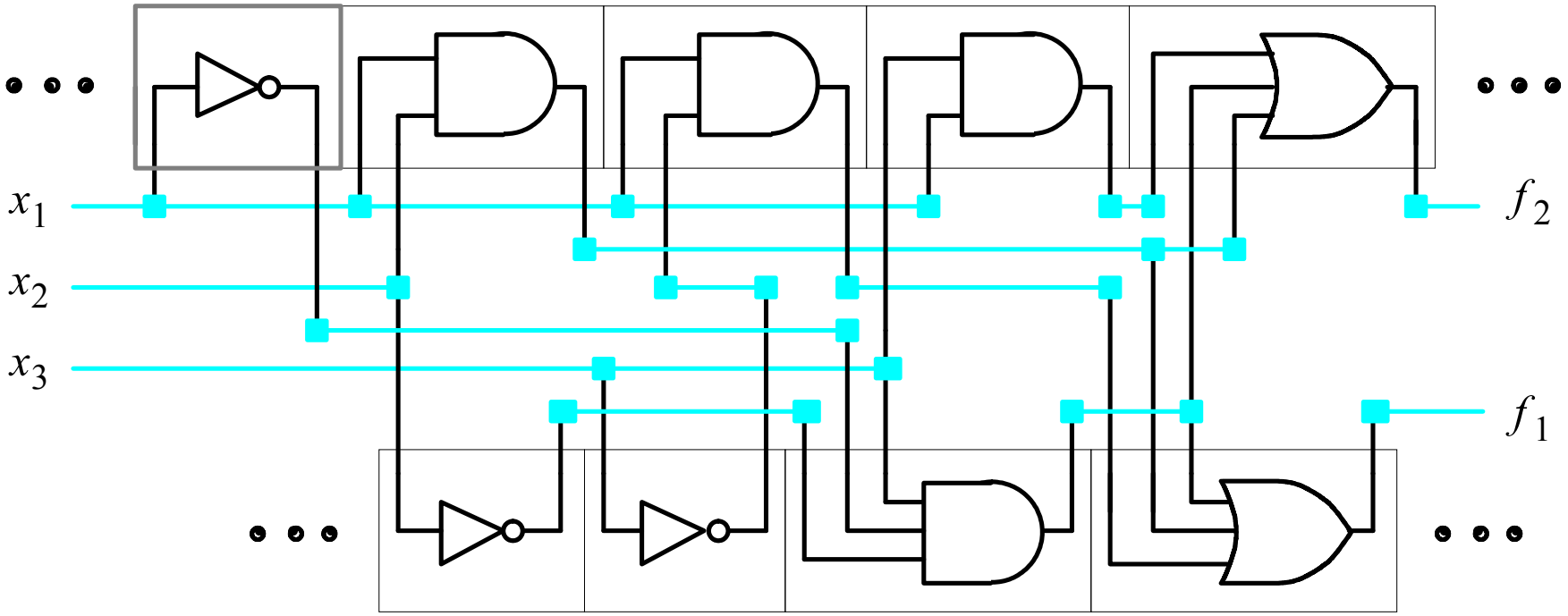


Figure B.40. A section of two rows in a standard-cell chip.

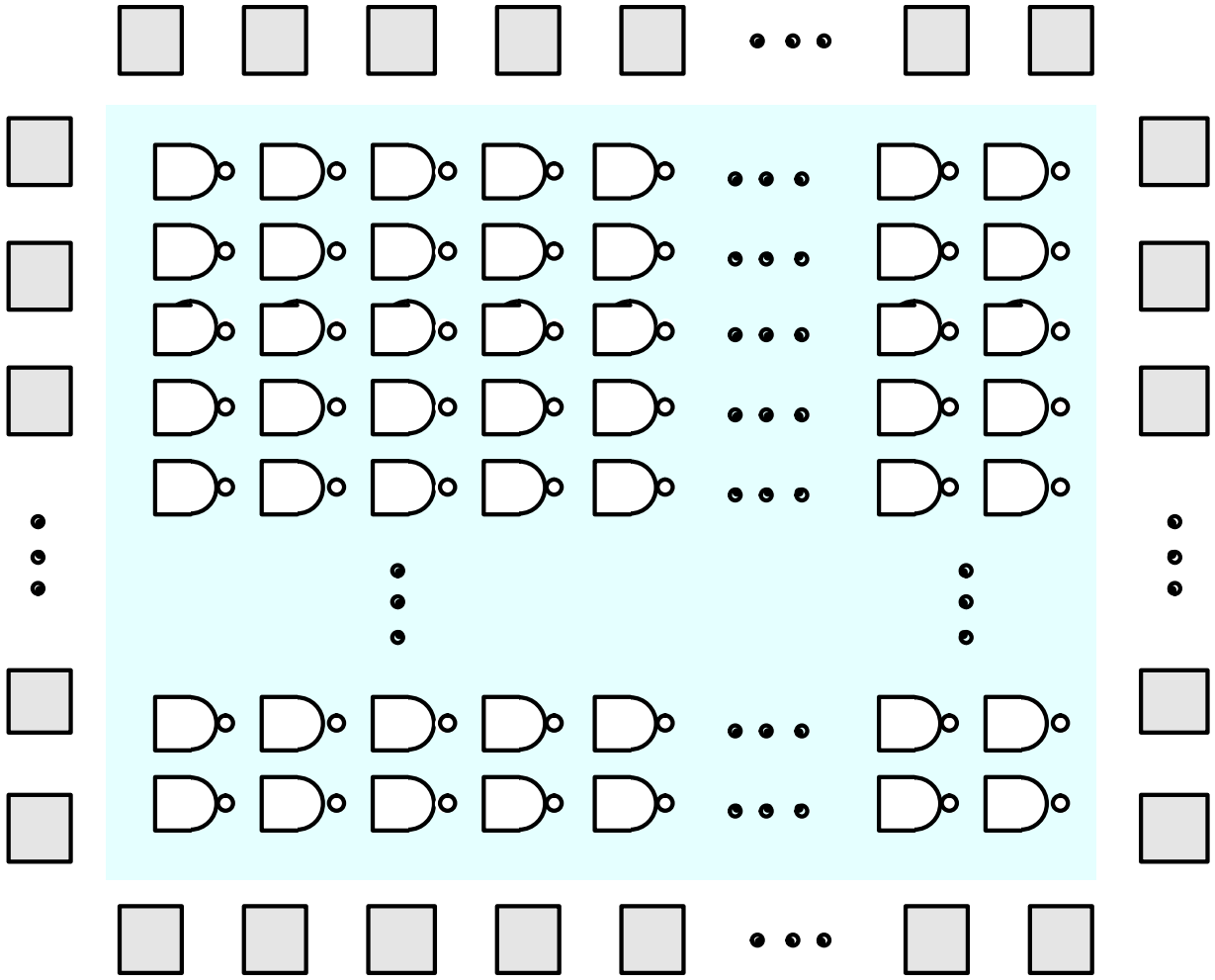


Figure B.41. A sea-of-gates gate array.

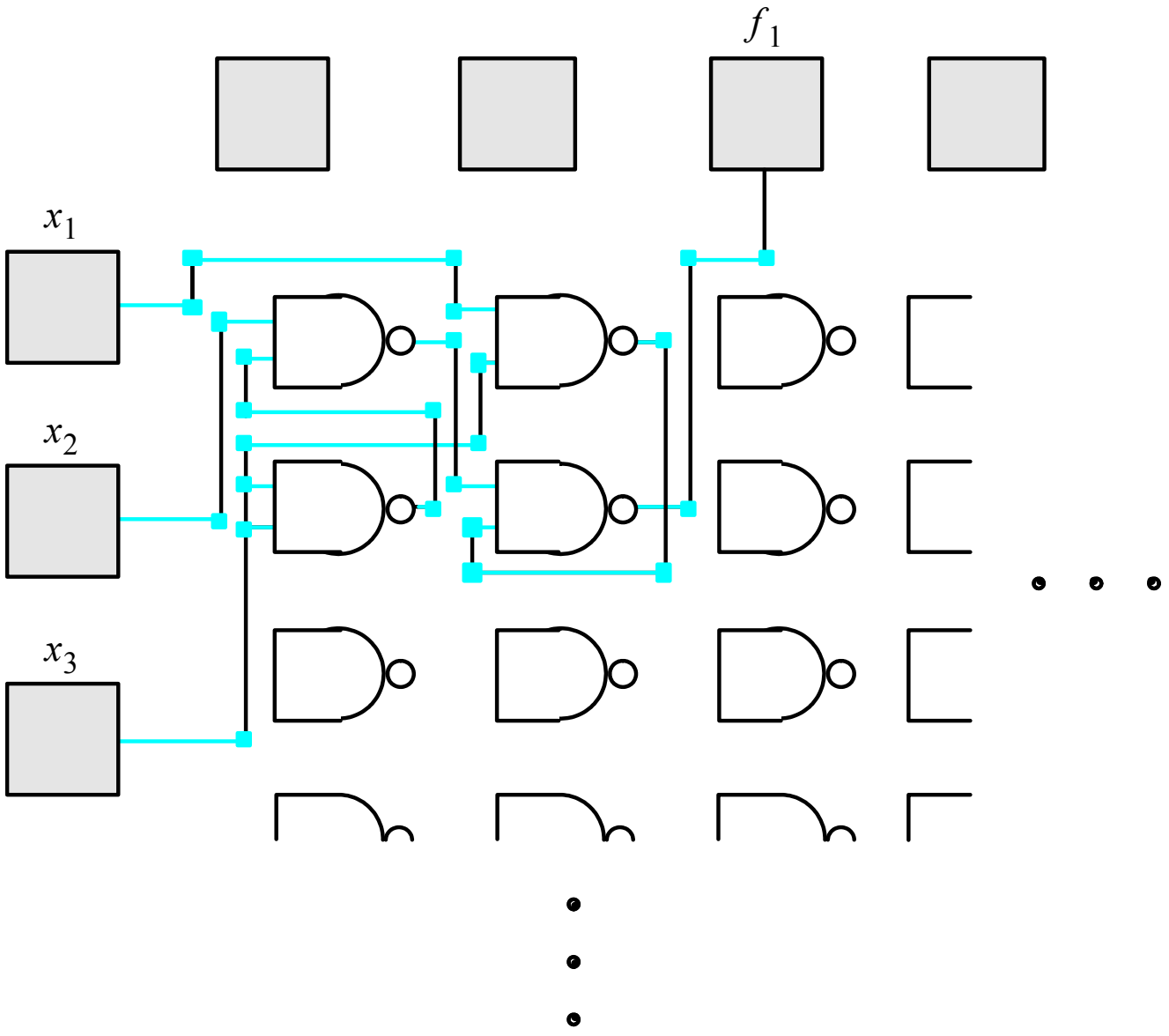
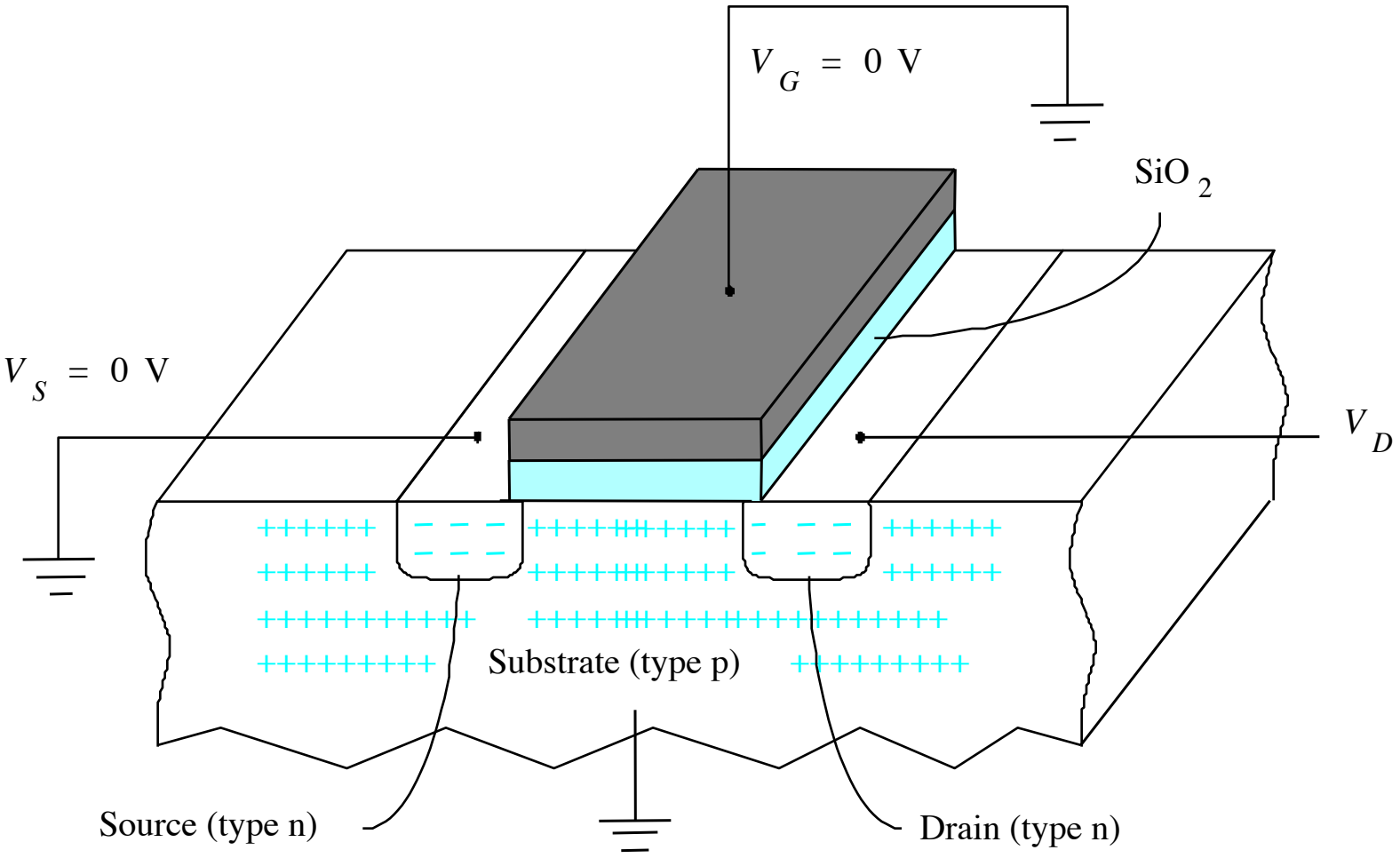
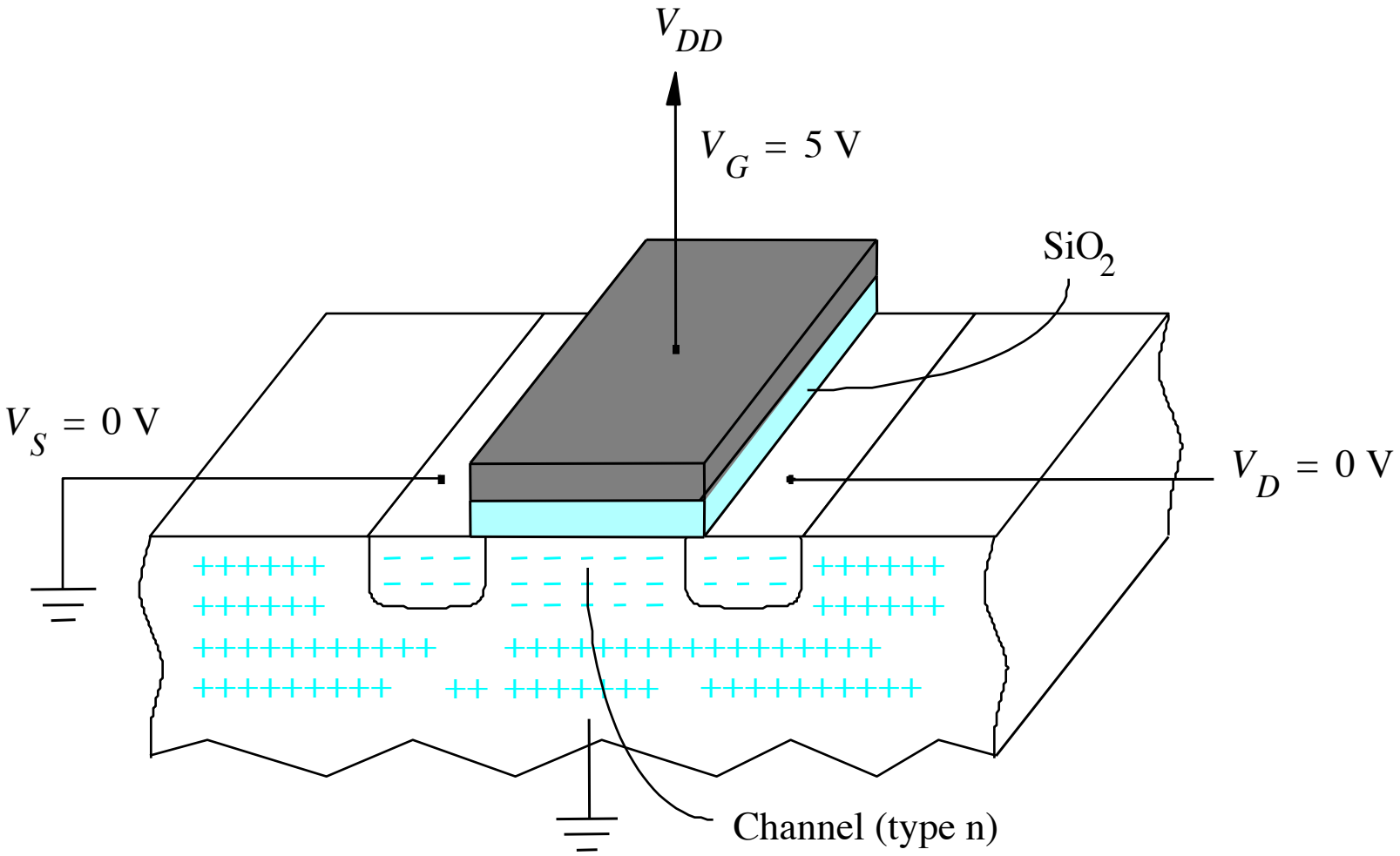


Figure B.42. The logic function $f_1 = x_2\bar{x}_3 + x_1x_3$ in the gate array of Figure B.41.



(a) When V_{GS} = 0 V, the transistor is off

Figure B.43*a*. NMOS transistor when turned off.



(b) When $V_{GS} = 5$ V, the transistor is on

Figure B.43*b*. NMOS transistor when turned on.

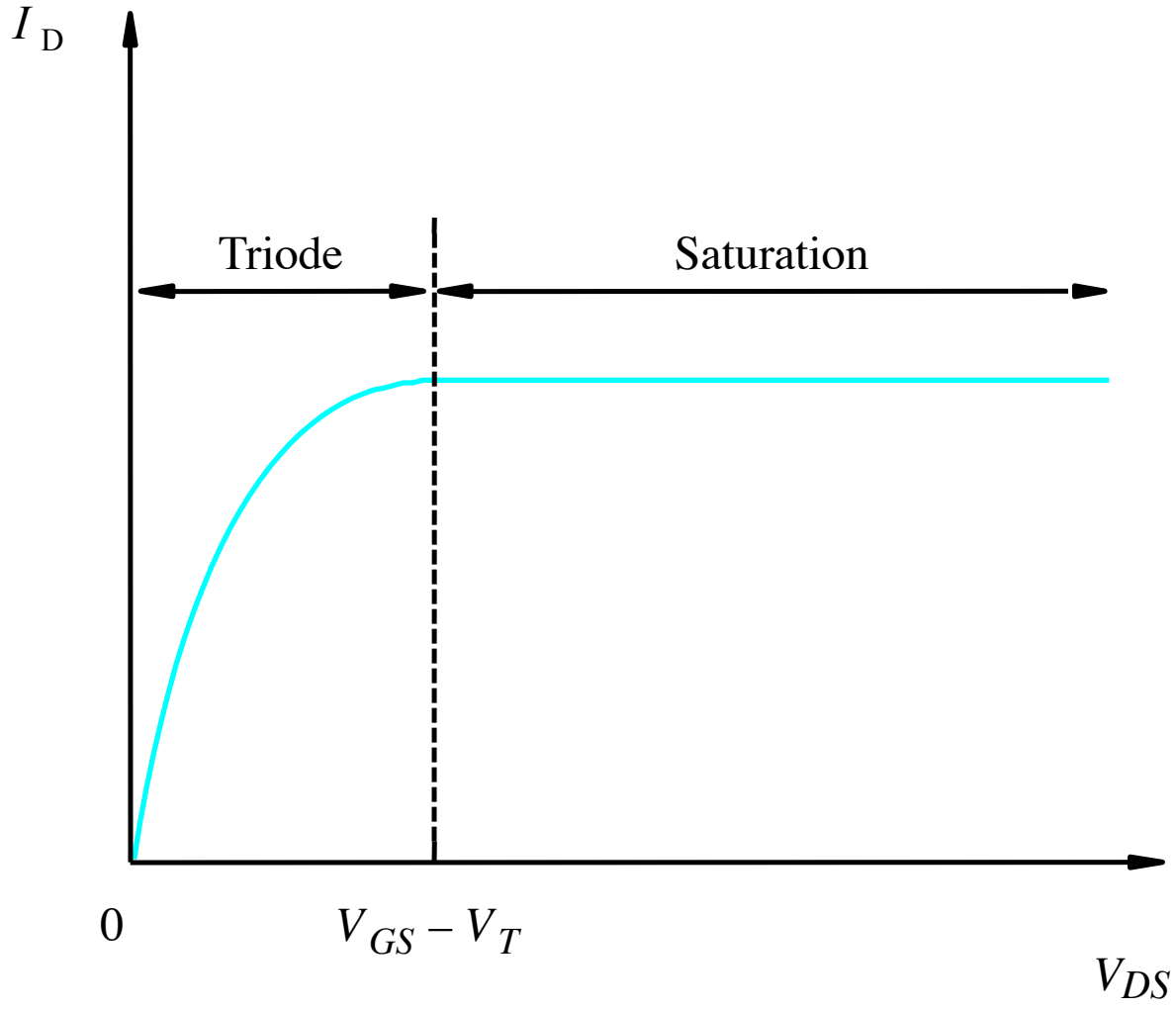


Figure B.44. The current-voltage relationship in the NMOS transistor.

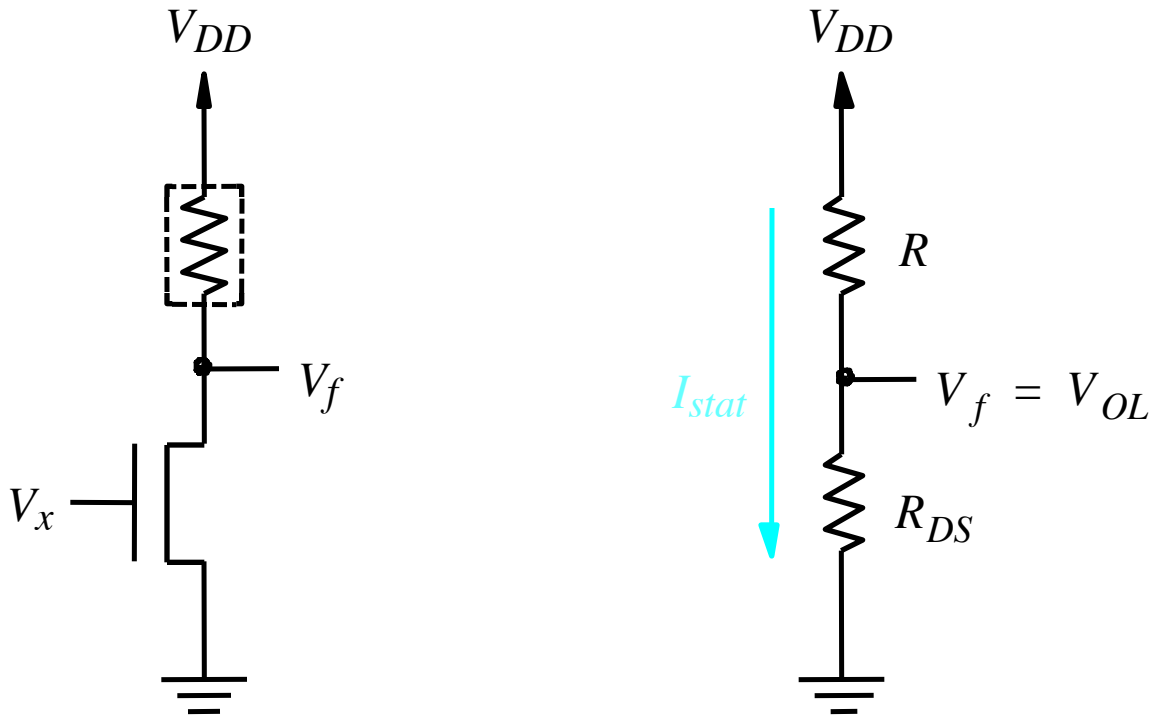


Figure B.45. Voltage levels in the NMOS inverter.

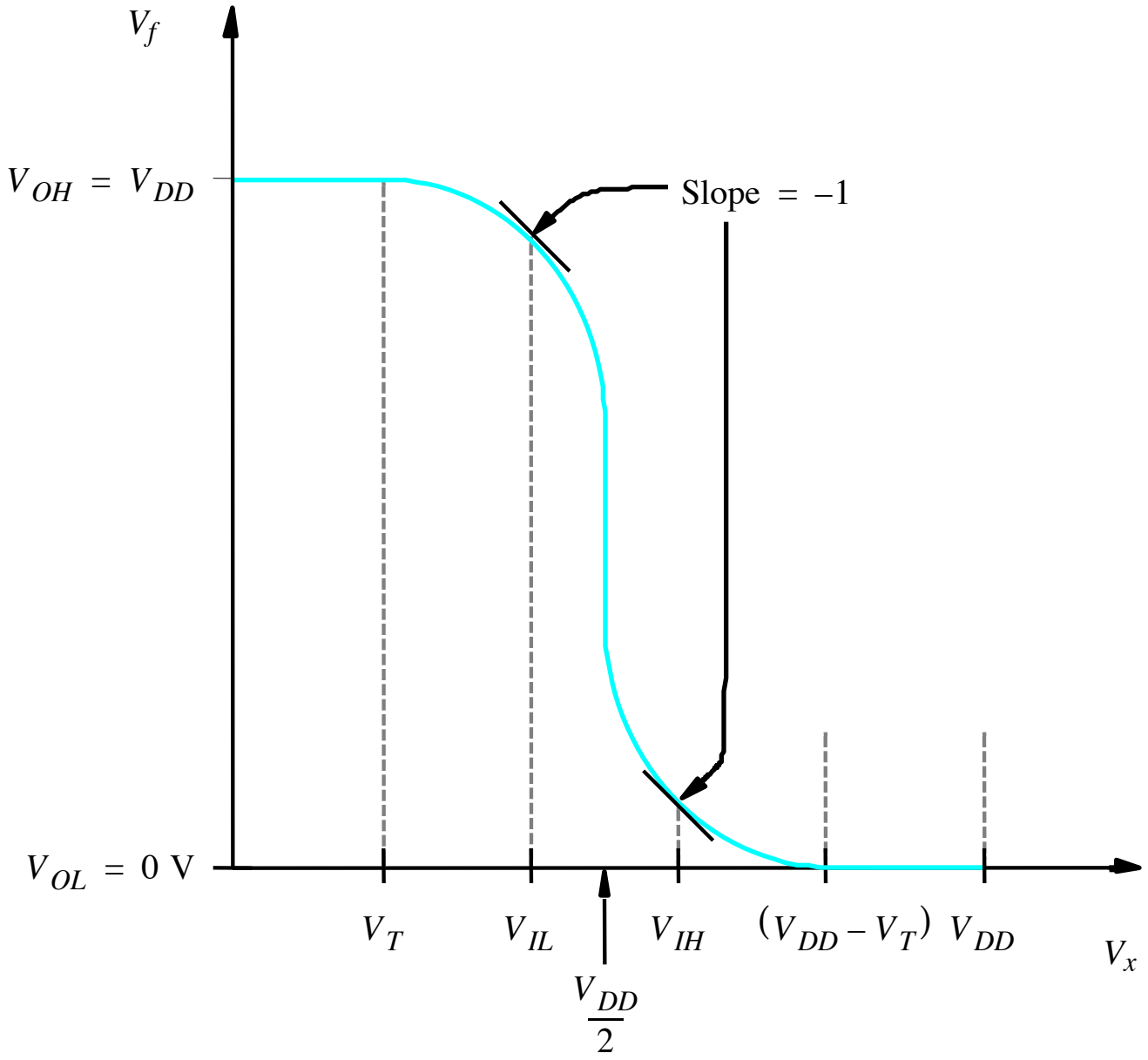
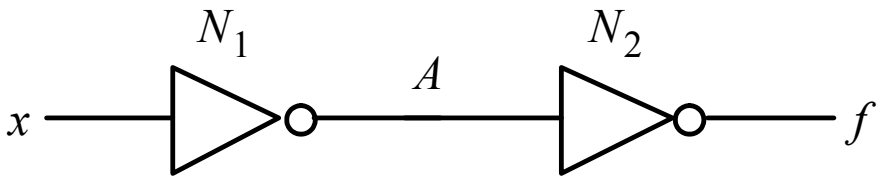
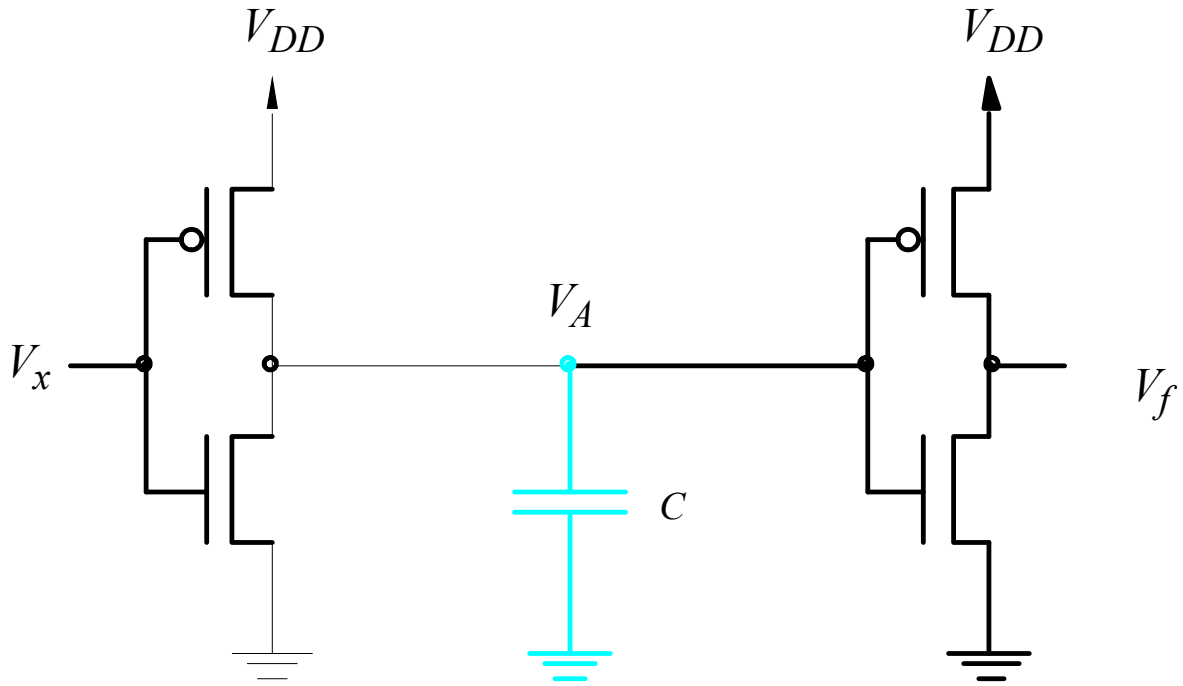


Figure B.46. The voltage transfer characteristic for the CMOS inverter.



(a) A NOT gate driving another NOT gate



(b) The capacitive load at node A

Figure B.47. Parasitic capacitance in integrated circuits.

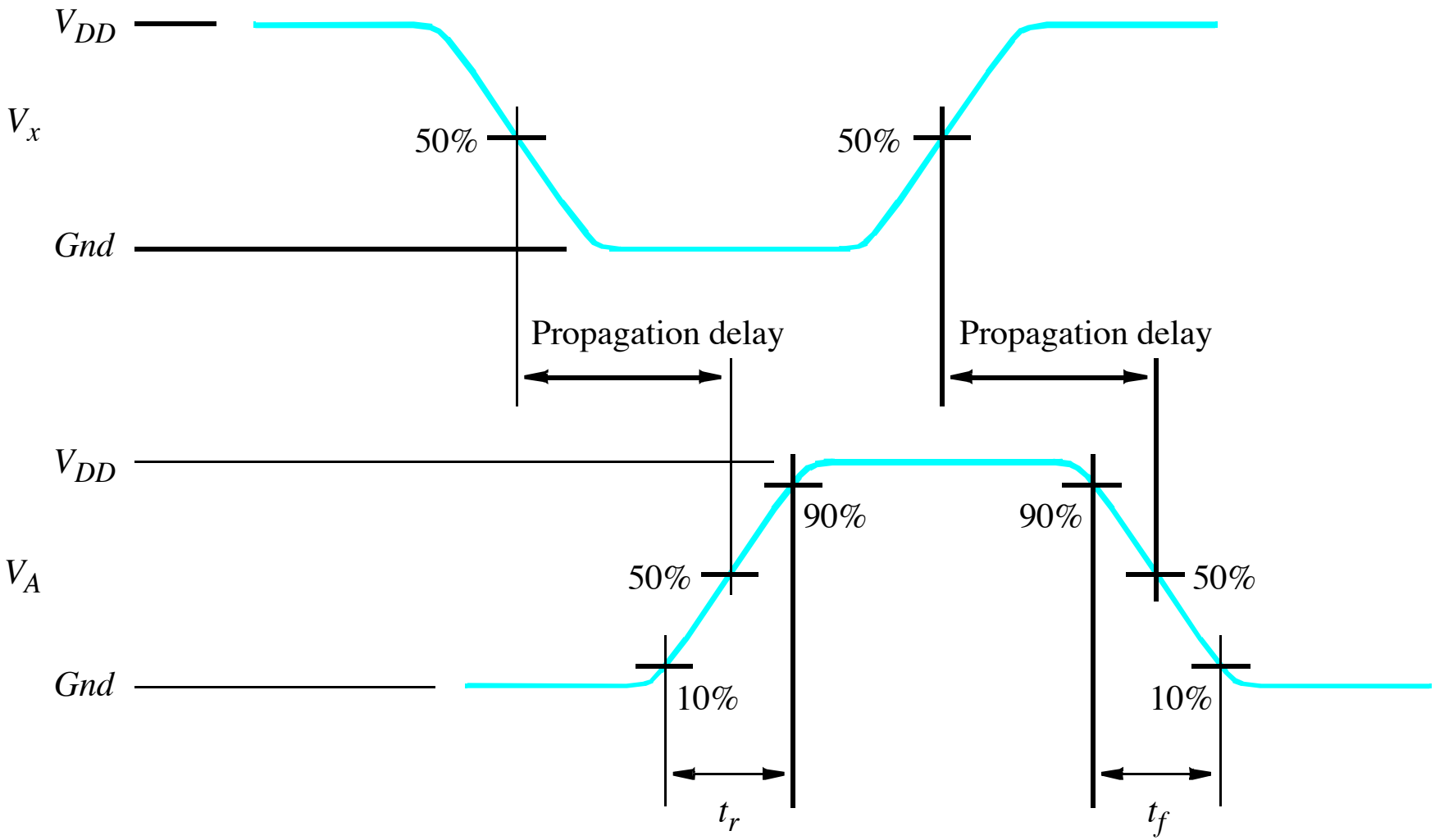
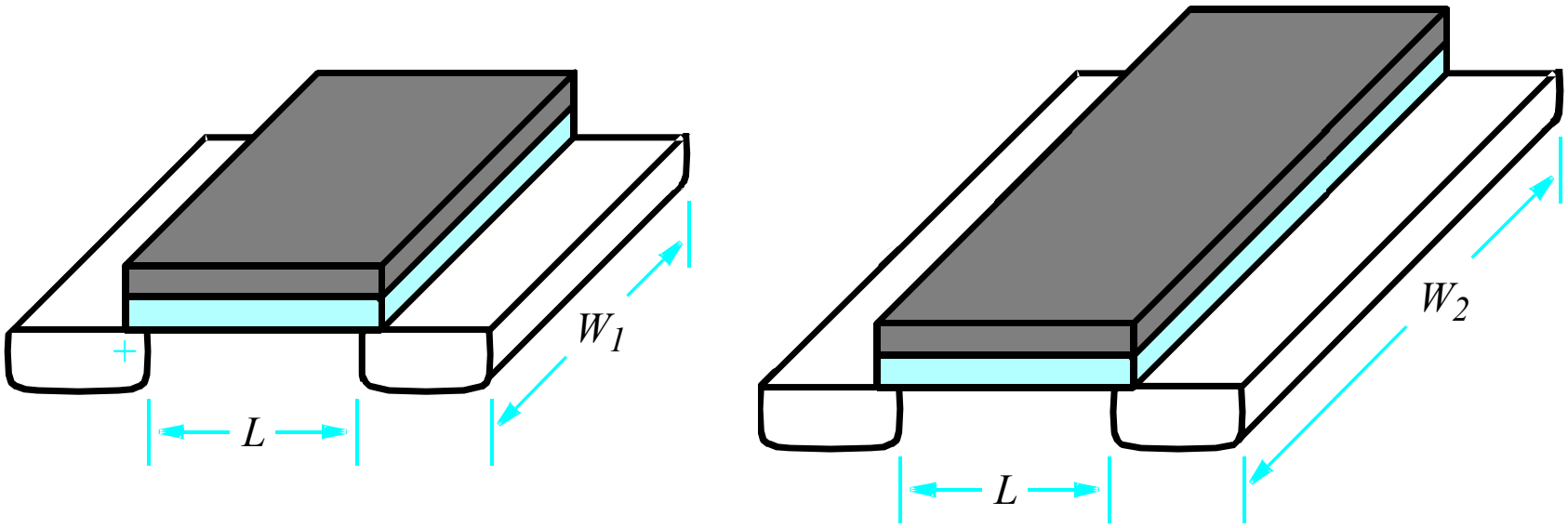


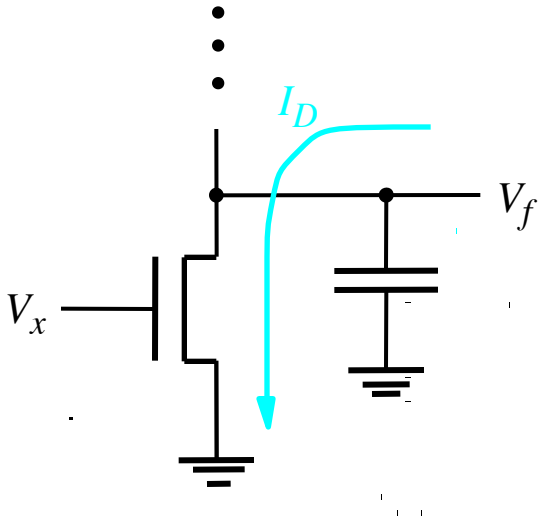
Figure B.48. Voltage waveforms for logic gates.



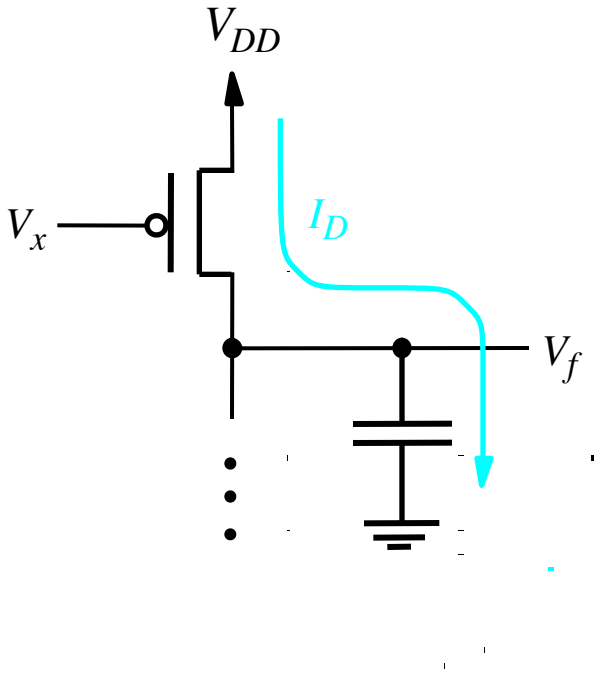
(a) Small transistor

(b) Larger transistor

Figure B.49. Transistor sizes.



(a) Current flow when input V_x changes from 0 V to 5 V



(b) Current flow when input V_x changes from 5 V to 0 V

Figure B.50. Dynamic current flow in CMOS circuits.

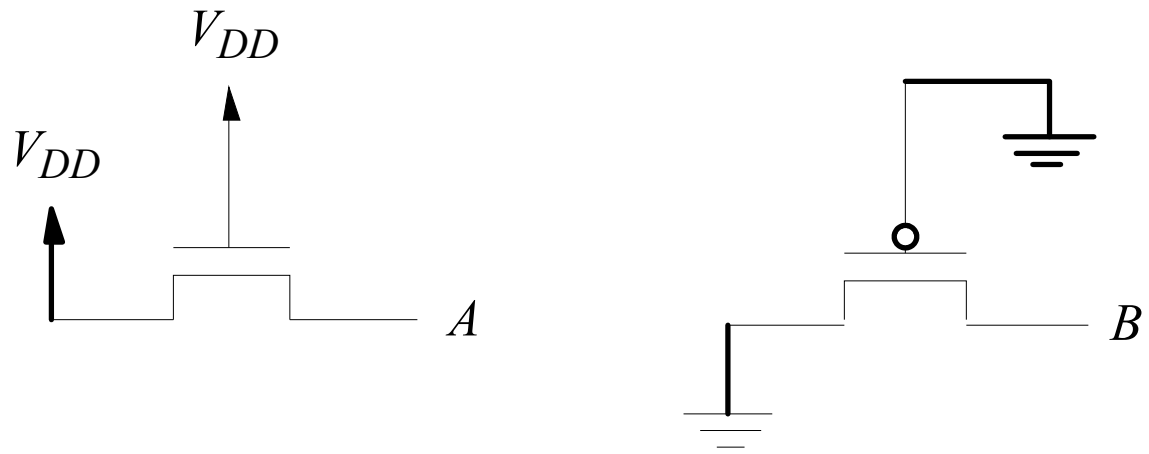
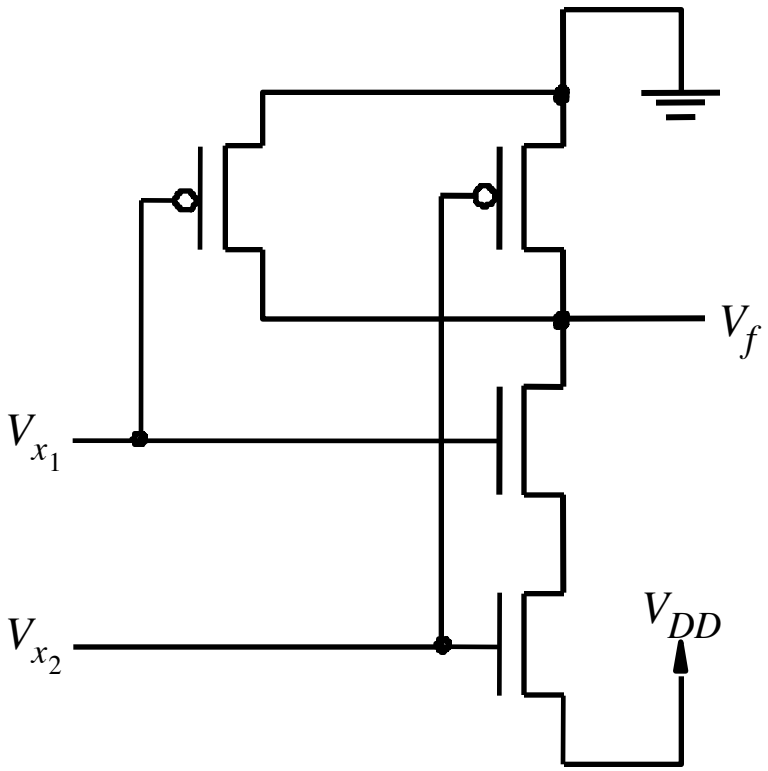


Figure B.51. NMOS and PMOS transistors used in the opposite way from Figure B.4.



(a) An AND gate circuit

Logic value		Voltage	Logic value
x_1	x_2	V_f	f
0	0	1.5 V	0
0	1	1.5 V	0
1	0	1.5 V	0
1	1	3.5 V	1

(b) Truth table and voltage levels

Figure B.52. A Poor implementation of a CMOS AND gate.

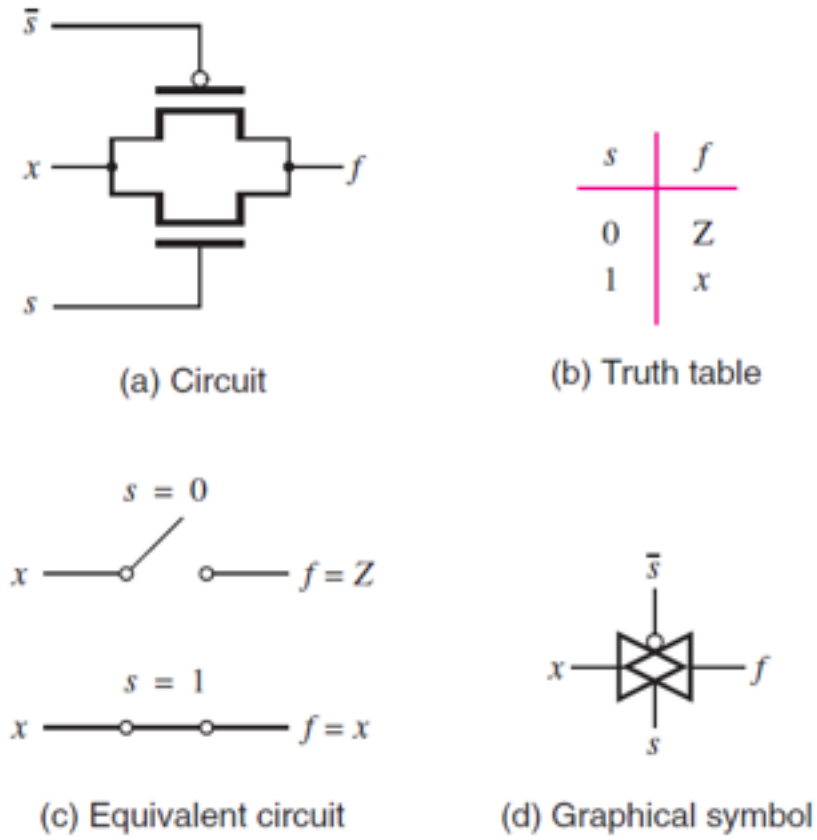


Figure B.53. A transmission gate.

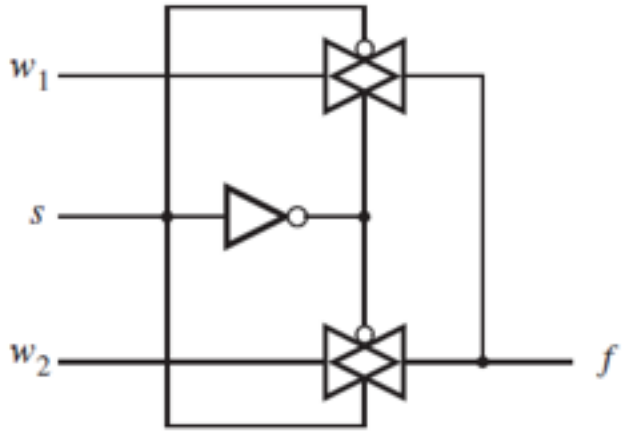


Figure B.54. A 2-to-1 multiplexer built using transmission gates.

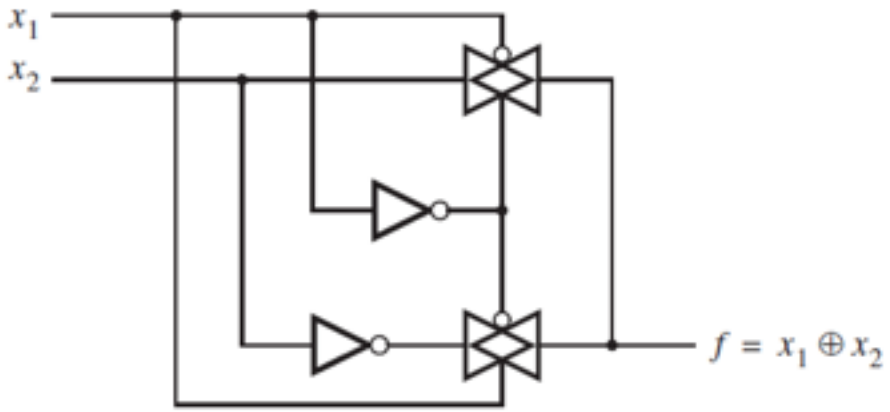


Figure B.55. Implementation of an XOR gate.

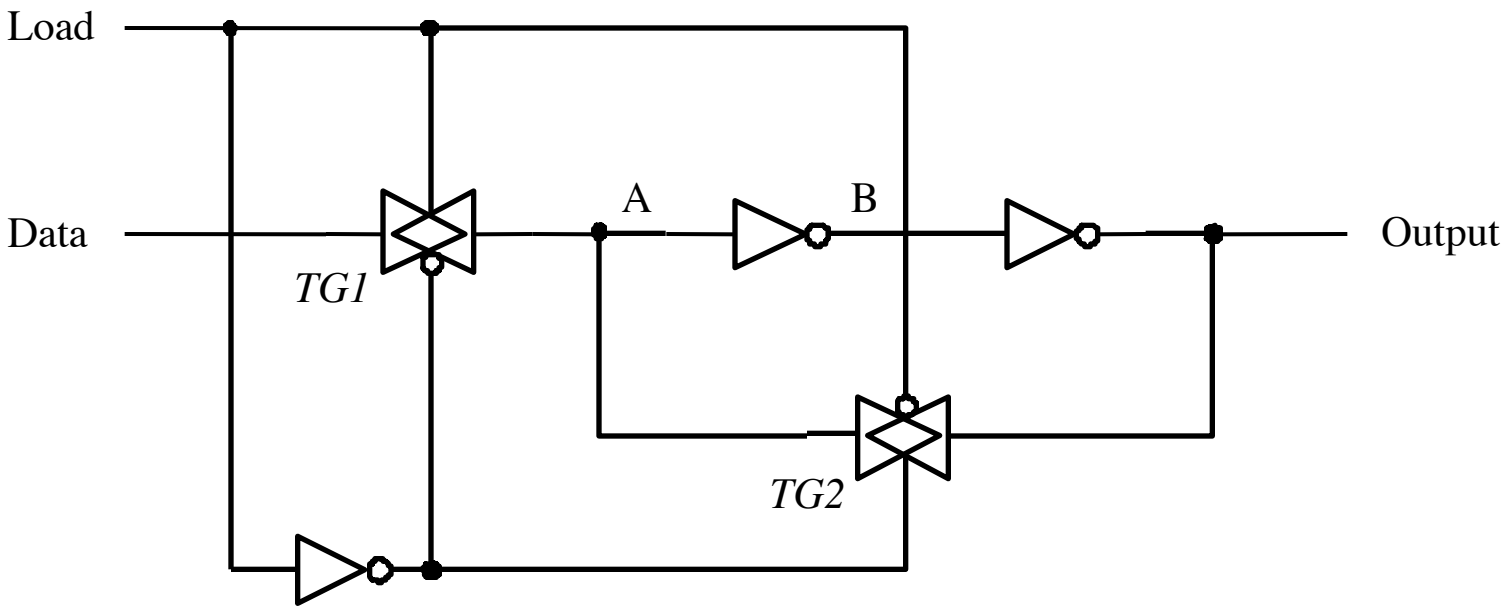


Figure B.56. Using transmission gates to implement a gated D latch.

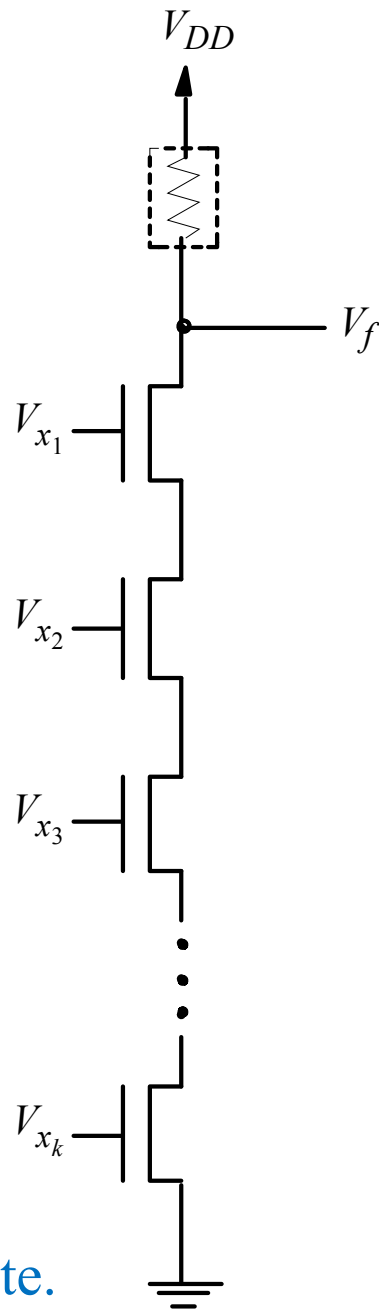


Figure B.57. High fan-in NMOS NAND gate.

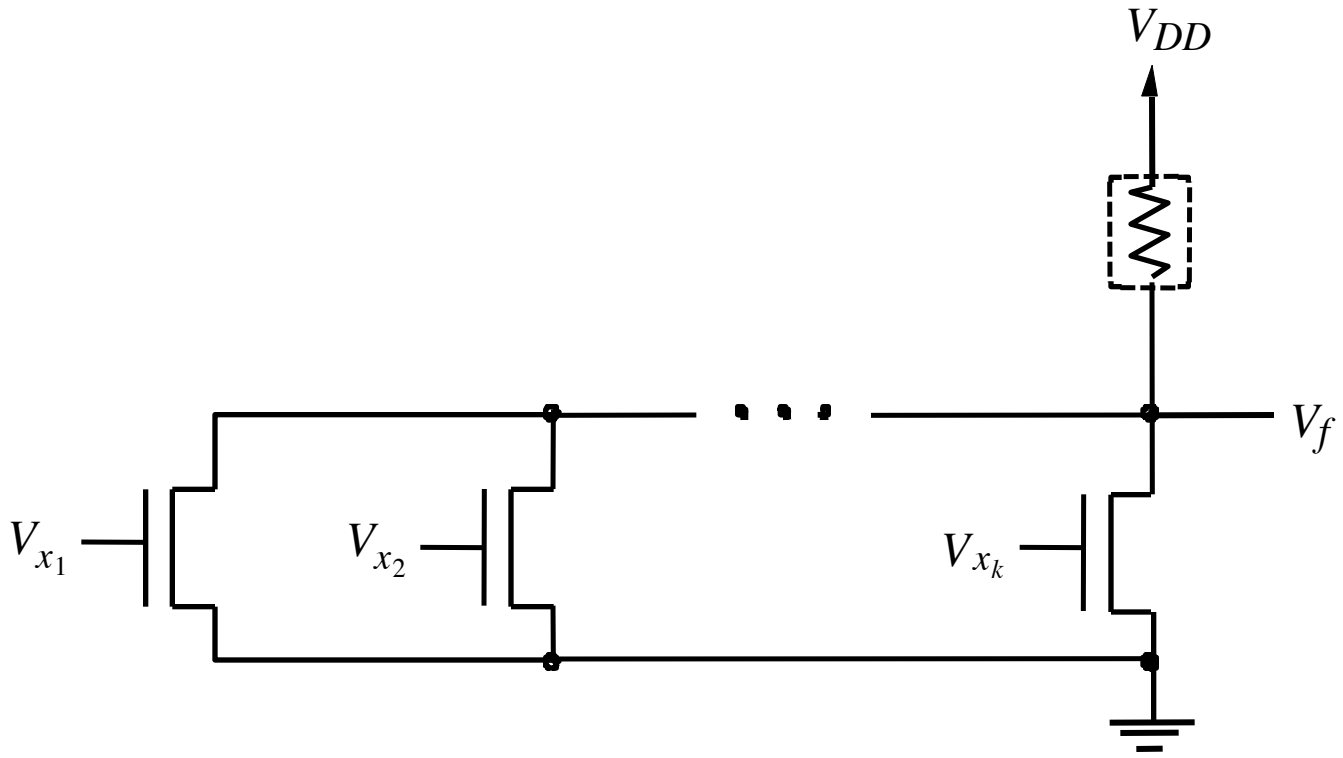
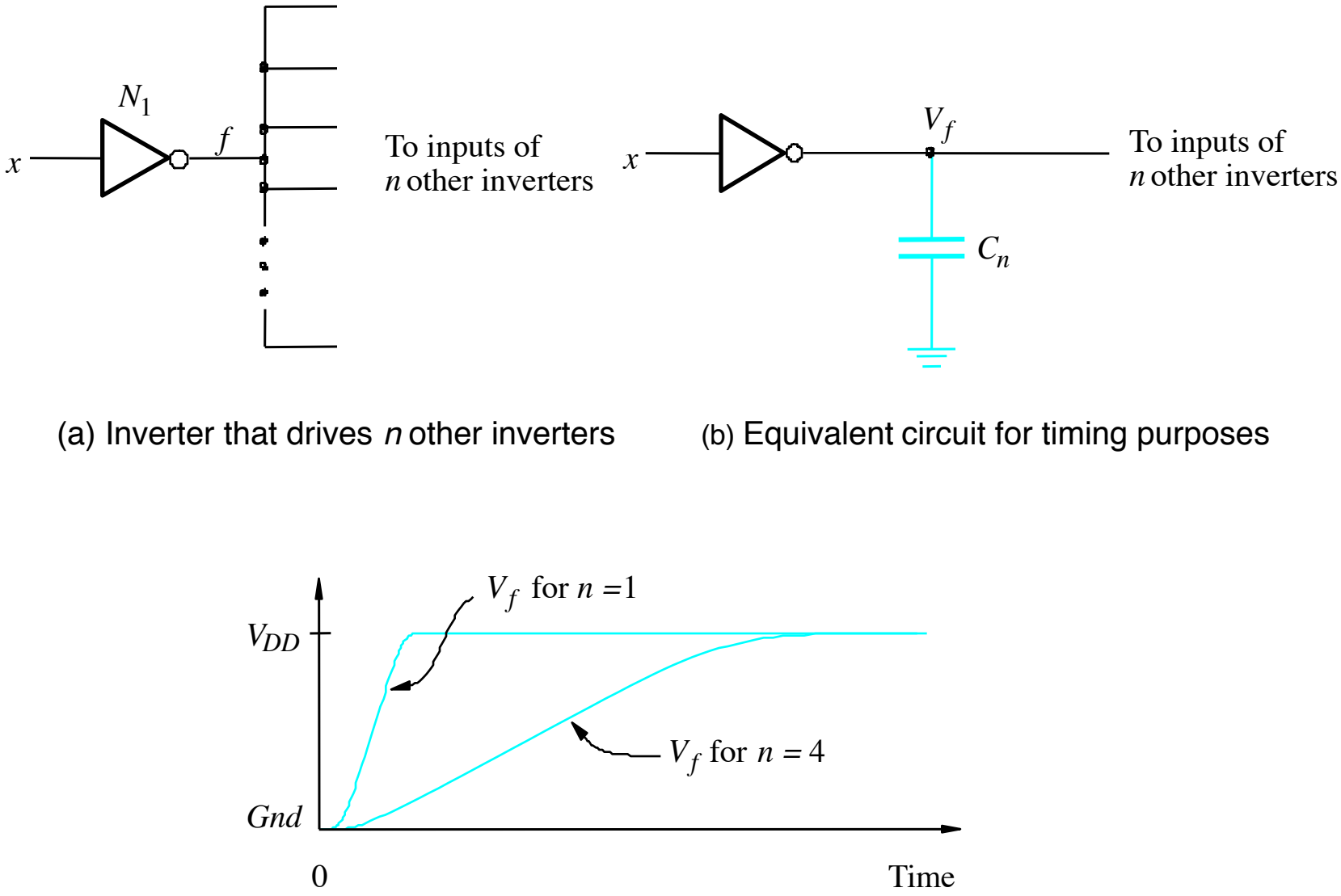


Figure B.58. High fan-in NMOS NOR gate.

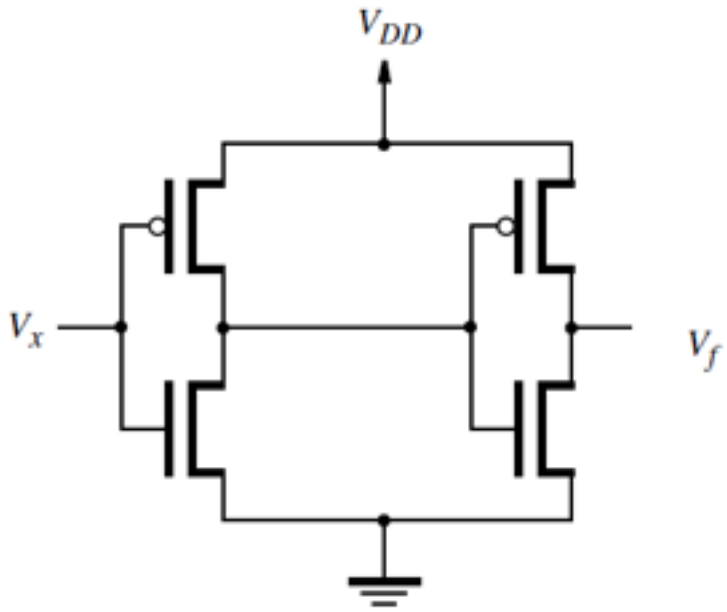


(a) Inverter that drives n other inverters

(b) Equivalent circuit for timing purposes

(c) Propagation times for different values of n

Figure B.59. The effect of fan-out on propagation delay.



(a) Implementation of a driver

(b) Graphical symbol

Figure B.60. A noninverting buffer.

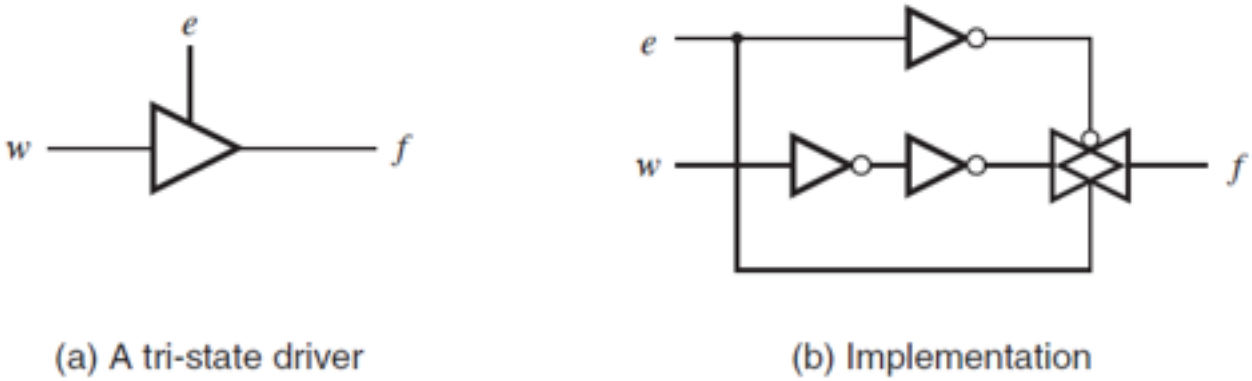


Figure B.61. Tri-state driver.

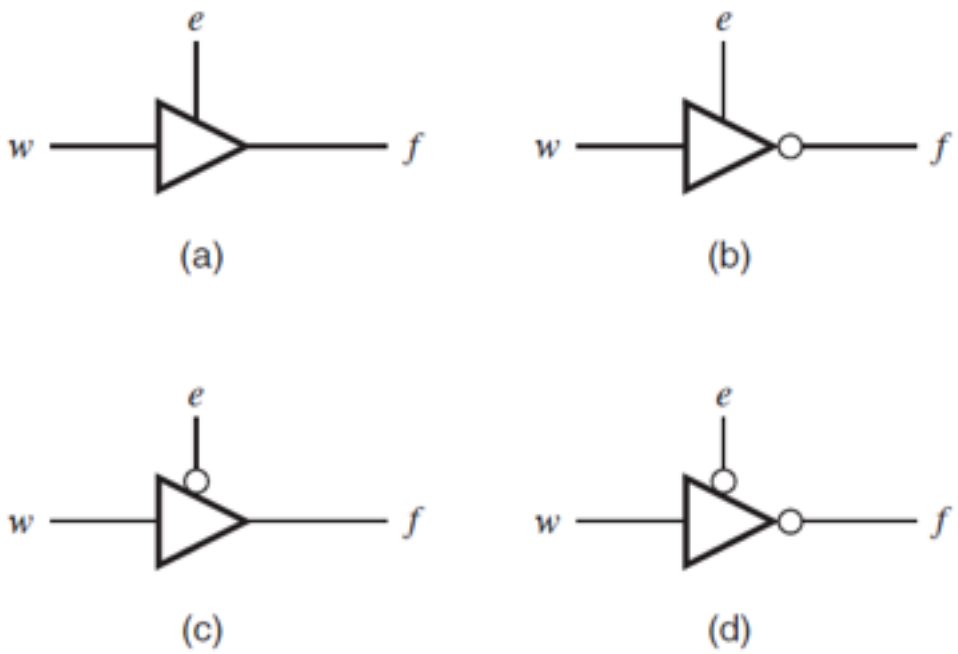


Figure B.62. Tri-state driver.

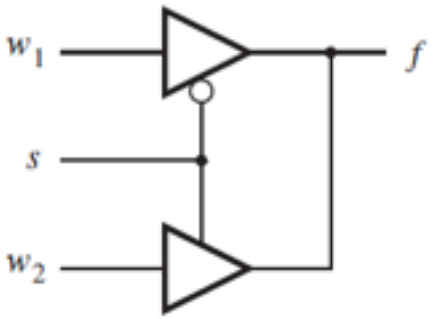


Figure B.63. An application of tri-state drivers.

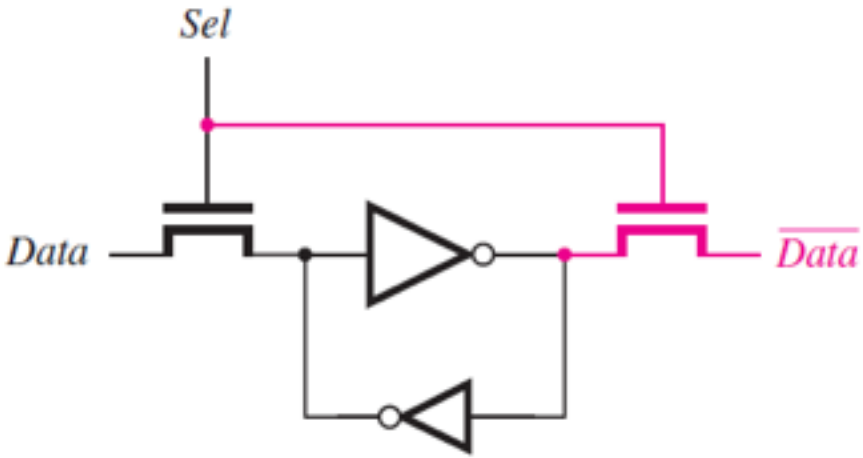


Figure B.64. An SRAM cell.

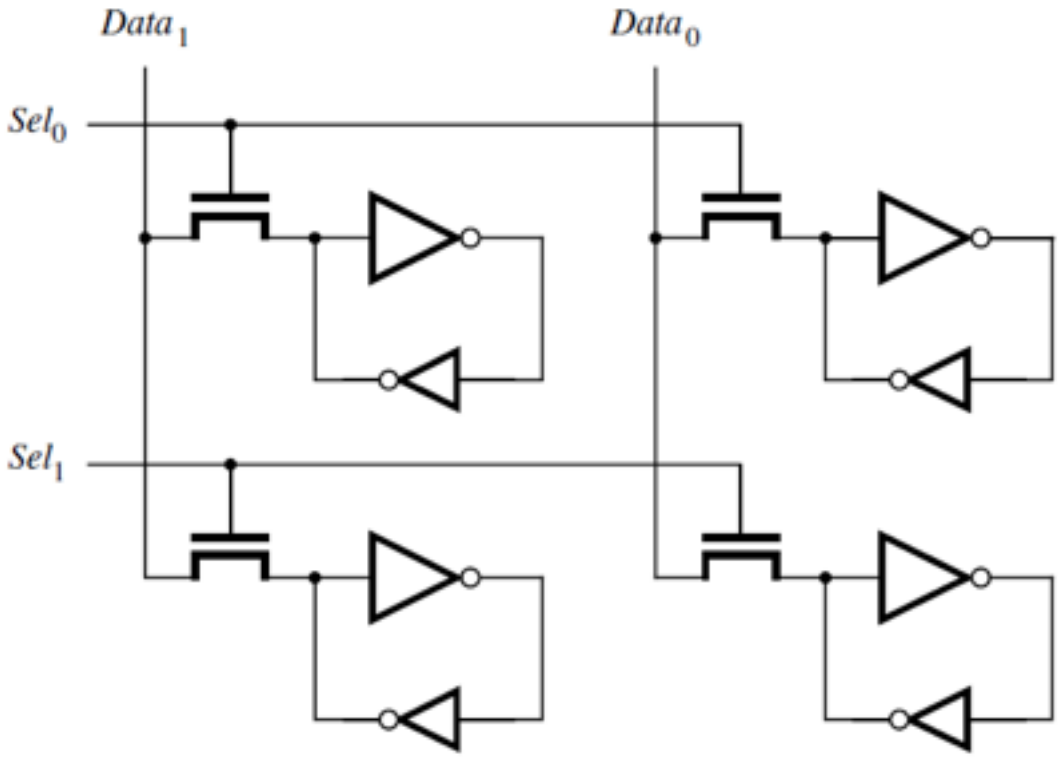


Figure B.65. A 2 x 2 array of SRAM cells.

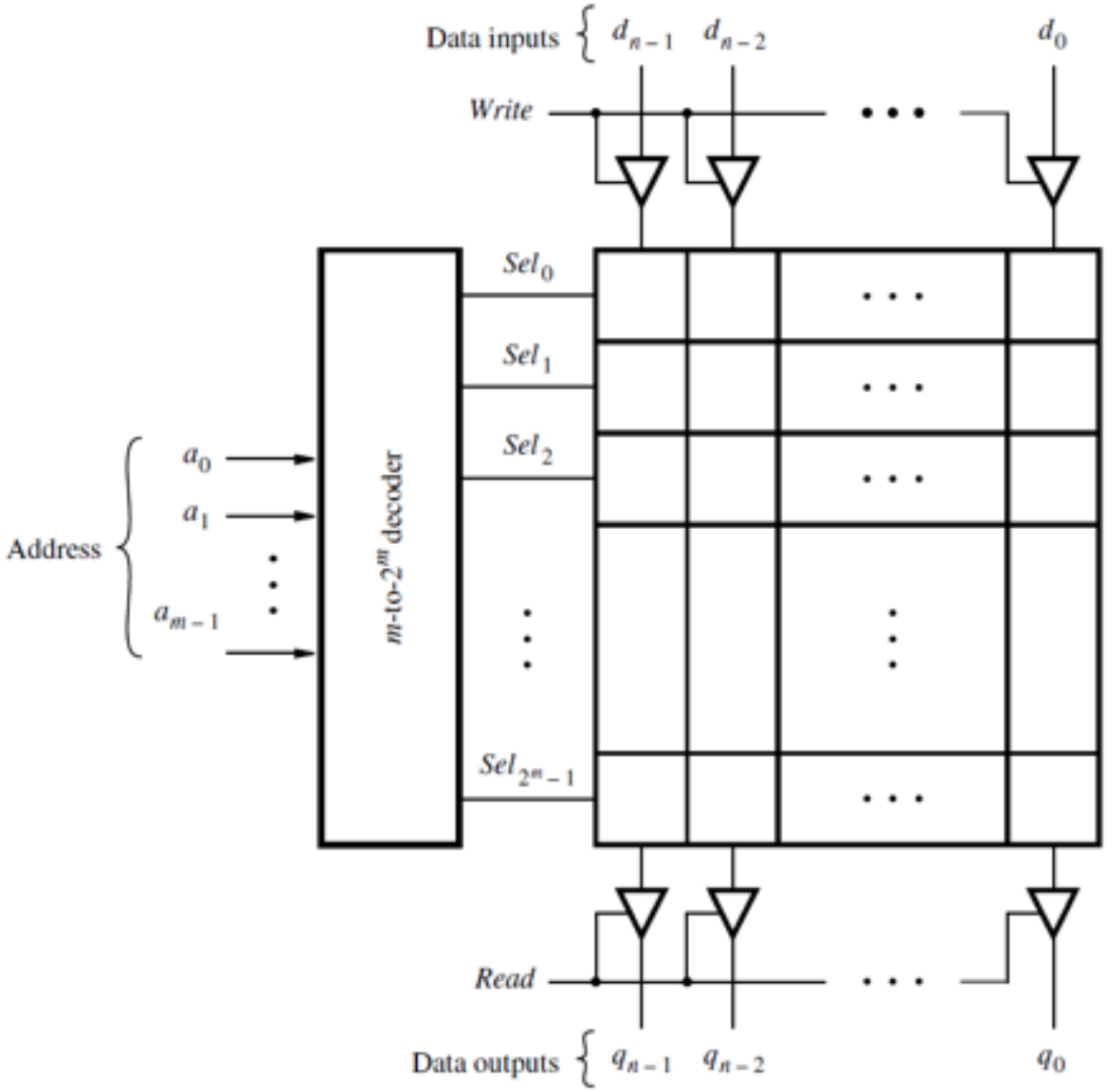


Figure B.66. A 2^m x n SRAM block.

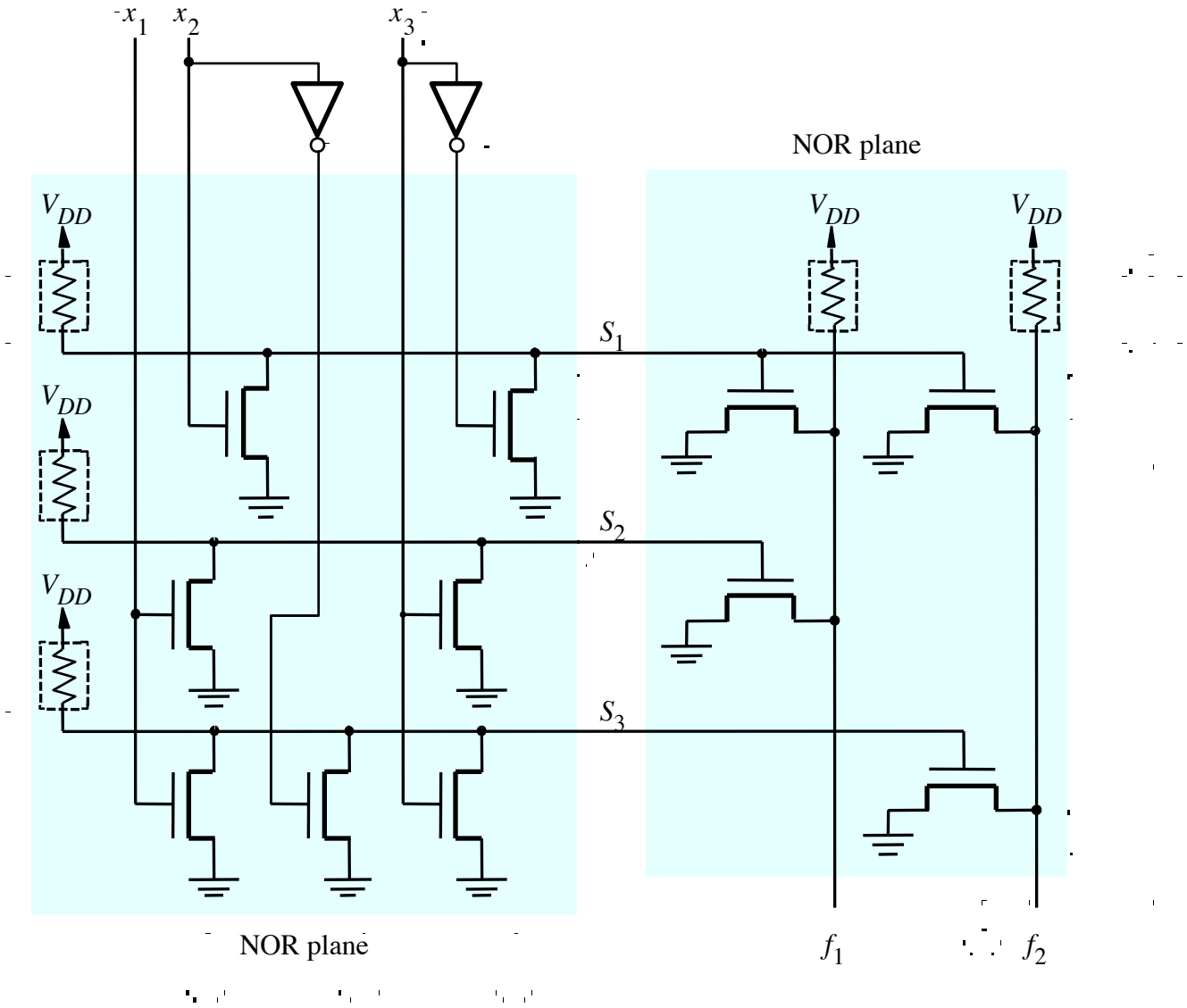


Figure B.67. An example of a NOR-NOR PLA.

Please see “portrait orientation” PowerPoint file for Chapter B

Figure B.68. Using EEPROM transistors to create a programmable NOR plane.

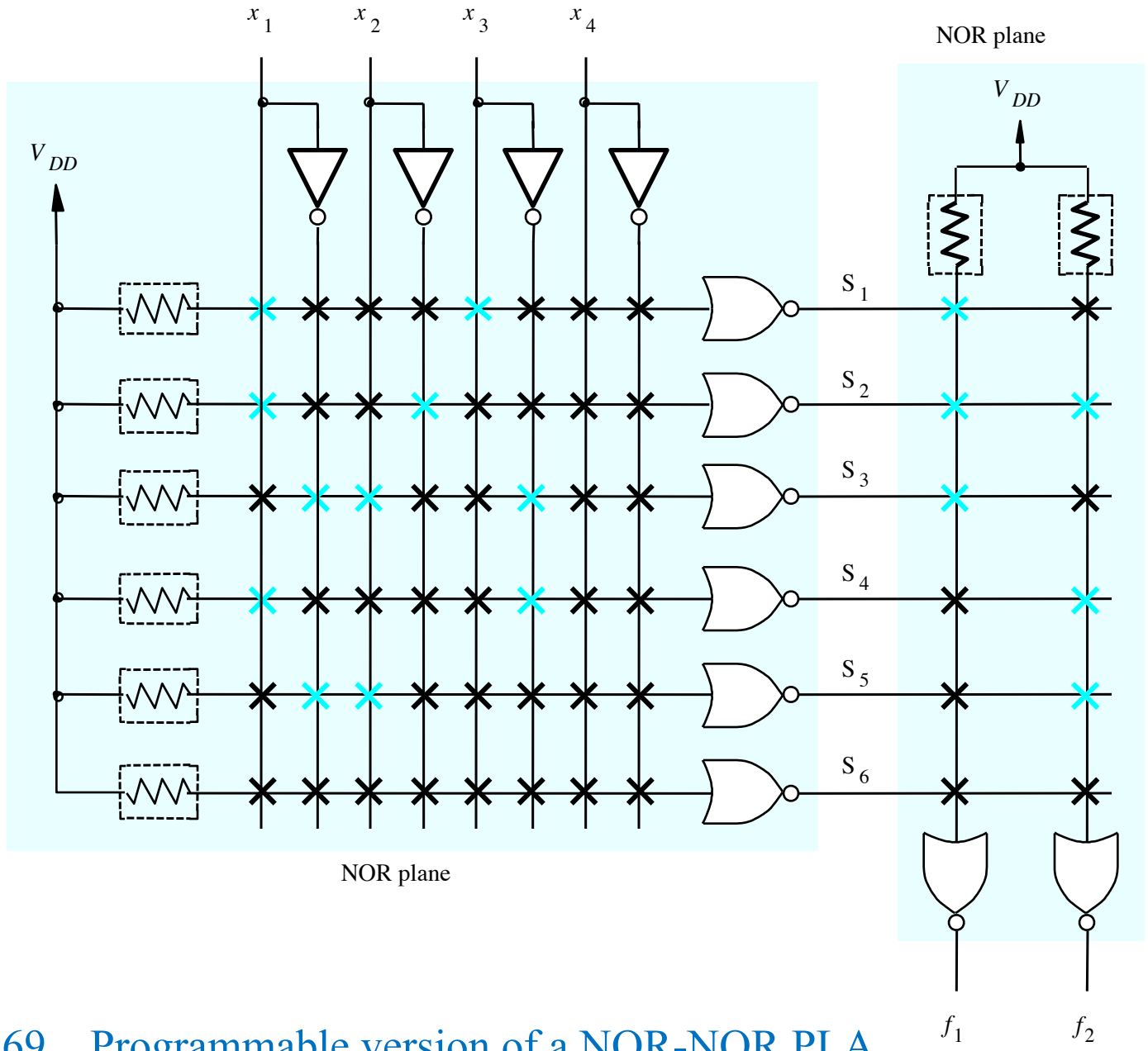


Figure B.69. Programmable version of a NOR-NOR PLA.

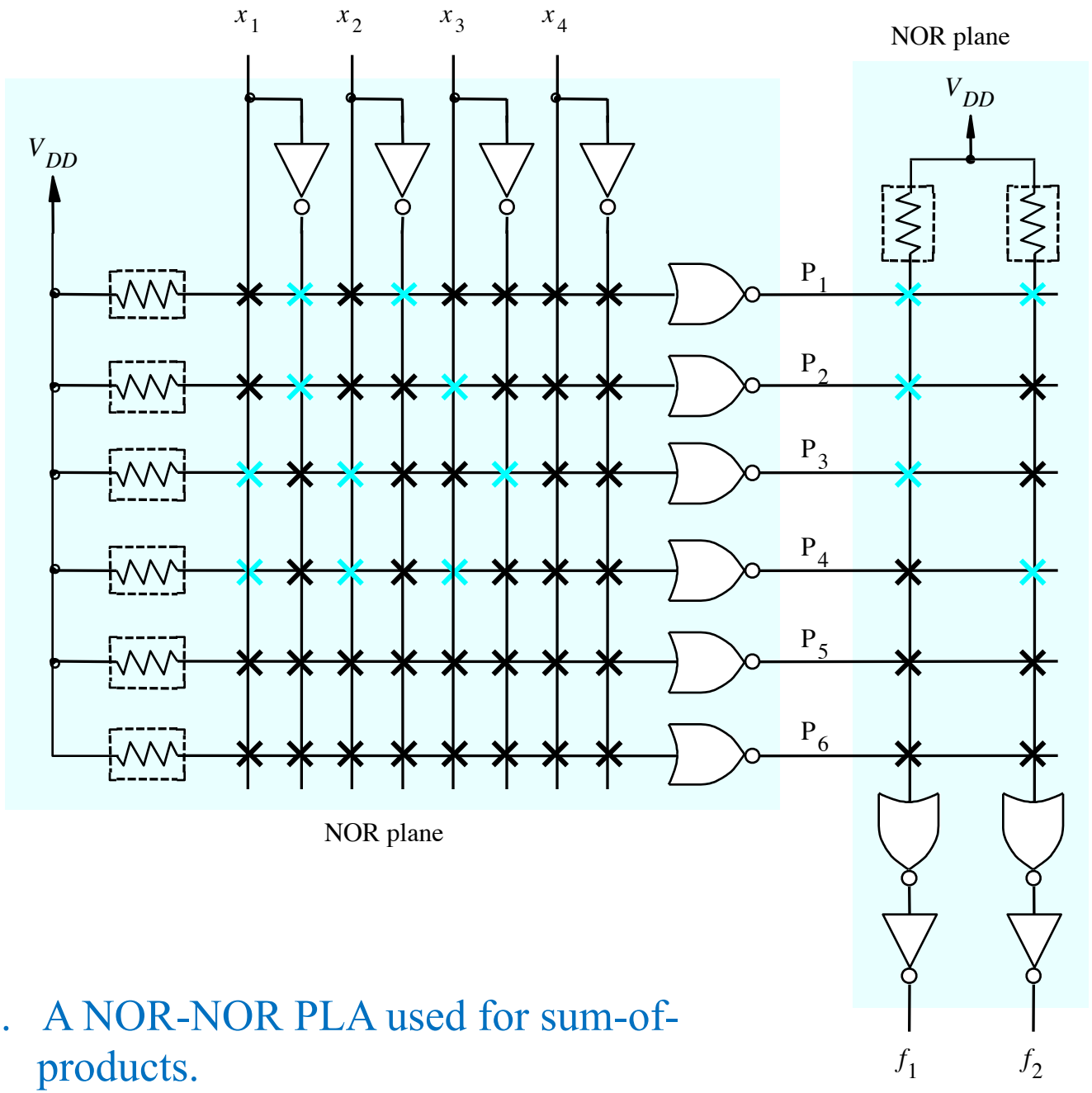


Figure B.70. A NOR-NOR PLA used for sum-of-products.

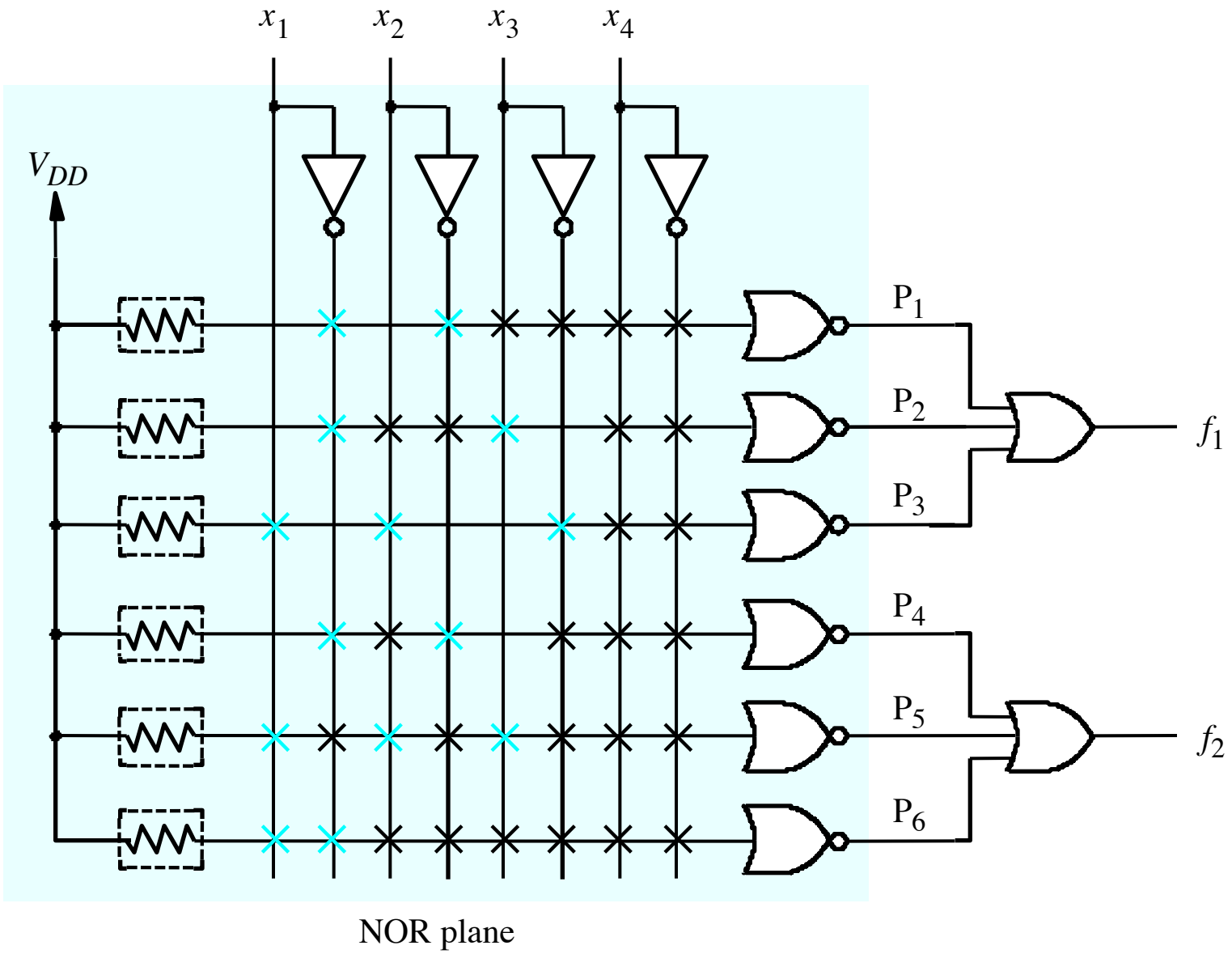


Figure B.71. PAL programmed to implement two functions in Figure B.70.

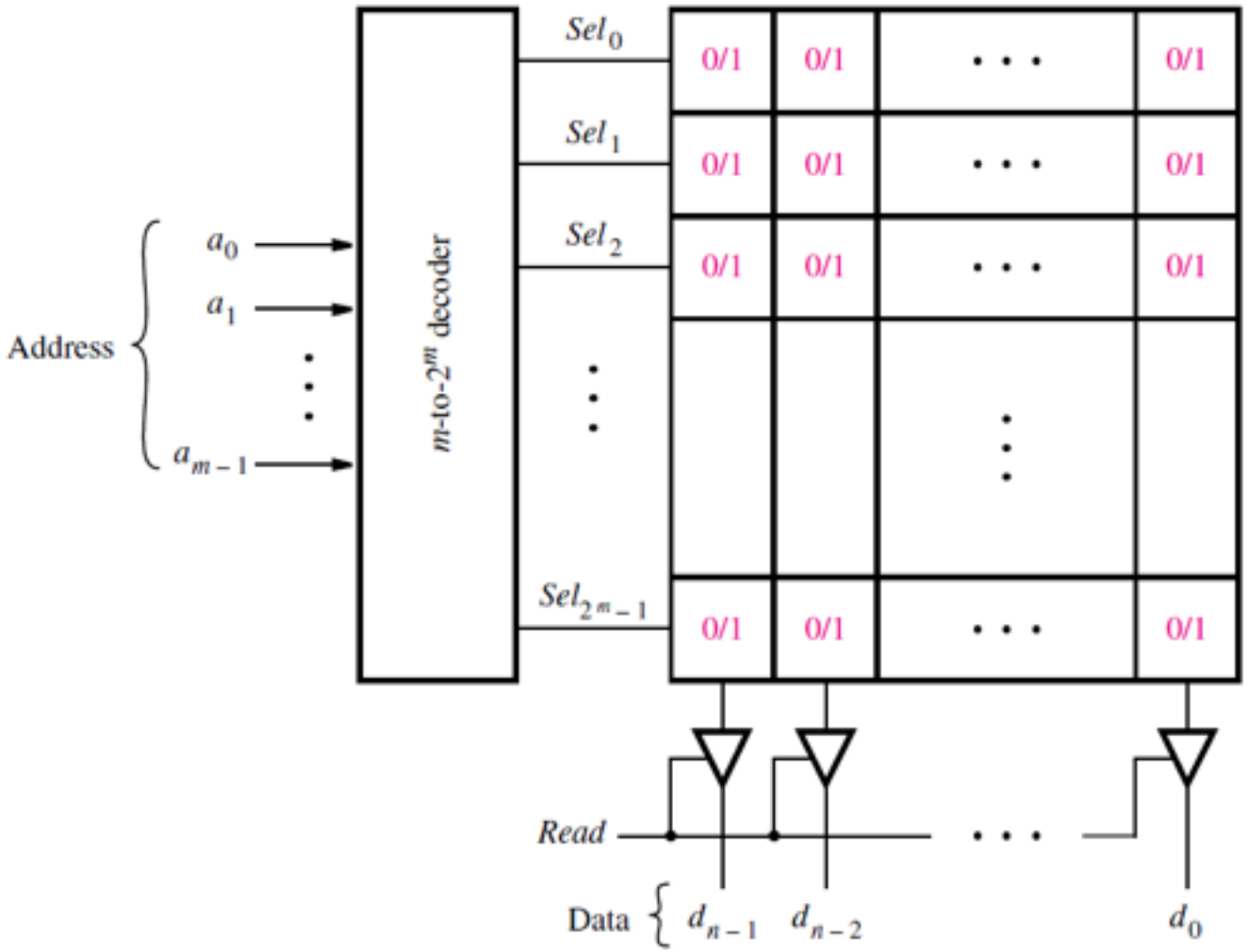


Figure B.72. A 2^m x n read-only memory (ROM) block.

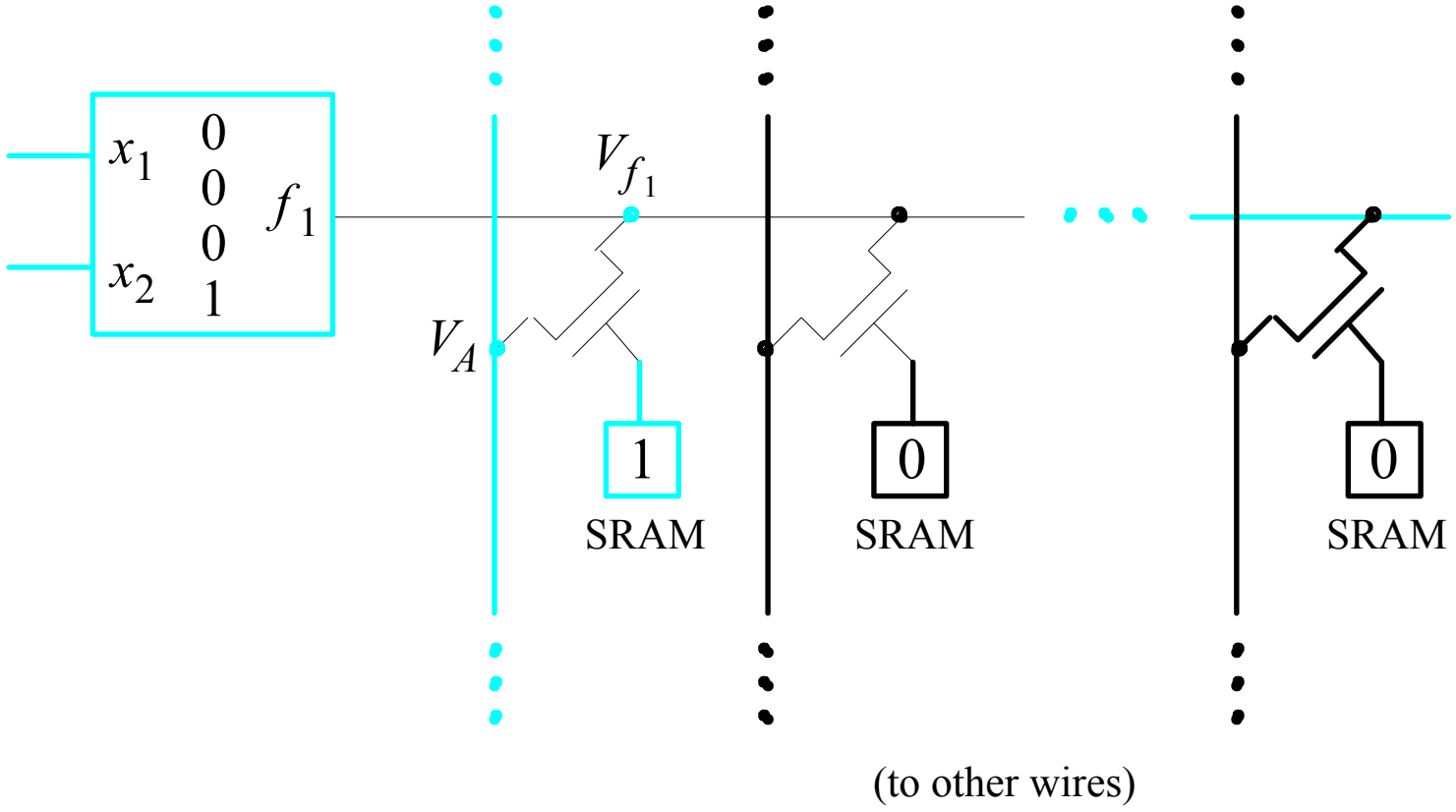


Figure B.73. Pass-transistor switches in FPGAs.

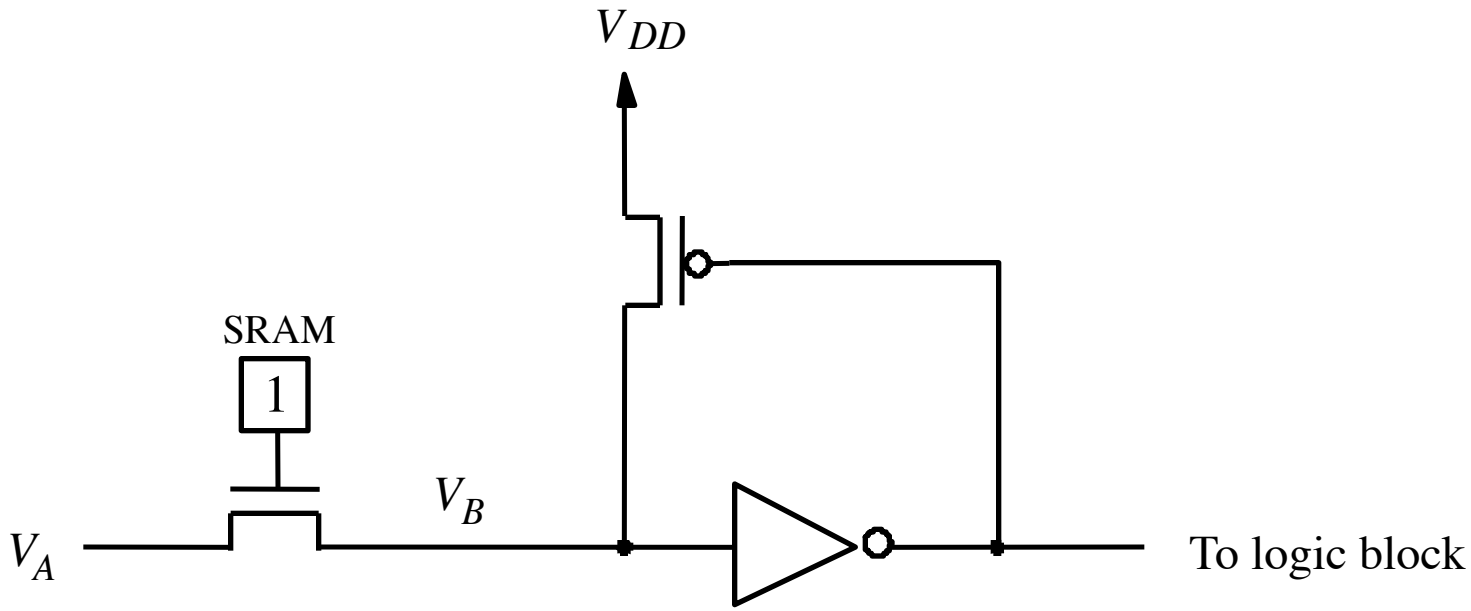


Figure B.74. Restoring a high voltage level.

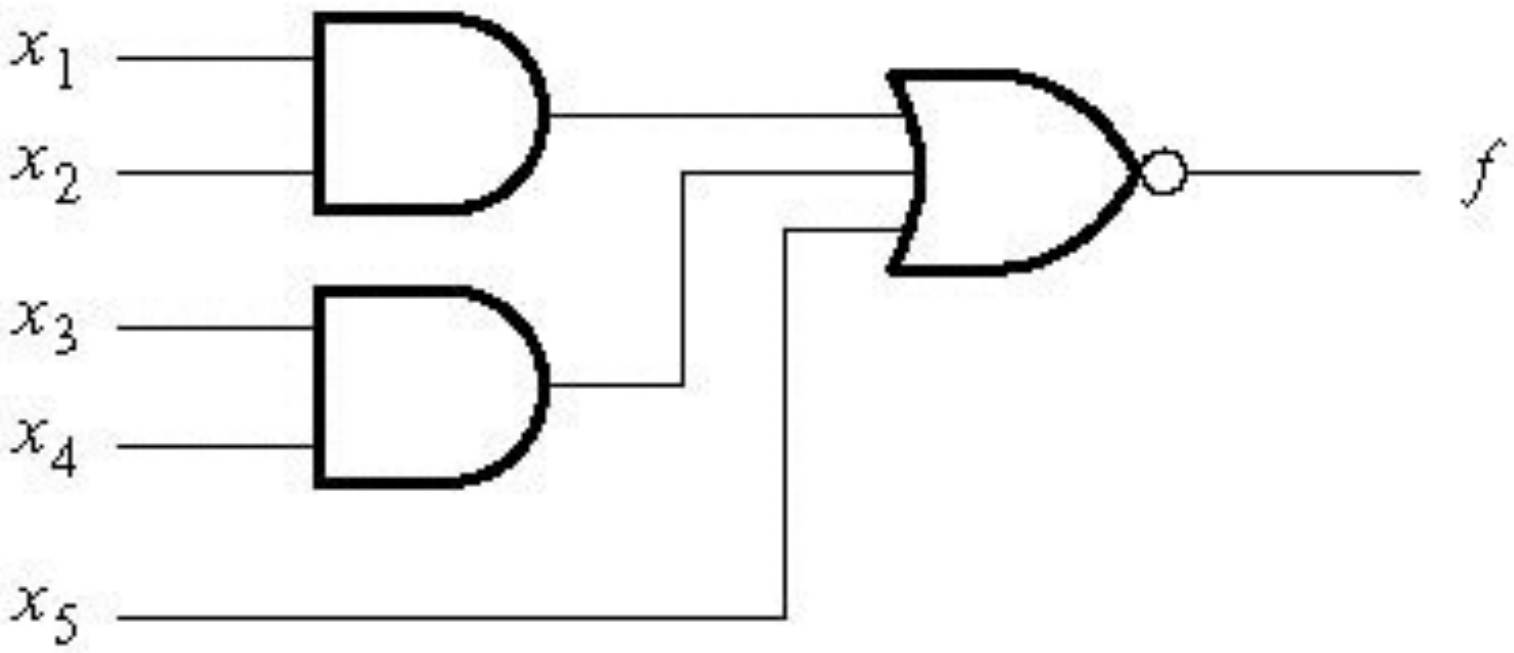


Figure B.75. The AOI cell for Example B.13.

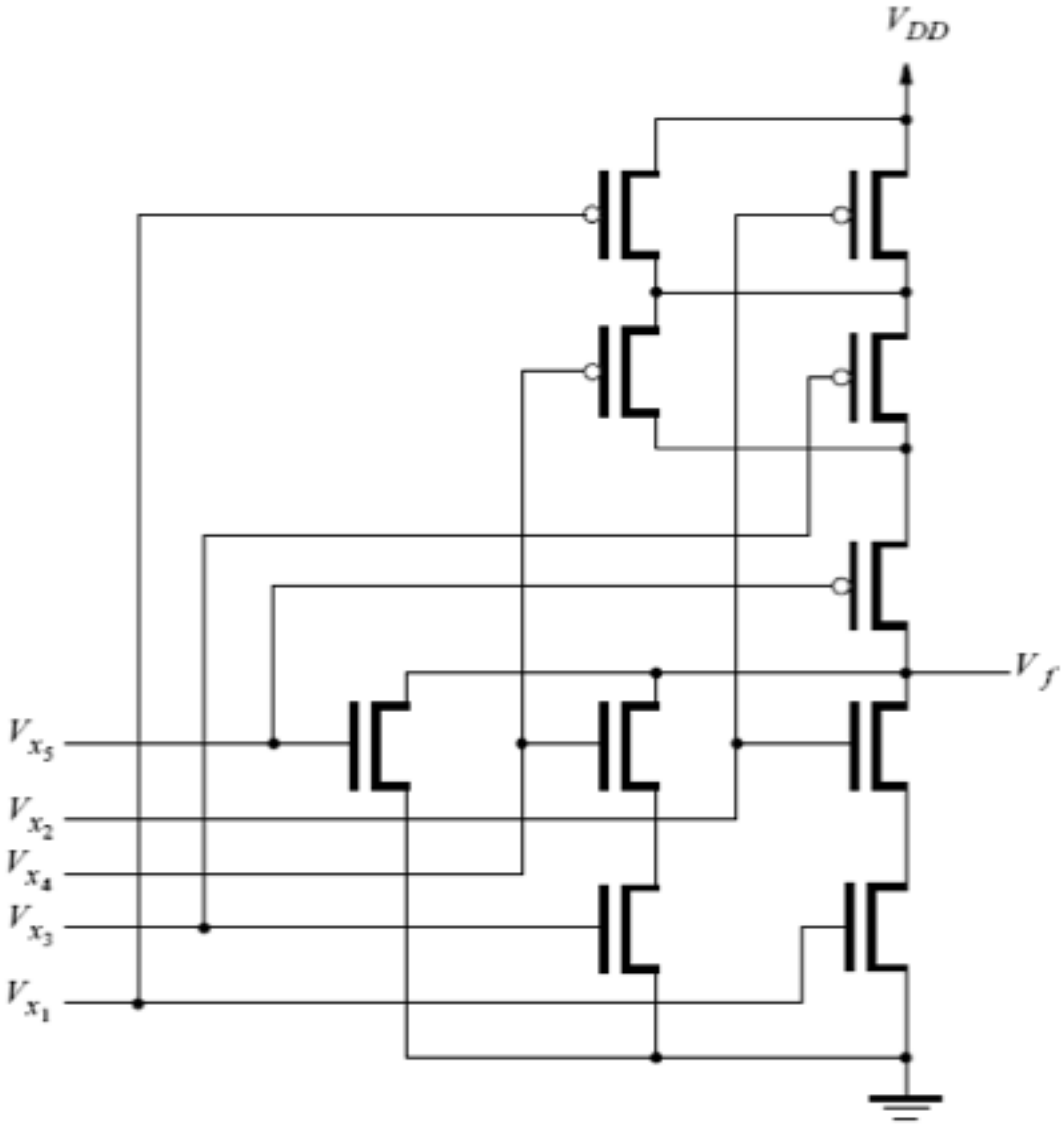


Figure B.76. Circuit for Examples B.13 and B.14.

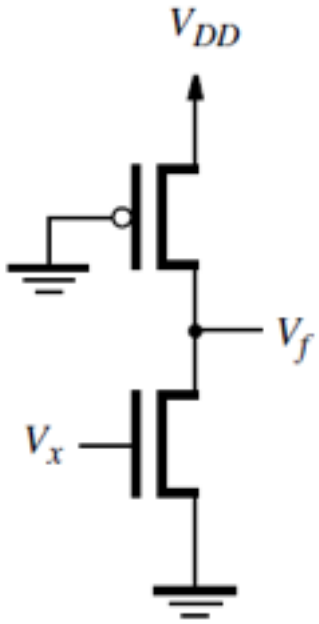


Figure B.77. The pseudo-NMOS inverter.

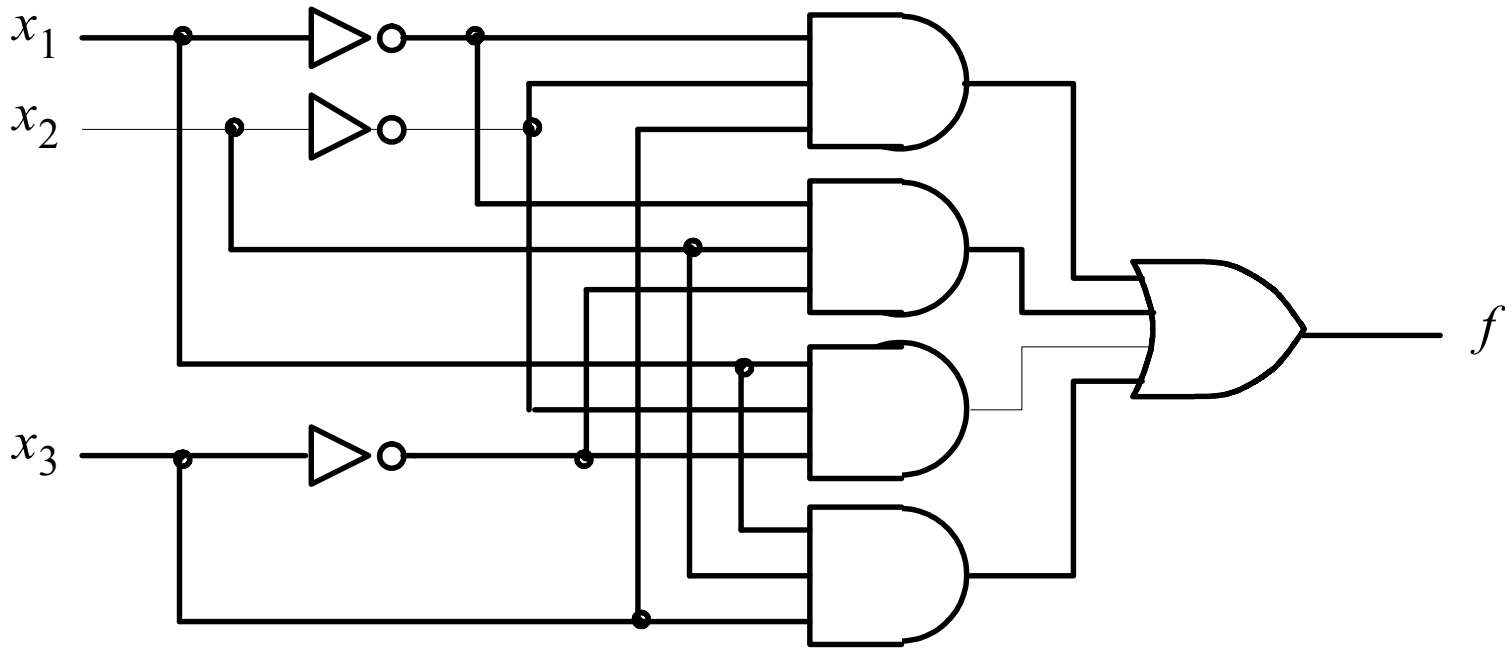


Figure PB.1. A sum-of-products CMOS circuit.

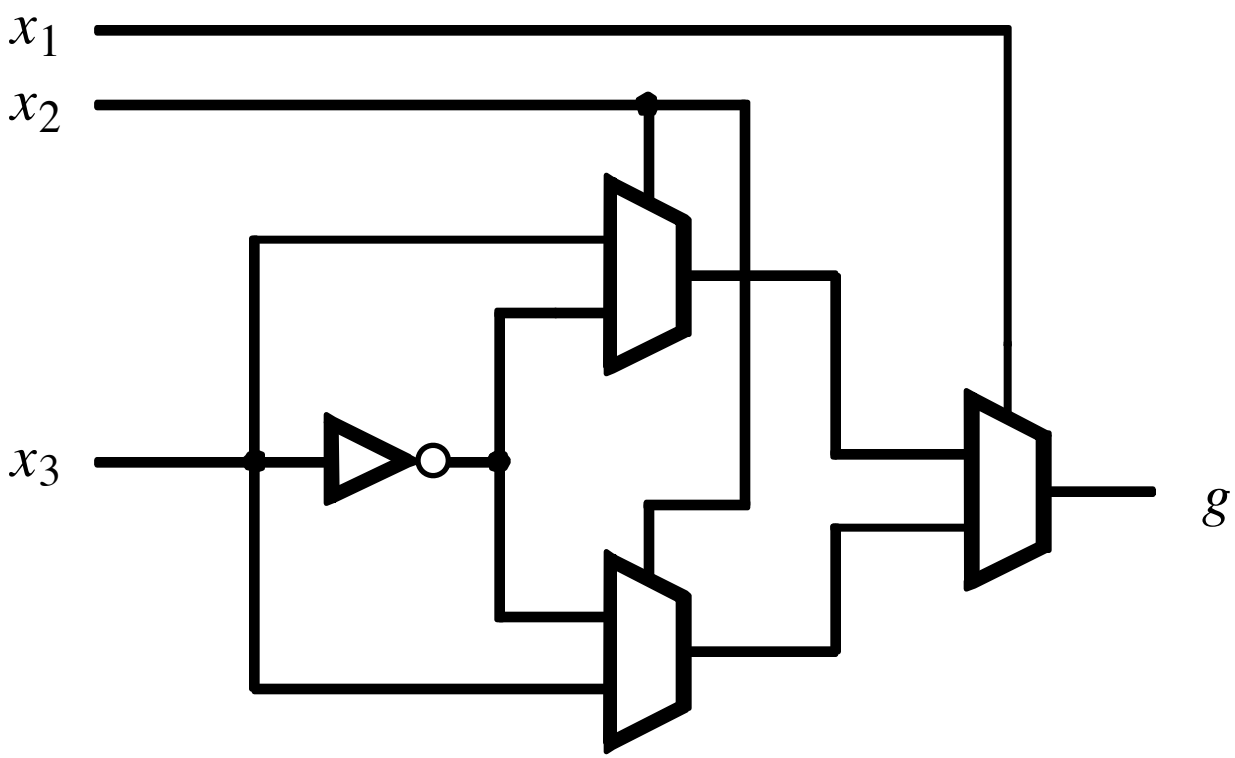


Figure PB.2. A CMOS circuit built with multiplexers.

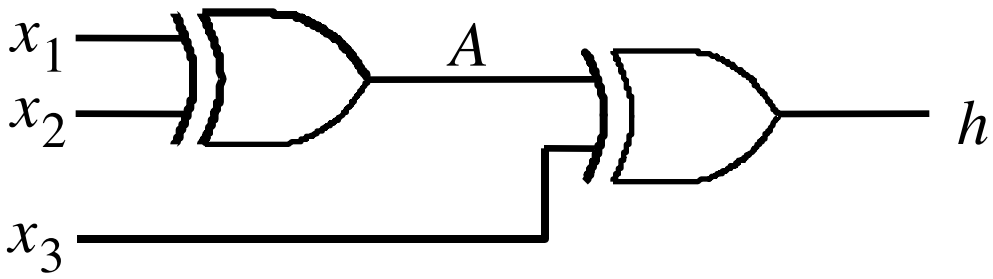


Figure PB.3. Circuit for problem B.3.

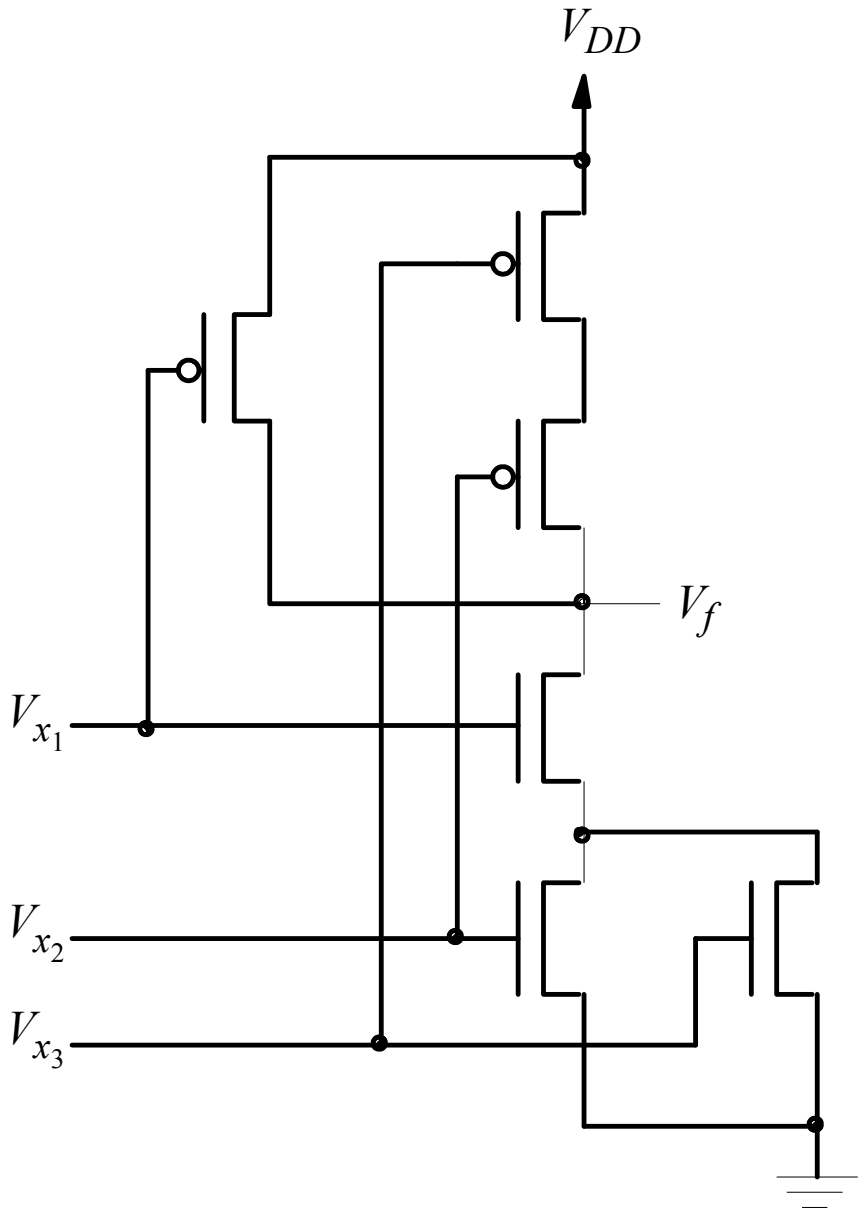


Figure PB.4. A three-input CMOS circuit.

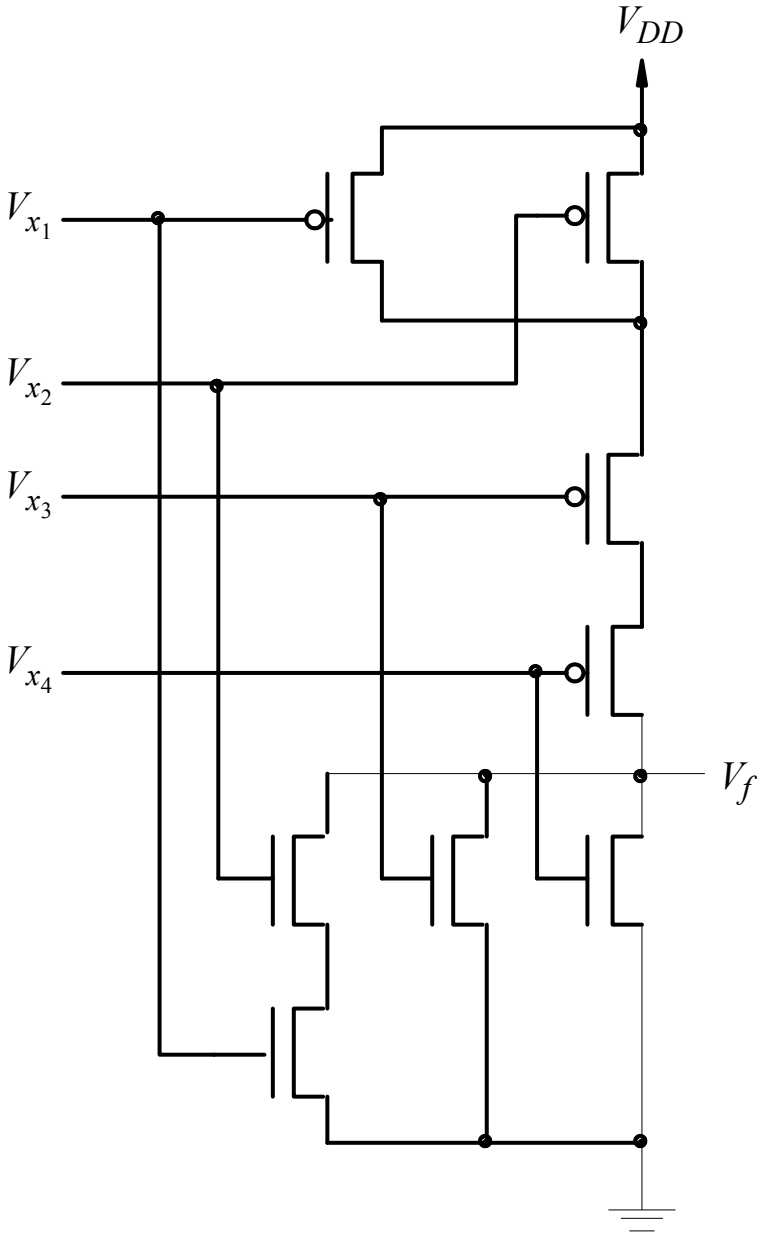


Figure PB.5. A four-input CMOS circuit.

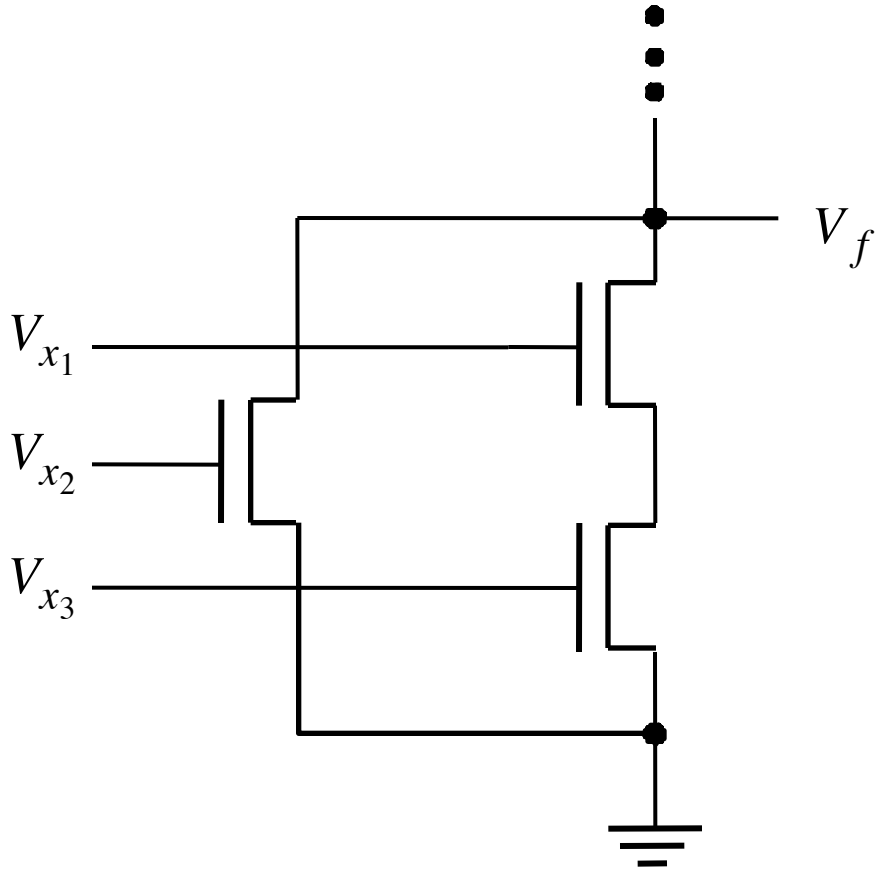


Figure PB.6. The PDN in a CMOS circuit.

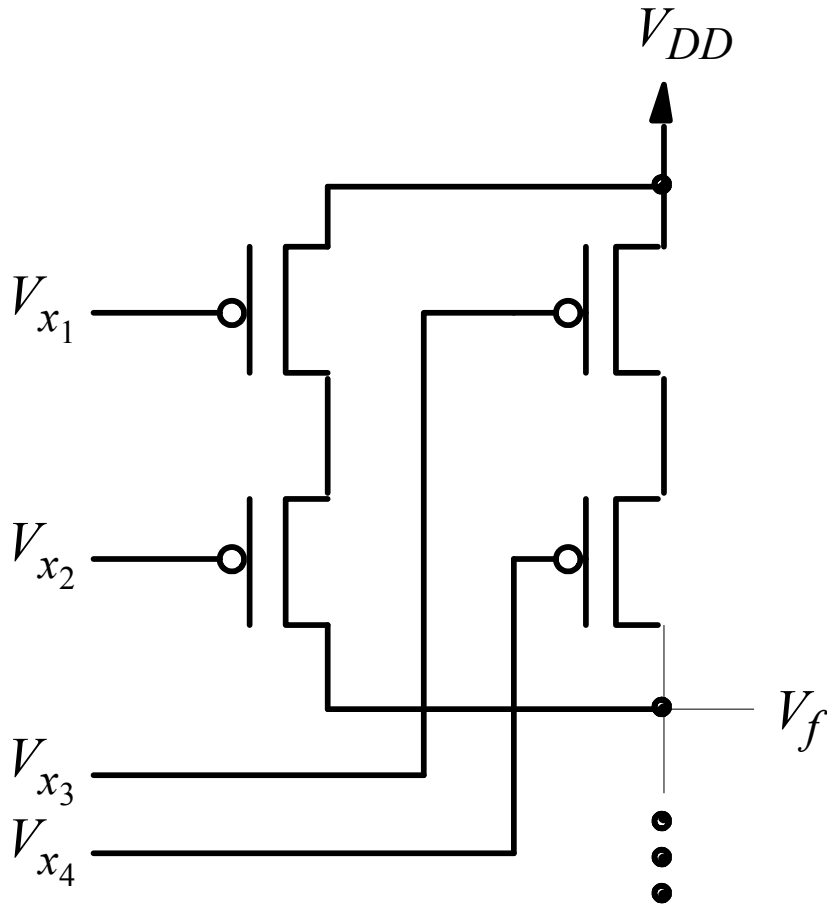


Figure PB.7. The PUN in a CMOS circuit.

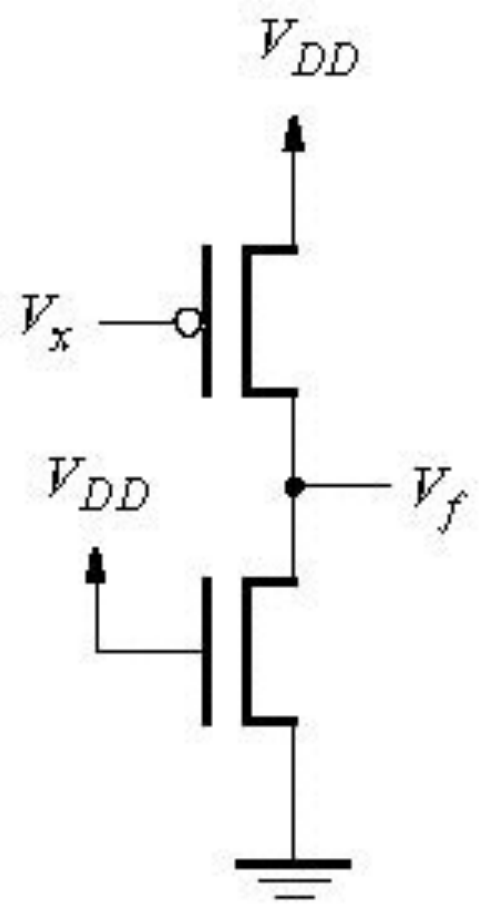


Figure PB.8. The pseudo-PMOS inverter.

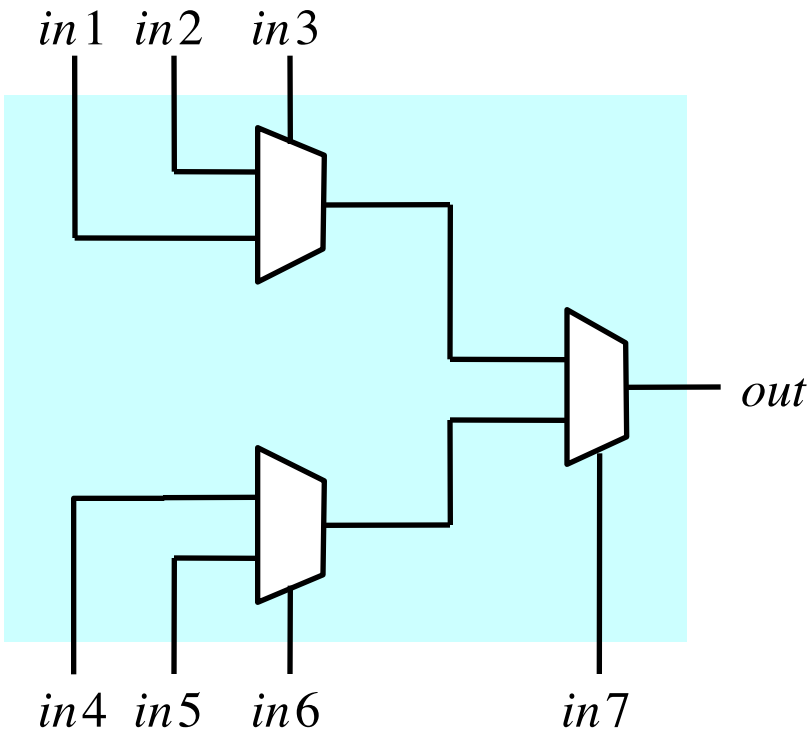


Figure PB.9. A gate-array logic cell.

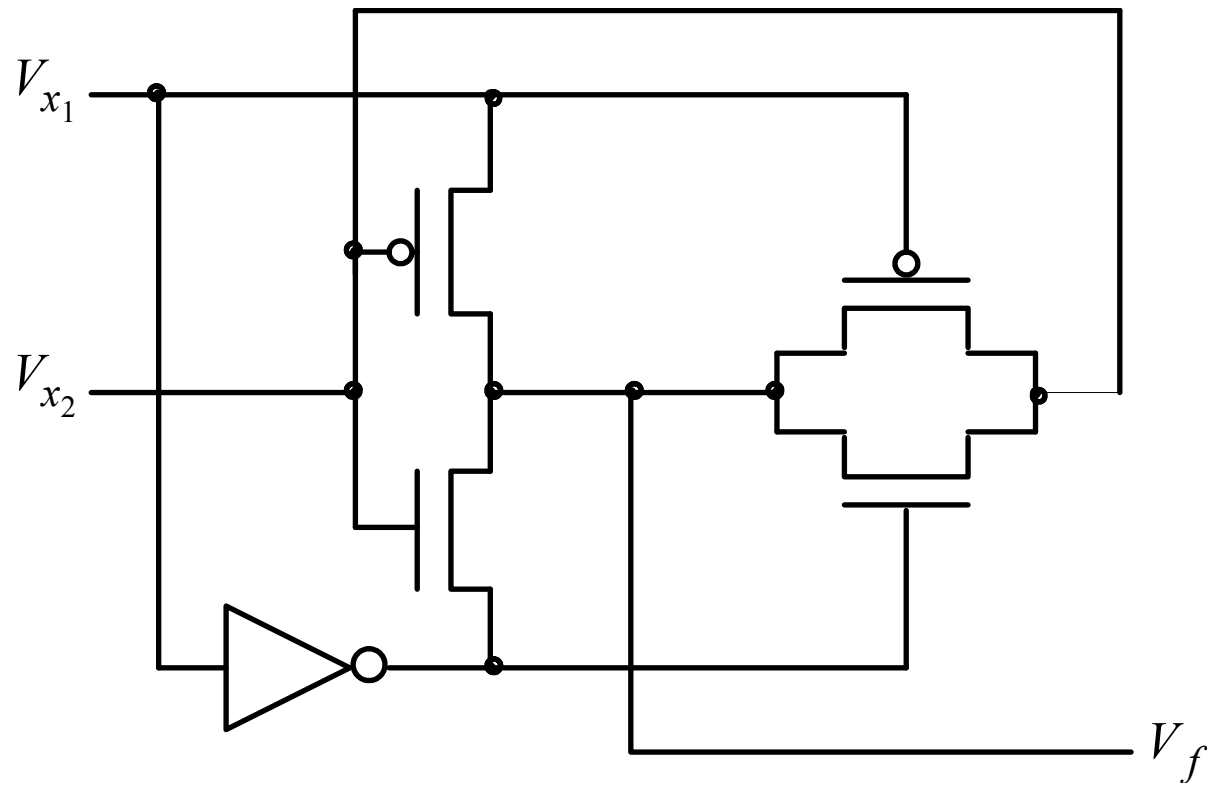


Figure PB.10. Circuit for problem B.51.

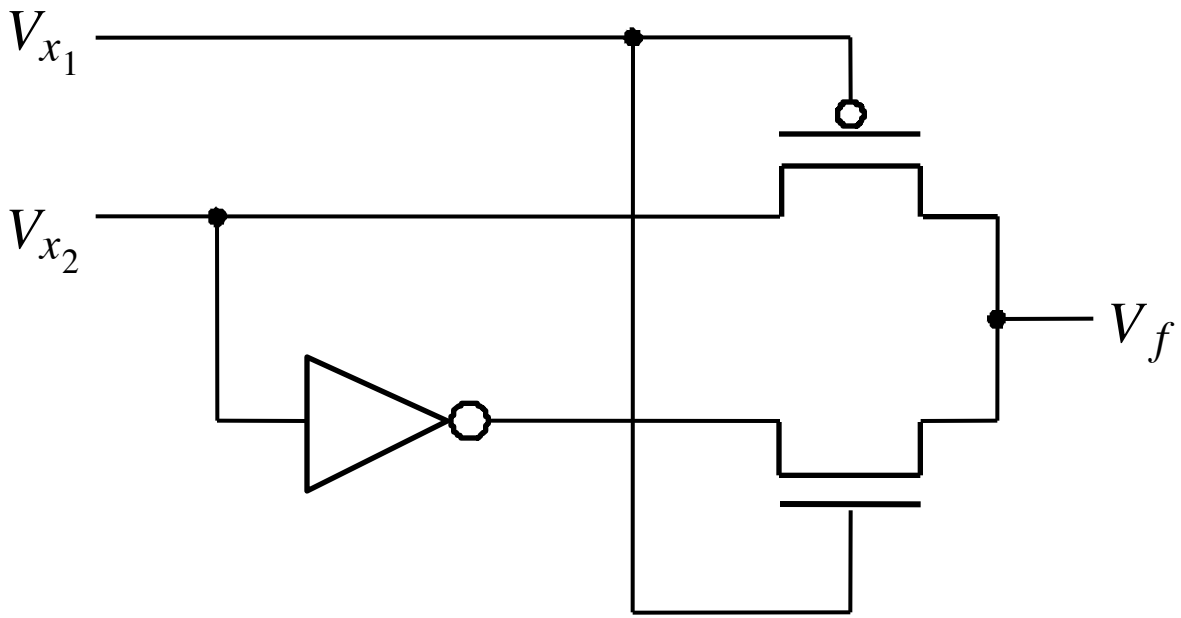


Figure PB.11. Circuit for problem B.52.